



STP62NS04Z

N-CHANNEL CLAMPED 12.5mΩ - 62A TO-220 FULLY PROTECTED MESH OVERLAY™ MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP62NS04Z	CLAMPED	<0.015 Ω	62 A

- TYPICAL R_{DS(on)} = 0.0125 Ω
- 100% AVALANCHE TESTED
- LOW CAPACITANCE AND GATE CHARGE
- 175 °C MAXIMUM JUNCTION TEMPERATURE

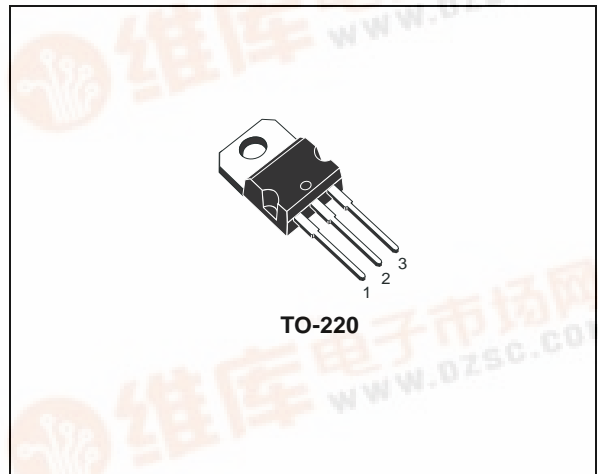
DESCRIPTION

This fully clamped Mosfet is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout.

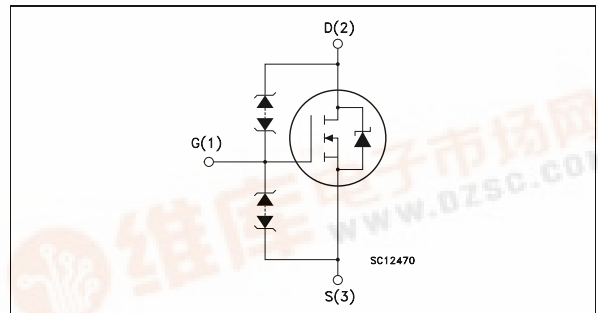
The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

APPLICATIONS

- ABS, SOLENOID DRIVERS
- POWER TOOLS



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP62NS04Z	P62NS04Z	TO-220	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	CLAMPED	V
V _{DG}	Drain-gate Voltage	CLAMPED	V
V _{GS}	Gate- source Voltage	CLAMPED	V
I _D	Drain Current (continuous) at T _C = 25°C	62	A
I _D	Drain Current (continuous) at T _C = 100°C	37.5	A
I _{DG}	Drain Gate Current (continuous)	± 50	mA
I _{GS}	Gate Source Current (continuous)	± 50	mA
I _{DM} (●)	Drain Current (pulsed)	248	A
P _{tot}	Total Dissipation at T _C = 25°C	110	W
	Derating Factor	0.74	W/°C
dv/dt ⁽¹⁾	Peak Diode Recovery voltage slope	8	V/ns
E _{AS} ⁽²⁾	Single Pulse Avalanche Energy	500	mJ
V _{ESD}	ESD (HBM - C = 100pF, R=1.5 kΩ)	8	kV
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Operating Junction Temperature		

(●) Pulse width limited by safe operating area.

(1) I_{SD} ≤ 40A, di/dt ≤ 100A/μs, V_{DD} ≤ V(BR)DSS, T_j ≤ T_{JMAX}

(2) Starting T_j = 25 °C, I_D = 20A, V_{DD} = 20V

STP62NS04Z

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose (for 10 sec., 1.6mm from case)		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Clamped Voltage	I _D = 1 mA, V _{GS} = 0	33			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = 16 V			10	μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 10 V			10	μA
V _{GSS}	Gate-Source Breakdown Voltage	I _{GS} = 100 μA	18			V

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2		4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 30 A		12.5	15	mΩ

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 15 V I _D = 30 A		20		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		1330 420 135		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 20\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		13 104		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 20\text{ V}$ $I_D = 40\text{ A}$ $V_{GS} = 10\text{ V}$		34 10 11.5	47	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 20\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		41 42		ns ns
$t_{r(voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{clamp} = 30\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Inductive Load, Figure 5)		30 54 90		ns ns ns

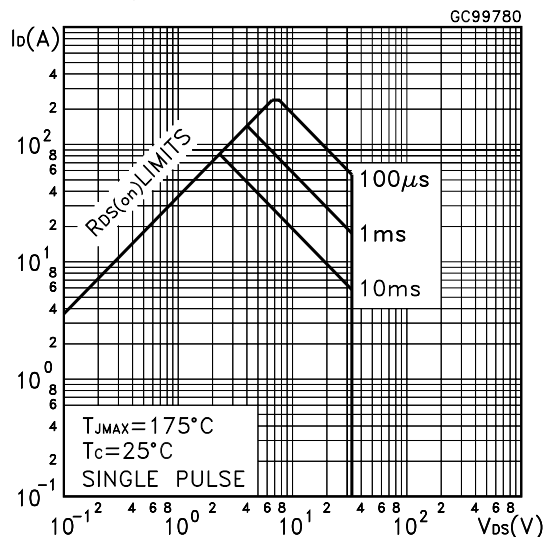
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				62 248	A A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 62\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		45 65 2.9		ns nC A

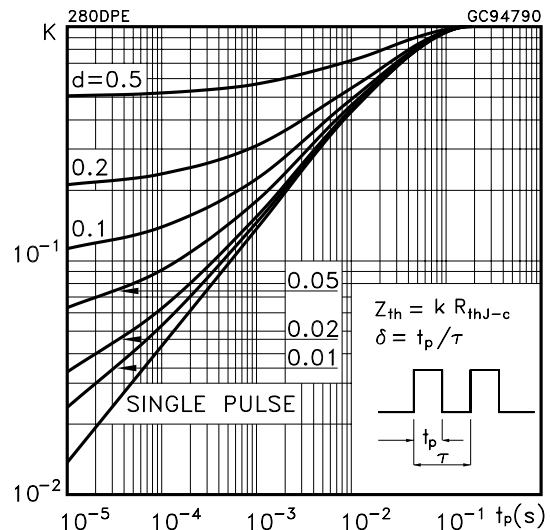
(\ast) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(\bullet) Pulse width limited by safe operating area.

Safe Operating Area

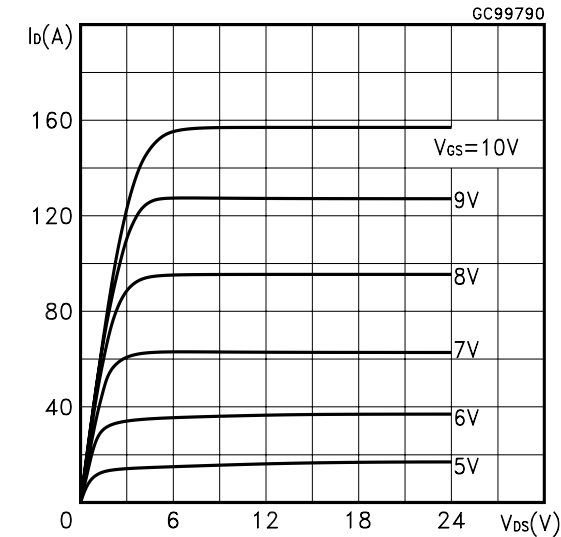


Thermal Impedance

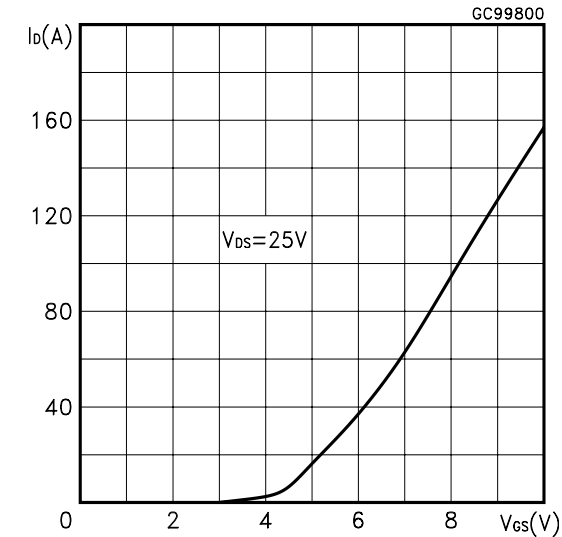


STP62NS04Z

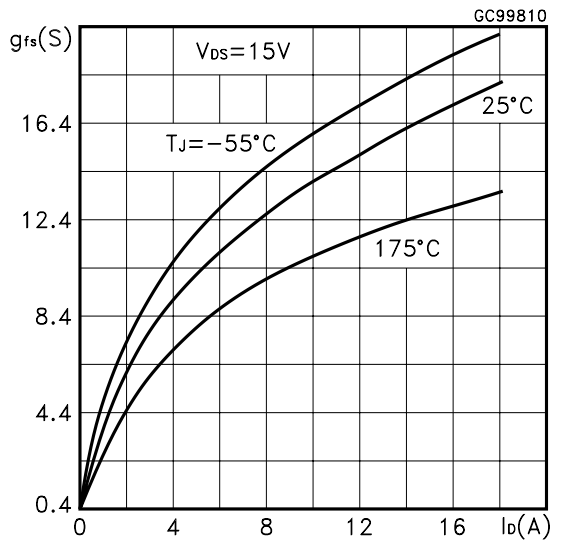
Output Characteristics



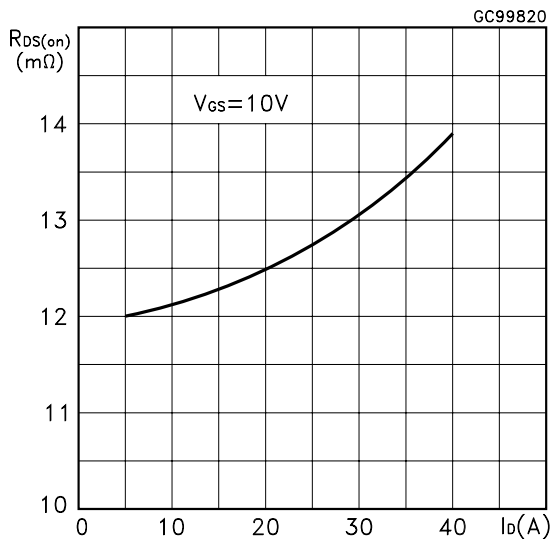
Transfer Characteristics



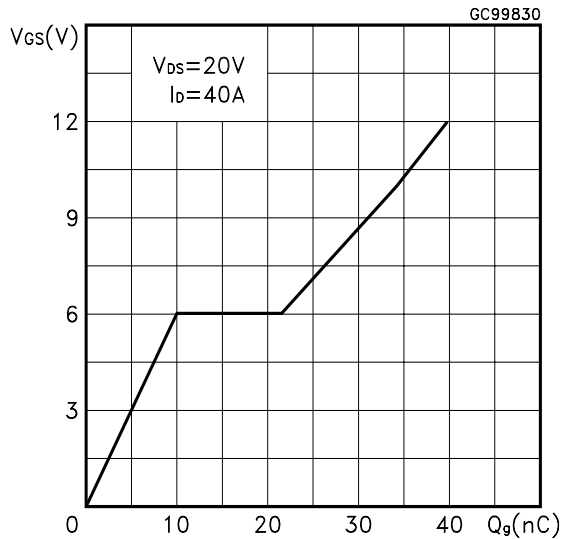
Transconductance



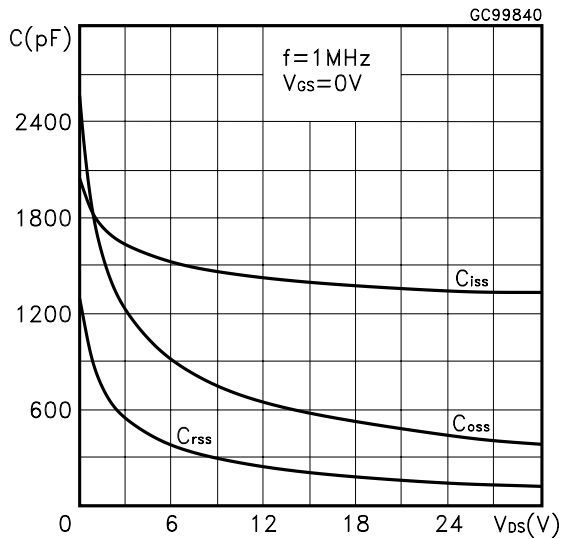
Static Drain-source On Resistance



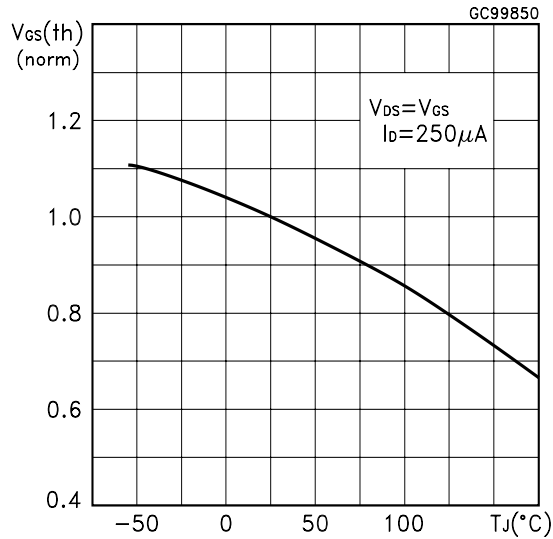
Gate Charge vs Gate-source Voltage



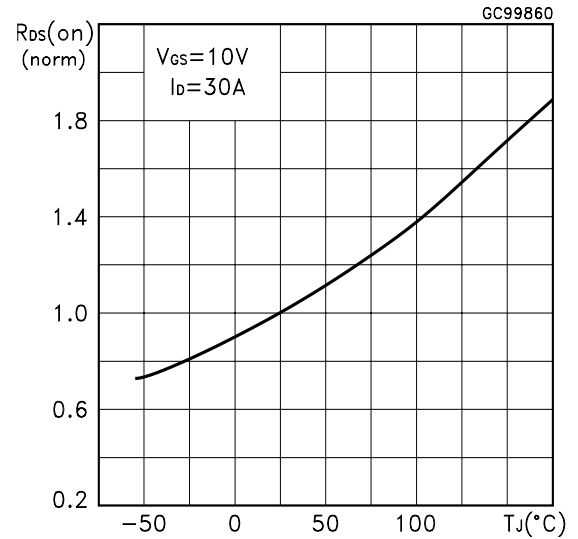
Capacitance Variations



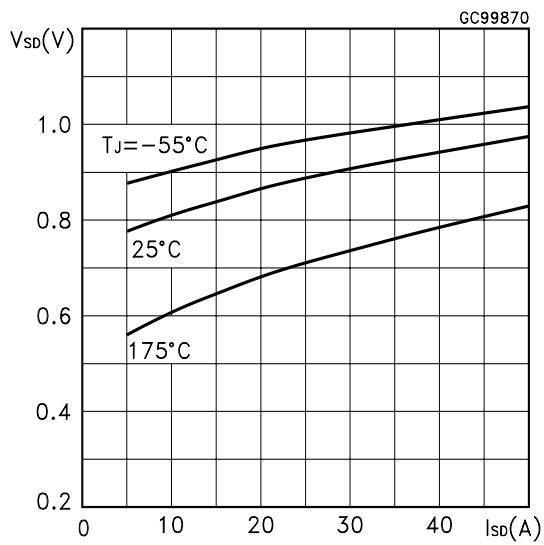
Normalized Gate Threshold Voltage vs Temperature



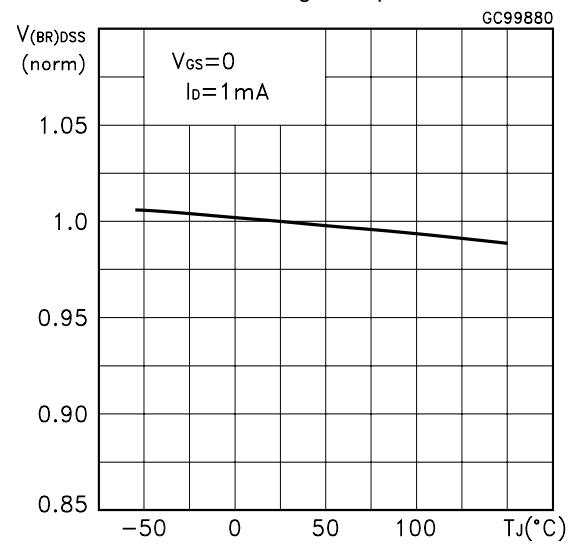
Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage Temperature.



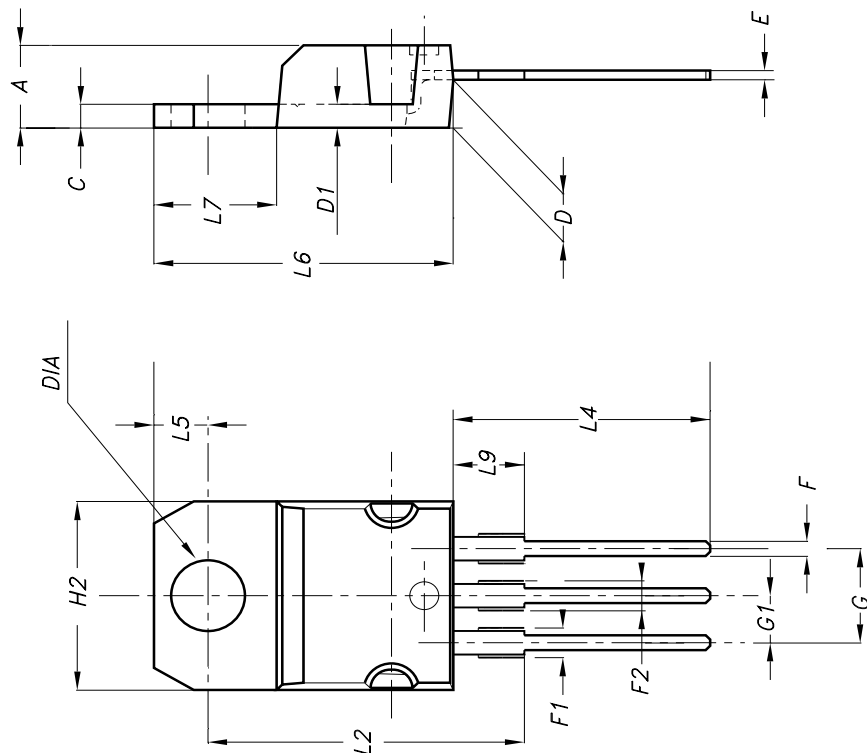
The graph illustrates the unclamped inductive waveforms for a MOSFET during a switching event. The horizontal axis represents time. The vertical axis represents voltage and current. The solid line represents the drain voltage V_D , which rises from 0 to a peak value $V_{(BR)DSS}$ and then falls back to 0. The dashed line represents the drain current I_D , which rises linearly to a peak value I_{DM} and then falls linearly back to 0. The input voltage V_{DD} is shown as a step function that transitions from 0 to a high level during the switching event.

The diagram shows a circuit for testing a Device Under Test (D.U.T.). It includes a 12V supply, a 47K resistor, a 100nF capacitor, a 1K resistor, and a D.U.T. (Device Under Test). The input voltage is $V_i = 20V = V_{GMAX}$. The gate voltage is V_G . The output voltage is V_{DD} . The circuit is labeled SC06000.

[illegible]

TO-220 MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2	16.10	16.40	16.73	0.633	0.645	0.658
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
All other names are the property of their respective owners.

© 2004 STMicroelectronics - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

www.st.com