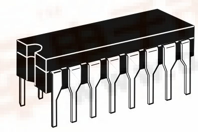
MC14520B
See Page 6-292

MC14521B

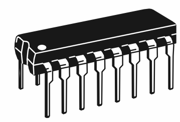
24-Stage Frequency Divider

The MC14521B consists of a chain of 24 flip–flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip–flop divides the frequency of the previous flip–flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven–stages are available for added flexibility.

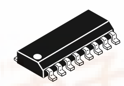
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low–Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load over the Rated Temperature Range.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

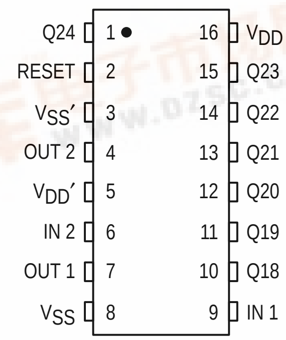
T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

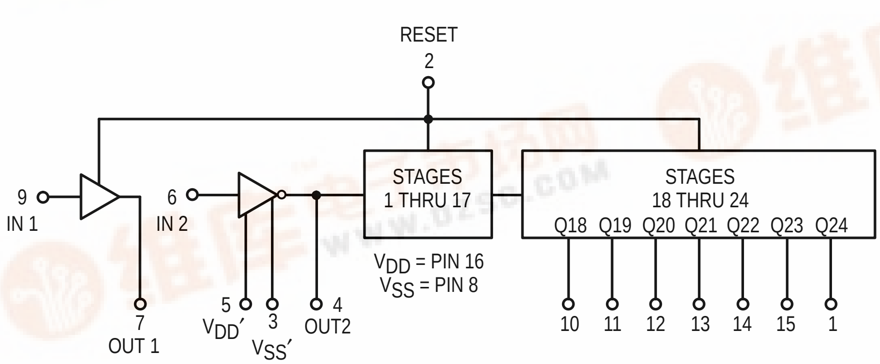
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT



BLOCK DIAGRAM



Output	Count Capacity
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2,097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) Pins 4 & 7 (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 1.2 – 0.25 – 0.62 – 1.8	— — — —	– 1.0 – 0.2 – 0.5 – 1.5	– 1.7 – 0.36 – 0.9 – 3.5	— — — —	– 0.7 – 0.14 – 0.35 – 1.1	— — — —	mAdc
(V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) Pins 1, 10, (V_{OH} = 9.5 Vdc) 11, 12, 13, 14 (V_{OH} = 13.5 Vdc) and 15		5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.42 µA/kHz) f + I_{DD} I_T = (0.85 µA/kHz) f + I_{DD} I_T = (1.40 µA/kHz) f + I_{DD}							µAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time (Counter Outputs)	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	—	40	80	
Propagation Delay Time	t_{PHL}, t_{PLH}					µs
Clock to Q18						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 4415 ns		5.0	—	4.5	9.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 1667 ns		10	—	1.7	3.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1275 ns		15	—	1.3	2.7	
Clock to Q24						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	—	6.0	12	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2167 ns		10	—	2.2	4.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1675 ns		15	—	1.7	3.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 1215 ns		5.0	—	1300	2600	
t_{PHL} = (0.66 ns/pF) C_L + 467 ns		10	—	500	1000	
t_{PHL} = (0.5 ns/pF) C_L + 350 ns		15	—	375	750	
Clock Pulse Width	$t_{WH(cl)}$	5.0	385	140	—	ns
		10	150	55	—	
		15	120	40	—	
Clock Pulse Frequency	f_{cl}	5.0	—	3.5	2.0	MHz
		10	—	9.0	5.0	
		15	—	12	6.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	µs
		10	—	—	5.0	
		15	—	—	4.0	
Reset Pulse Width	$t_{WH(R)}$	5.0	1400	700	—	ns
		10	600	300	—	
		15	450	225	—	
Reset Removal Time	t_{rem}	5.0	30	– 200	—	ns
		10	0	– 160	—	
		15	– 40	– 110	—	

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

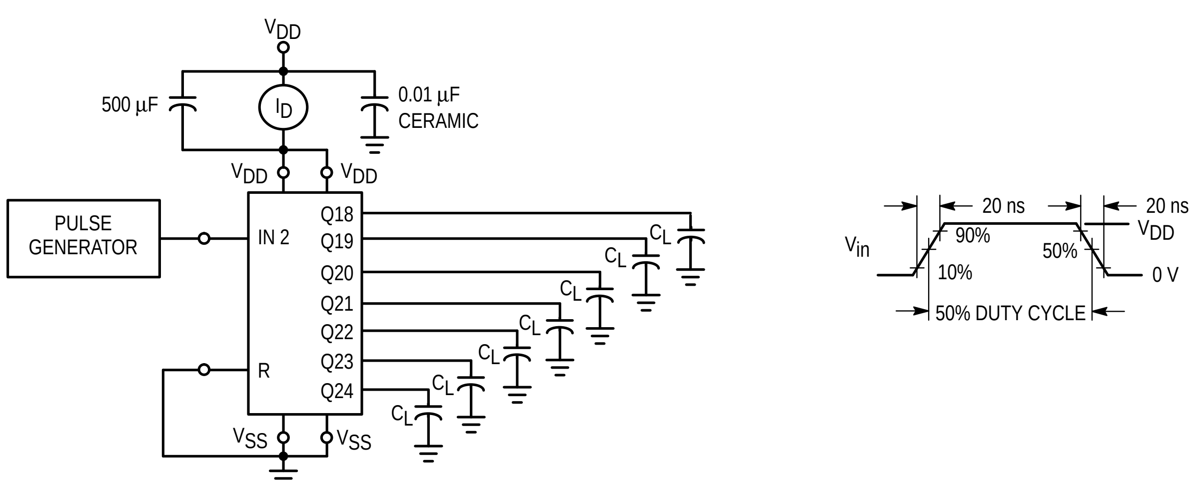


Figure 1. Power Dissipation Test Circuit and Waveform

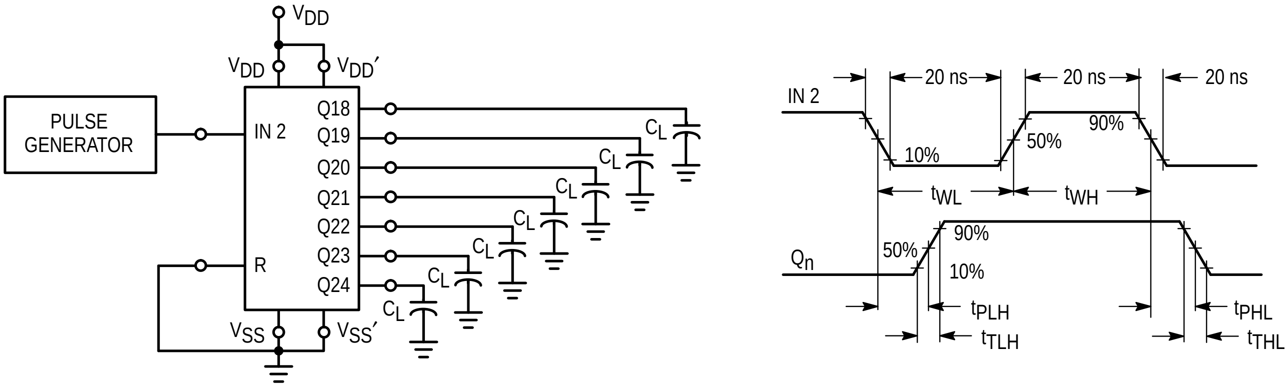
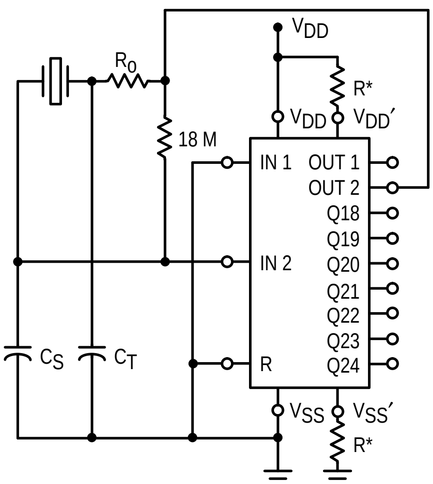


Figure 2. Switching Time Test Circuit and Waveforms



* Optional for low power operation,
10 kΩ ≤ R ≤ 70 kΩ.

Figure 3. Crystal Oscillator Circuit

Characteristic	500 kHz Circuit	50 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+ 6.0	+ 2.0	ppm
V_{DD} Change from 10 V to 15 V	+ 2.0	+ 2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from – 55°C to + 25°C			
MC14521 only	– 4.0	– 2.0	ppm
Complete Oscillator*	+ 100	+ 120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	– 2.0	– 2.0	ppm
Complete Oscillator*	– 160	– 560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

Figure 4. Typical Data for Crystal Oscillator Circuit

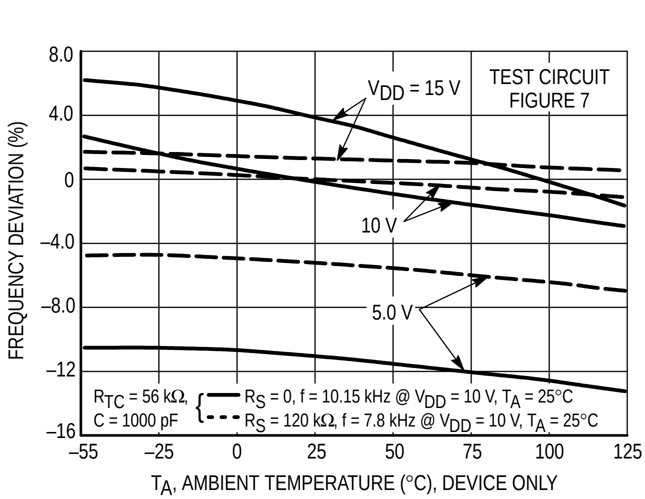


Figure 5. RC Oscillator Stability

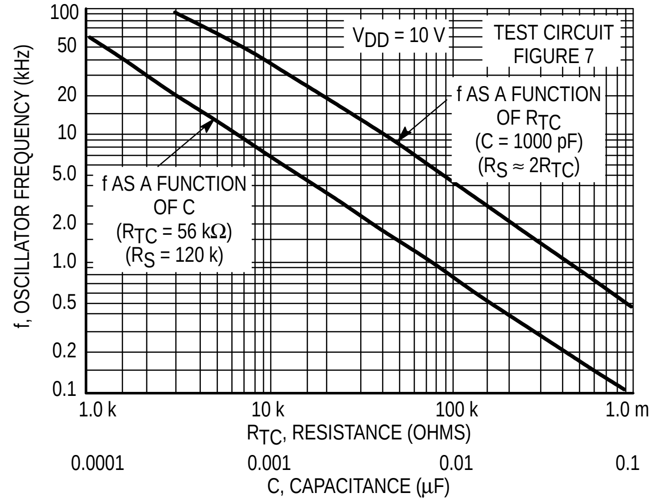


Figure 6. RC Oscillator Frequency as a Function of R_{TC} and C

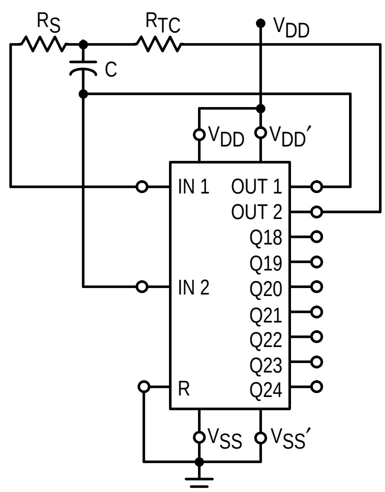


Figure 7. RC Oscillator Circuit

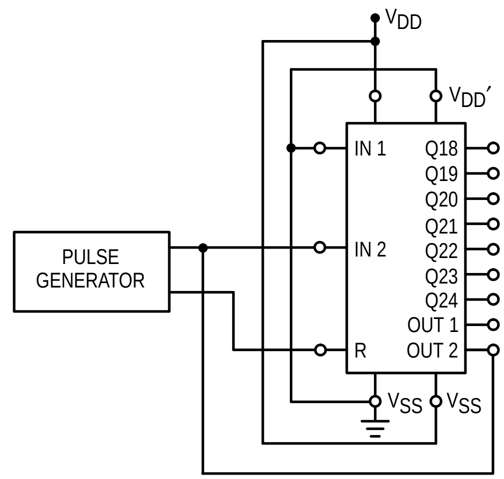


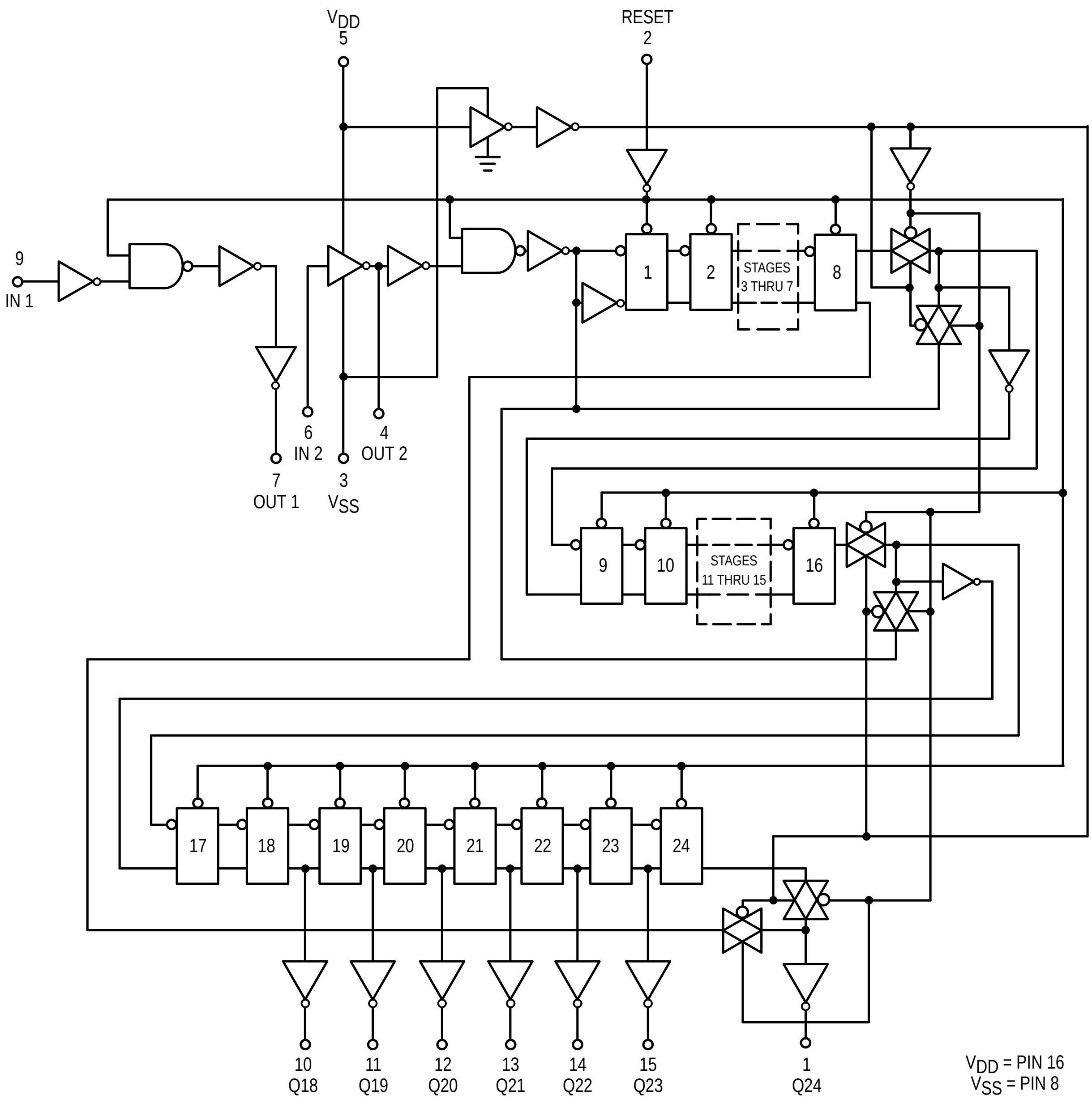
Figure 8. Functional Test Circuit

FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8–stage sections, and 255 counts are loaded in each of the 8–stage sections in parallel. All flip–flops are now at a logic "1". The counter is now returned to the normal 24–stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

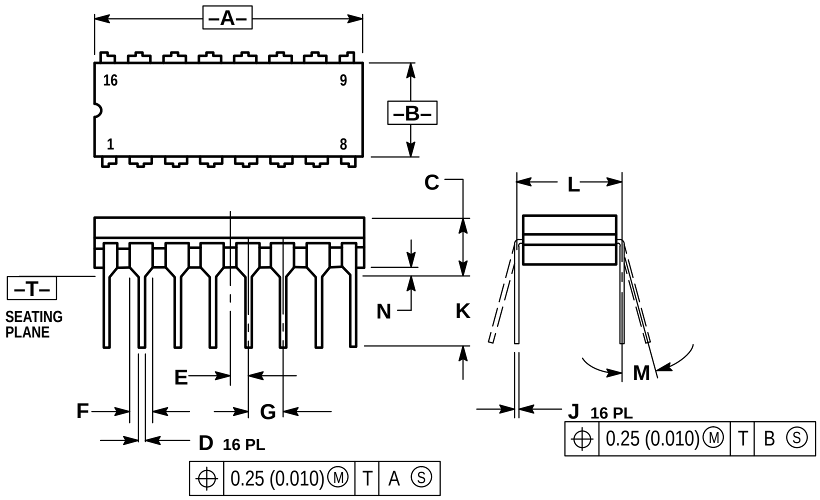
Inputs		Outputs				Comments
Reset	In 2	Out 2	$V_{SS}′$	$V_{DD}′$	Q18 thru Q24	
1	0	0	V_{DD}	Gnd	0	Counter is in three 8–stage sections in parallel mode Counter is reset. In 2 and Out 2 are connected together
0 ↓	1	1	↓	↓		First "0" to "1" transition on In 2, Out 2 node.
	0 1 — — —	0 1 — — —				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
	1	1			1	The 255th "0" to "1" transition.
	0 0	0 0	Gnd		1 1	
	1	0	↓	V_{DD}	1	Counter converted back to 24–stages in series mode.
	1	0		↓	1	Out 2 converts back to an output.
↓	0	1	↓	↓	0	Counter ripples from an all "1" state to an all "0" stage.

LOGIC DIAGRAM



OUTLINE DIMENSIONS

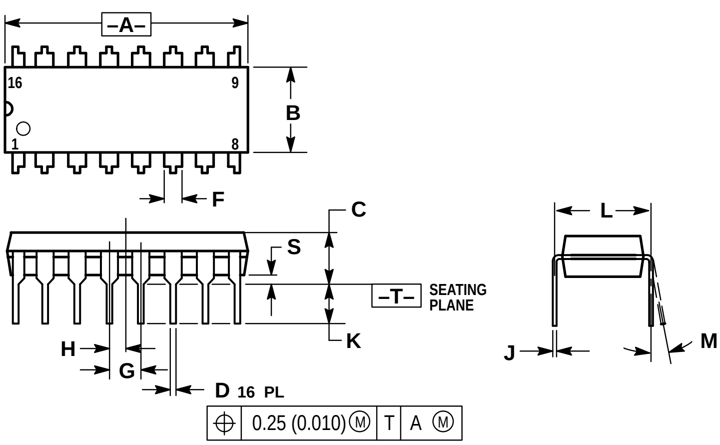
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

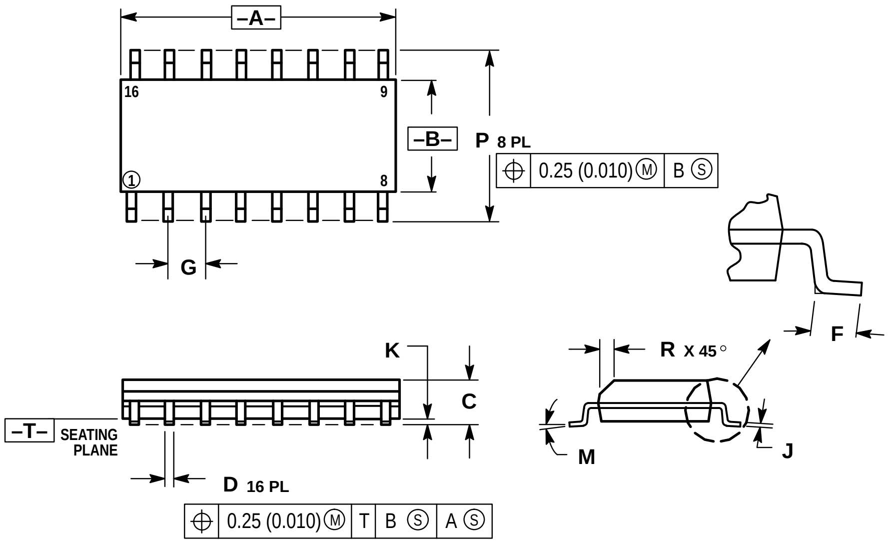


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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