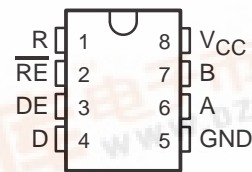


- **Bidirectional Transceiver With Fail-Safe Receiver**
- **Meets or Exceeds the Requirements of ITU Recommendation V.11**
- **Electrically Compatible With ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ± 60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedance . . . 12 k Ω Min**
- **Receiver Input Sensitivity . . . -300 mV/0 mV**
- **Operates From Single 5-V Supply**
- **Pin-to-Pin Compatible With SN75176A**

**D OR P PACKAGE
(TOP VIEW)**



description

The SN75276 differential bus transceiver is a monolithic, integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and is electrically compatible with ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A, and meets ITU Recommendation V.11.

The fail-safe operation ensures a known level on the circuit output under bus fault conditions. The circuit provides a high-level output under floating-line, idle-line, open-circuit, and short-circuit bus conditions (see Function Tables).

The SN75276 combines a 3-state, differential line driver and a differential input line receiver, both of which operate from a single, 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k Ω .

The SN75276 can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

SN75276 is characterized for operation from 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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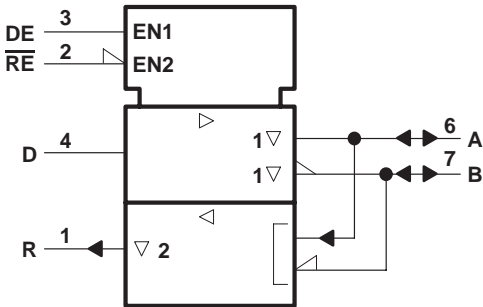
Function Tables

EACH DRIVER			
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

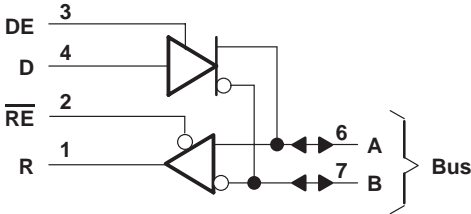
EACH RECEIVER		
DIFFERENTIAL A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0\text{ V}$	L	H
$-0.3\text{ V} < V_{ID} < 0\text{ V}$	L	?
$V_{ID} \leq -0.3$	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



logic diagram (positive logic)



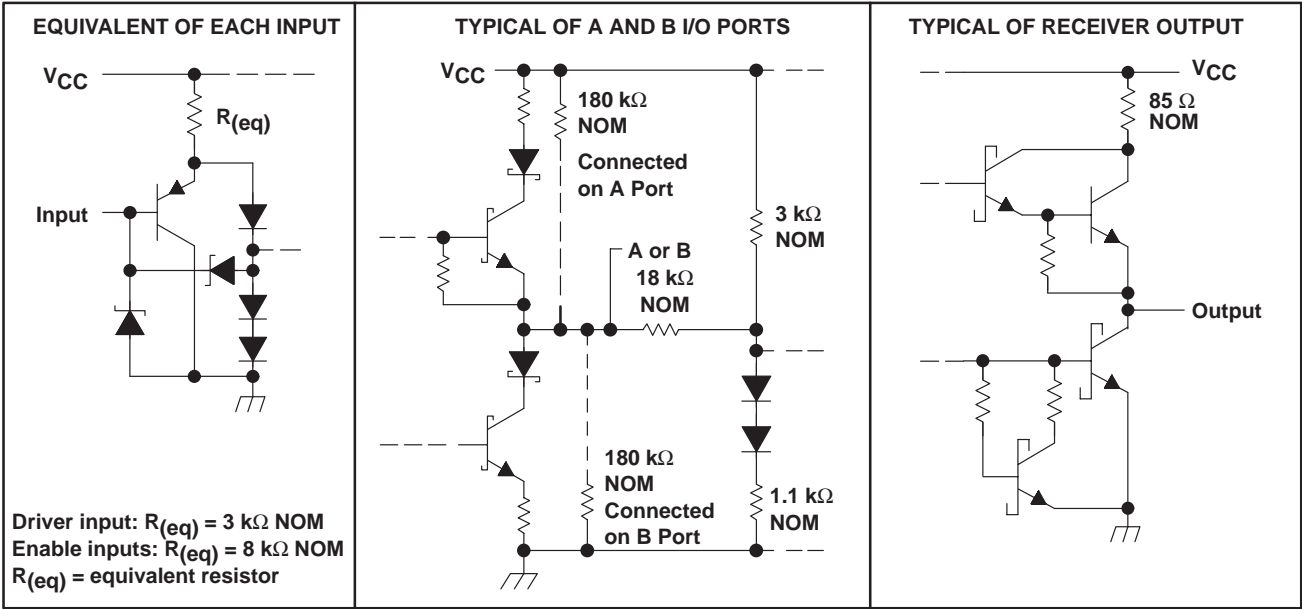
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage at any bus terminal	–10 V to 15 V
Enable input voltage, V_I	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 105^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	704 mW	396 mW

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recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V _I or V _{IC}		12			V
		−7			
High-level input voltage, V _{IH}	D, DE, and \overline{RE}	2			V
Low-level input voltage, V _{IL}	D, DE, and \overline{RE}	0.8			V
Differential input voltage, V _{ID} (see Note 2)		±12			V
High-level output current, I _{OH}	Driver	−60			mA
	Receiver	−400			μA
Low-level output current, I _{OL}	Driver	60			mA
	Receiver	8			
Operating free-air temperature, T _A		0		70	°C

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5	3.6	6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$, See Figure 1	$1/2 V_{OD1}$ or 2§			V
	$R_L = 54 \Omega$, See Figure 1	1.5	2.5	5	V
V_{OD3} Differential output voltage	See Note 3	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage¶	$R_L = 54 \Omega$ or 100Ω , See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage				+3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage¶				± 0.2	V
I_O Output current	Output disabled, See Note 4	$V_O = 12 \text{ V}$		1	mA
		$V_O = -7 \text{ V}$		-0.8	
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$			-400	μA
I_{OS} Short-circuit output current	$V_O = -7 \text{ V}$			-250	mA
	$V_O = 0$			150	
	$V_O = V_{CC}$			250	
	$V_O = 12 \text{ V}$			250	
I_{CC} Supply current (total package)	No load	Outputs enabled	42	70	mA
		Outputs disabled	26	35	

† The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $1/2 V_{OD1}$ or 2 V , whichever is greater.

¶ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

NOTES: 3. This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

4. See TIA/EIA-485-A Figure 3.5, Test Termination Measurement 2.

switching characteristics, $V_{CC} = 5 \text{ V}$, $R_L = 110 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential-output delay time	$R_L = 54 \Omega$, See Figure 3		15	22	ns
$t_{t(OD)}$ Differential-output transition time			20	30	ns
t_{PZH} Output enable time to high level	See Figure 4		85	120	ns
t_{PZL} Output enable time to low level	See Figure 5		40	60	ns
t_{PHZ} Output disable time from high level	See Figure 4		150	250	ns
t_{PLZ} Output disable time from low level	See Figure 5		20	30	ns

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DRIVER SECTION

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$ V_{OD1} $	V_o	V_o
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
V_{OD3}	None	V_t (Test Termination Measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = 2.7 \text{ V}$, $I_O = -0.4 \text{ mA}$			0	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.5 \text{ V}$, $I_O = 8 \text{ mA}$	-0.3^\ddagger			V
V_{IK} Enable clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 0$, See Figure 2 $I_{OH} = -400 \mu\text{A}$,	2.7			V
V_{OL} Low-level output voltage	$V_{ID} = -300 \text{ mV}$, See Figure 2 $I_{OL} = 8 \text{ mA}$,			0.45	V
I_{OZ} High-impedance-state output current	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$			± 20	μA
I_I Line input current	Other input = 0 V, See Note 5	$V_I = 12 \text{ V}$		1	mA
		$V_I = -7 \text{ V}$		-0.8	
I_{IH} High-level enable input current	$V_{IH} = 2.7 \text{ V}$			20	μA
I_{IL} Low-level enable input current	$V_{IL} = 0.4 \text{ V}$			-100	μA
r_i Input resistance	$V_I = 12 \text{ V}$	12			$\text{k}\Omega$
I_{OS} Short-circuit output current		-15		-85	mA
I_{CC} Supply current (total package)	No load	Outputs enabled	42	55	mA
		Outputs disabled	26	35	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for negative-going input threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

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RECEIVER SECTION

switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = 0\text{ to }3\text{ V}$, See Figure 6		21	35	ns
t_{PHL} Propagation delay time, high- to low-level output			23	35	ns
t_{PZH} Output enable time to high level	See Figure 7		10	20	ns
t_{PZL} Output enable time to low level			12	20	ns
t_{PHZ} Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ} Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

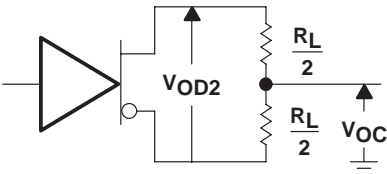


Figure 1. Driver V_{OD} and V_{OC}

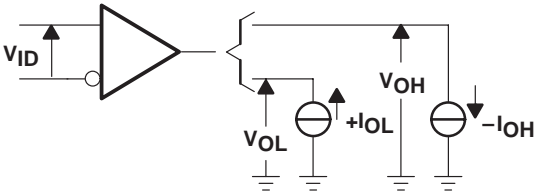
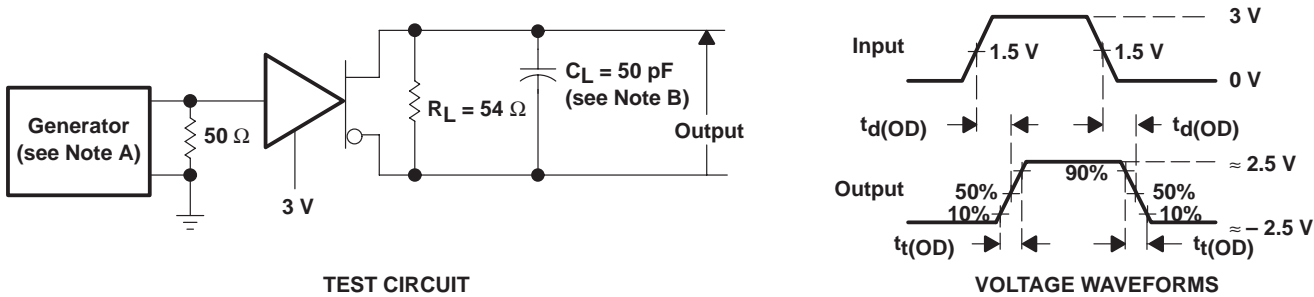


Figure 2. Receiver V_{OH} and V_{OL}



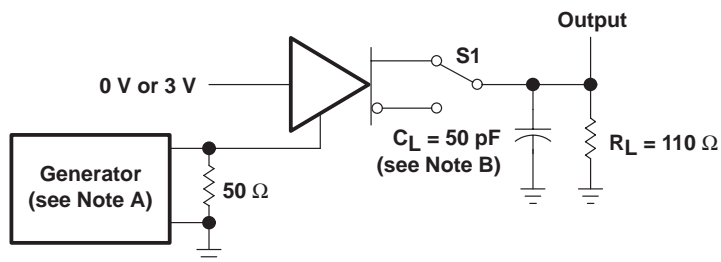
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $Z_O = 50\text{ }\Omega$.
- B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

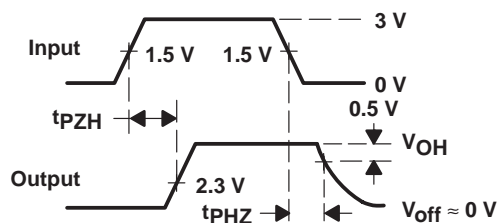
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PARAMETER MEASUREMENT INFORMATION



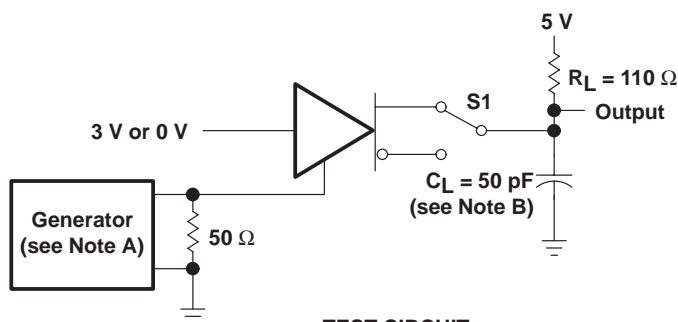
TEST CIRCUIT



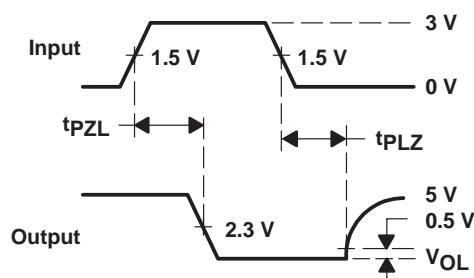
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms



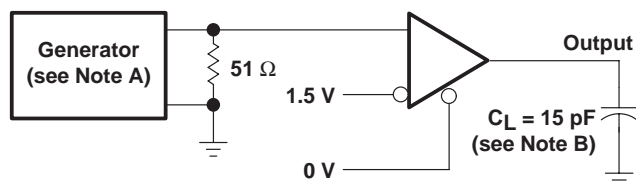
TEST CIRCUIT



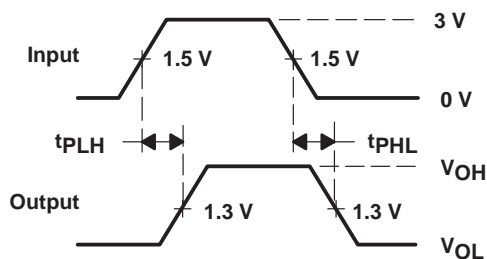
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

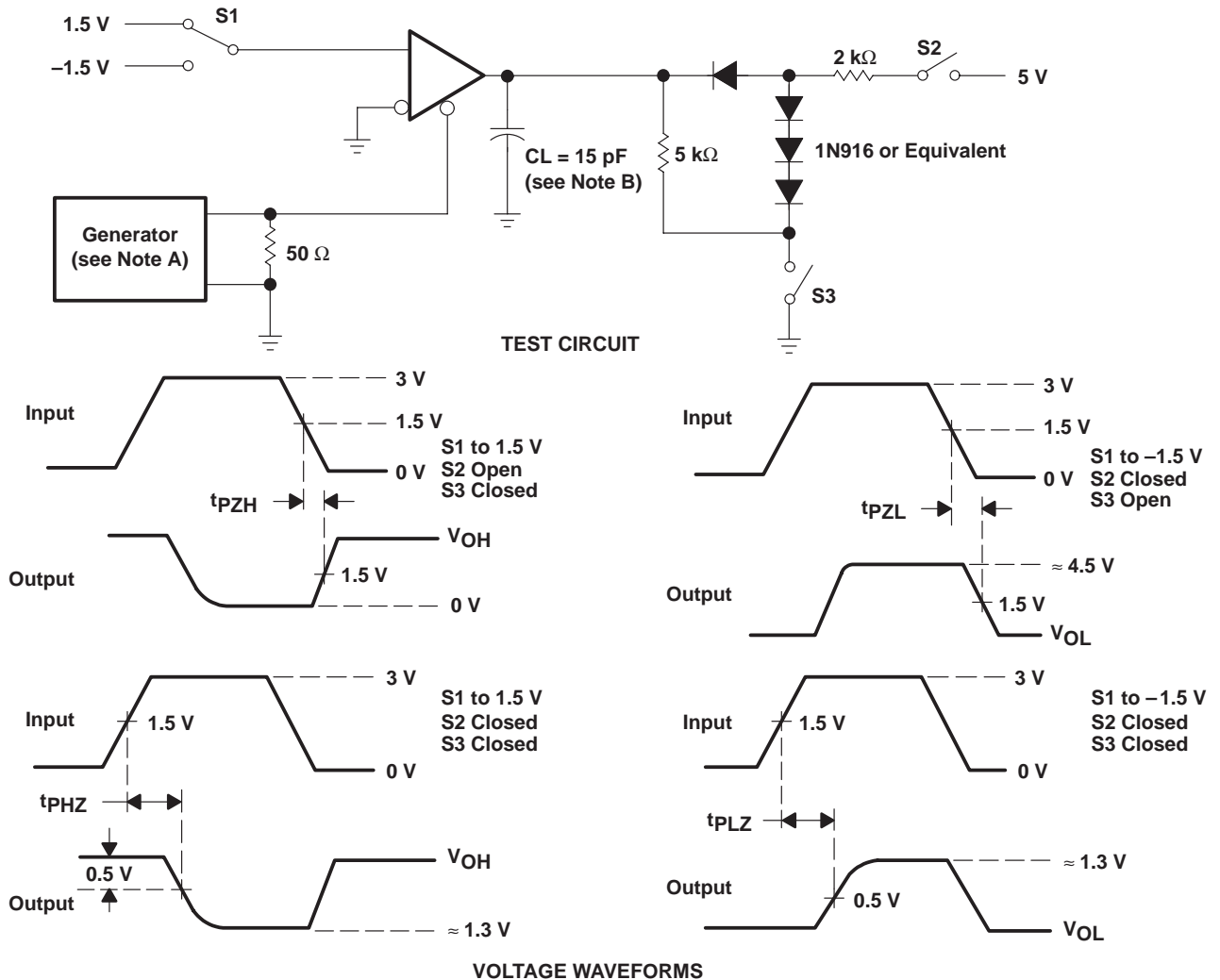
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

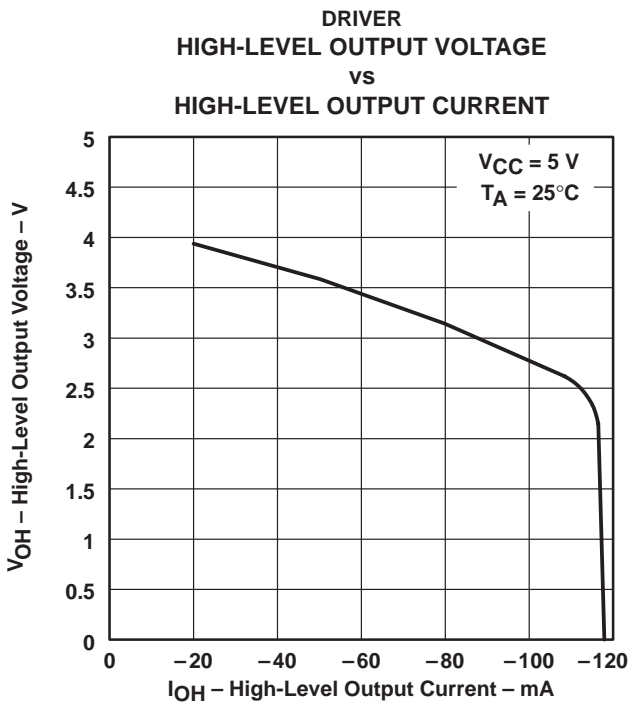


Figure 8

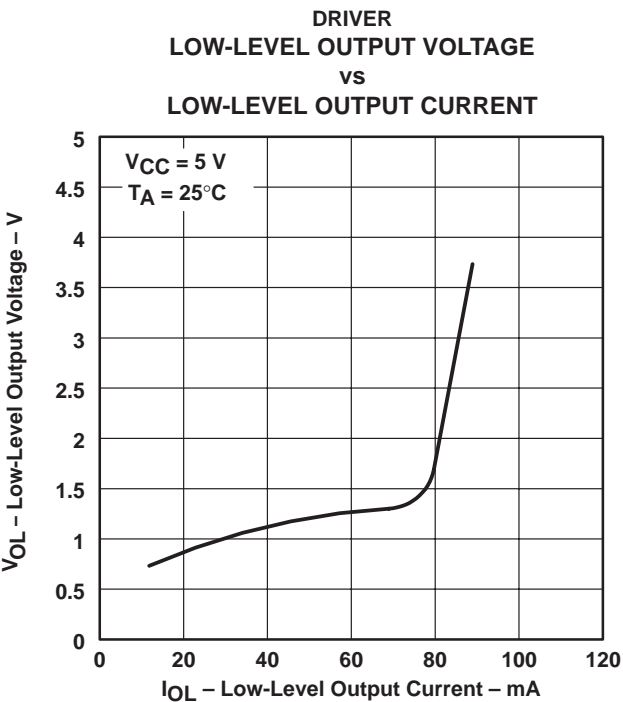


Figure 9

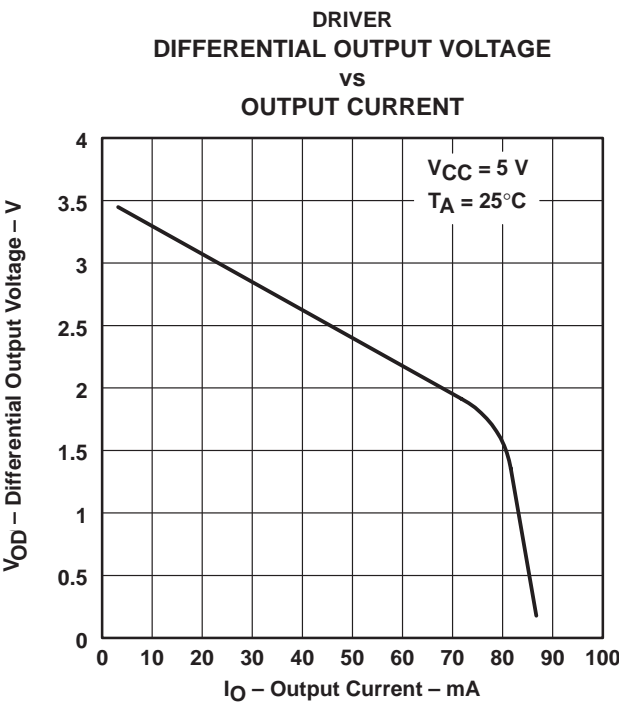


Figure 10

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TYPICAL CHARACTERISTICS†

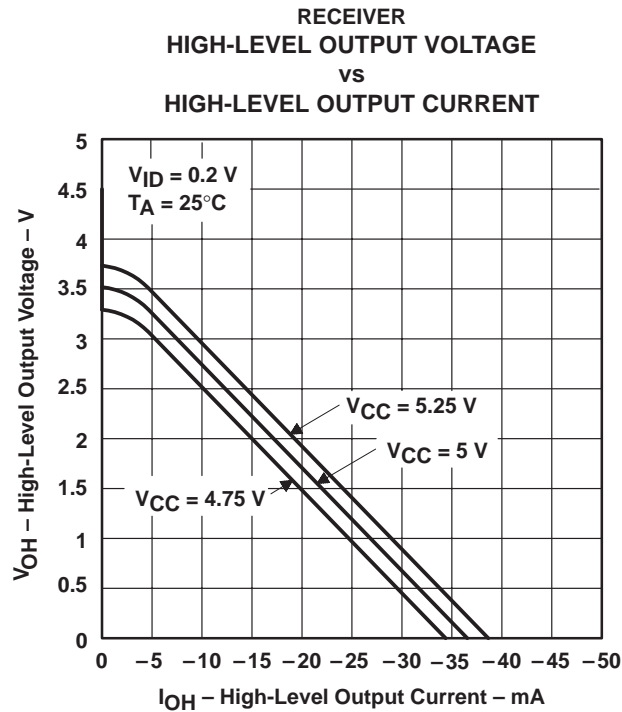


Figure 11

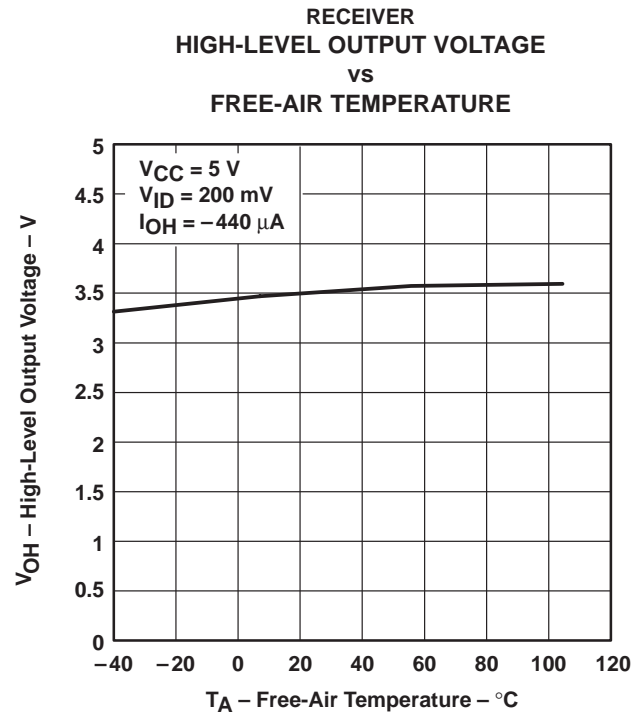


Figure 12

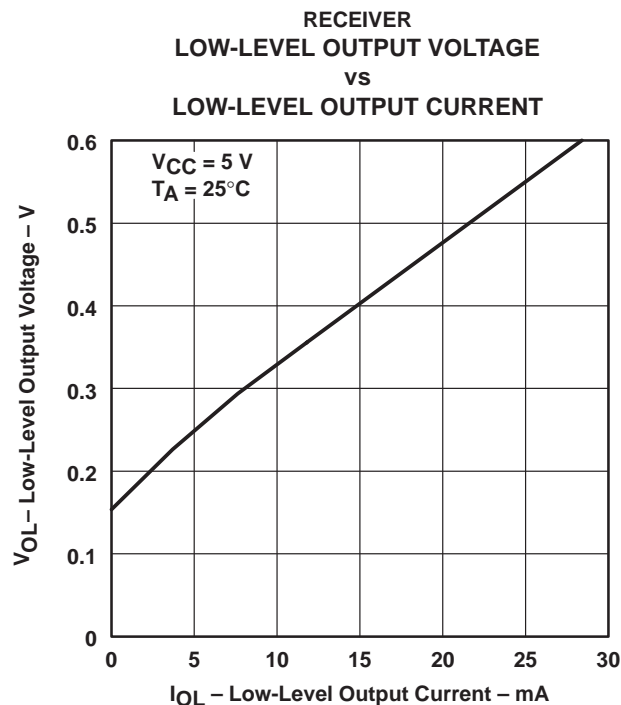


Figure 13

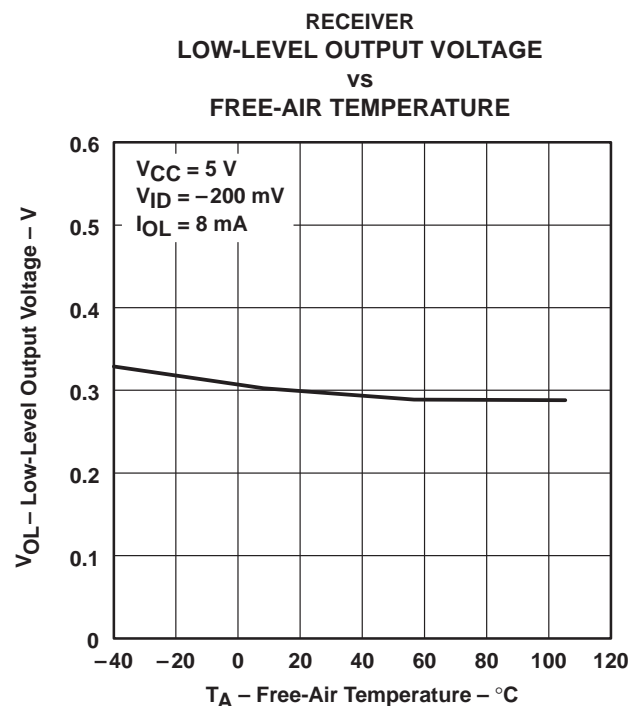


Figure 14

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS

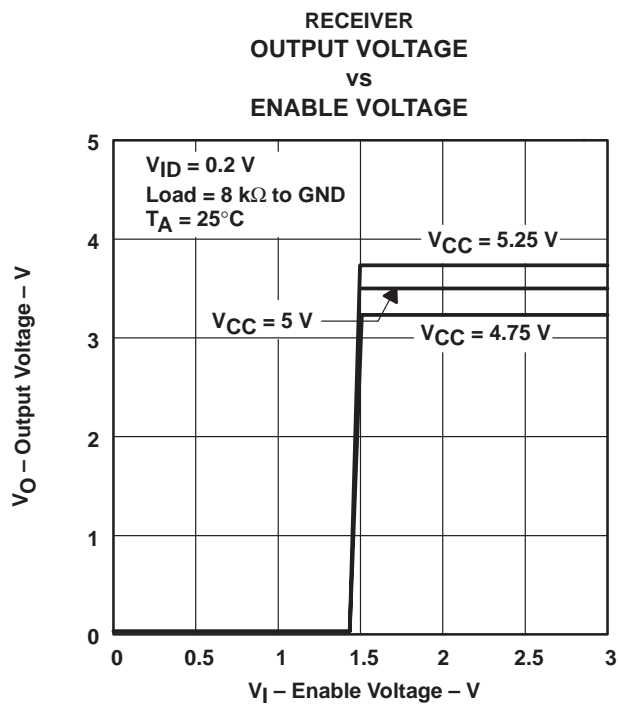


Figure 15

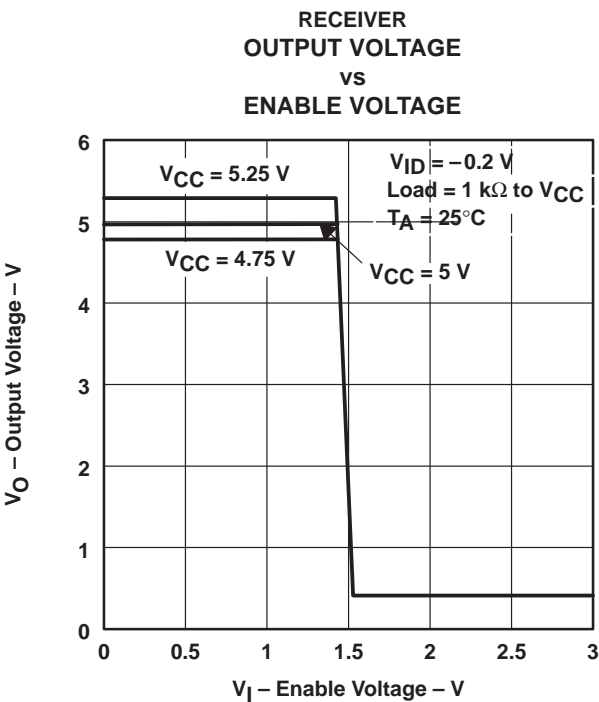
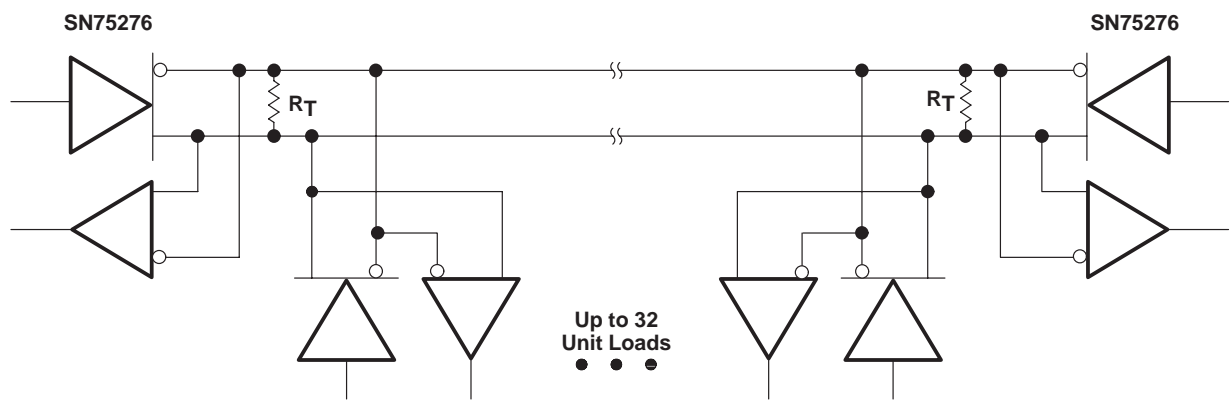


Figure 16

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible ($R_T = Z_O$).

Figure 17. Typical Application Circuit

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