

MOTOROLA

SEMICONDUCTOR TECHNICAL DATA

Voltage Controlled Oscillator

Consider MC12148 for New Designs

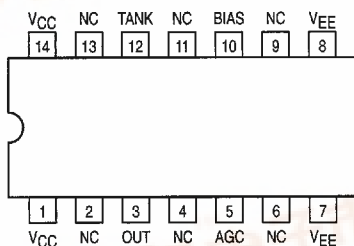
The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). **For Maximum Performance $Q_L \geq 100$ at Frequency of Operation.**

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 14. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 7)

The MC1648 may be operated from a +5.0Vdc supply or a -5.2Vdc supply, depending upon system requirements.

NOTE: The MC1648 is NOT useable as a crystal oscillator.

Pinout: 14-Lead Package (Top View)



Pin assignment is for Dual-in-Line Package.

For PLLC pin assignment, see the MC1648 Non-Standard Pin Conversion Table below.

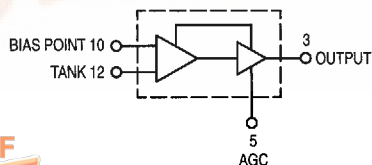
MC1648 NON-STANDARD PIN CONVERSION DATA

Package	TANK	VCC	VCC	OUT	AGC	VEE	VEE	BIAS
8 D	1	2	3	4	5	6	7	8
14 L,P	12	14	1	3	5	7	8	10
20FN	18	20	2	4	8	10	12	14

*NOTE - All unused pins are not connected.

Supply Voltage	GND Pins	Supply Pins
+5.0Vdc	7,8	1,14
-5.2Vdc	1,14	7,8

LOGIC DIAGRAM



- Input Capacitance = 6.0pF (TYP)
- Maximum Series Resistance for L (External Inductance) = 50Ω (TYP)
- Power Dissipation = 150mW (TYP)/Pkg (+5.0Vdc Supply)
- Maximum Output Frequency = 225MHz (TYP)

VCC1 = Pin 1
VCC2 = Pin 14
VEE = Pin 7

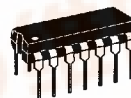
MC1648

VOLTAGE CONTROLLED OSCILLATOR



L SUFFIX
14-LEAD CERAMIC PACKAGE
CASE 632-08

Not Recommended for New Designs



P SUFFIX
14-LEAD PLASTIC PACKAGE
CASE 646-06



D SUFFIX
8-PIN PLASTIC SOIC PACKAGE
CASE 751-05



FN SUFFIX
20-LEAD PLCC PACKAGE
CASE 775-02



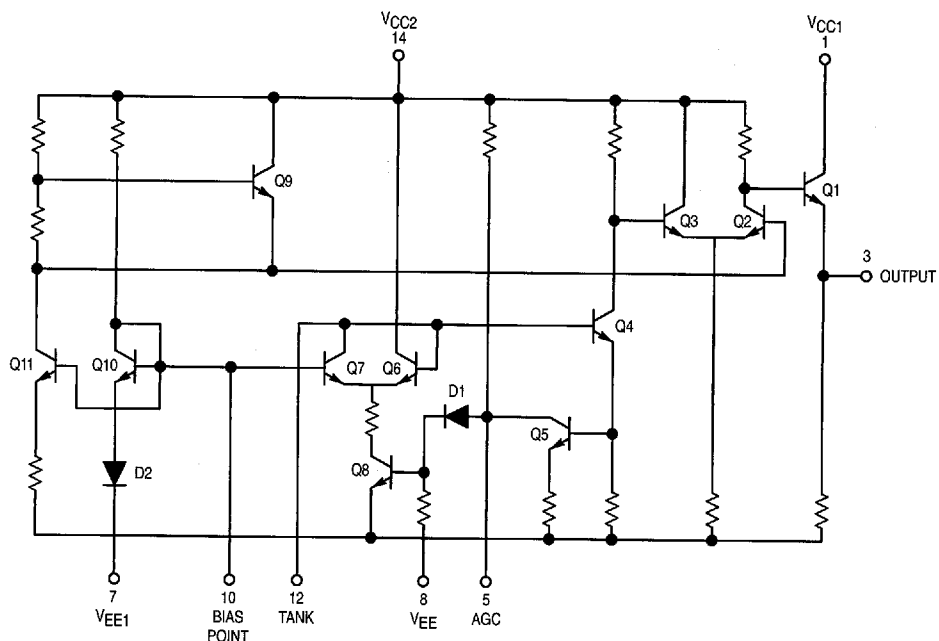


Figure 1. Circuit Schematic

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	(Volts)			mAdc
	V _{IHmax}	V _{ILmin}	V _{CC}	I _L
MC1648				
-30°C	+2.0	+1.5	+5.0	-5.0
+25°C	+1.85	+1.35	+5.0	-5.0
+85°C	+1.7	+1.2	+5.0	-5.0

Note: SOIC "D" package guaranteed -30°C to +70°C only

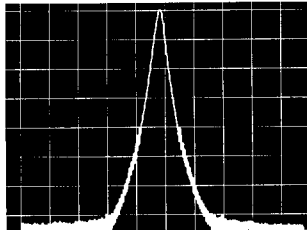
ELECTRICAL CHARACTERISTICS (Supply Voltage = +5.0V)

Symbol	Characteristic	-30°C		+25°C		+85°C		Unit	Condition			
		Min	Max	Min	Max	Min	Max					
I _E	Power Supply Drain Current	—	—	—	41	—	—	mAdc	Inputs and outputs open			
V _{OH}	Logic "1" Output Voltage	3.955	4.185	4.04	4.25	4.11	4.36	Vdc	V _{ILmin} to Pin 12, I _L @ Pin 3			
V _{OL}	Logic "0" Output Voltage	3.16	3.4	3.2	3.43	3.22	3.475	Vdc	V _{IHmax} to Pin 12, I _L @ Pin 3			
V _{BIAS} ¹	Bias Voltage	1.6	1.9	1.45	1.75	1.3	1.6	Vdc	V _{ILmin} to Pin 12			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V _{P-P}	Peak-to-Peak Tank Voltage	—	—	—	—	400	—	—	—	—	mV	See Figure 3
V _{dc}	Output Duty Cycle	—	—	—	—	50	—	—	—	—	%	
f _{max} ²	Oscillation Frequency	—	225	—	200	225	—	—	225	—	MHz	

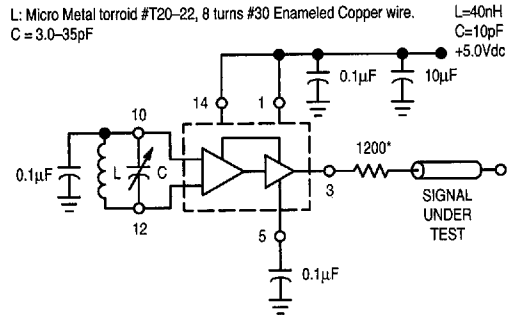
1. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

2. Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.

MC1648



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-075-50 or equivalent.

Figure 2. Spectral Purity of Signal Output for 200MHz Testing

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	(Volts)			mAdc
	V _{IHmax}	V _{ILmin}	V _{EE}	I _L
MC1648				
-30°C	-3.2	-3.7	-5.2	-5.0
+25°C	-3.35	-3.85	-5.2	-5.0
+85°C	-3.5	-4.0	-5.2	-5.0

Note: SOIC "D" package guaranteed -30°C to +70°C only

ELECTRICAL CHARACTERISTICS (Supply Voltage = -5.2V)

Symbol	Characteristic	-30°C		+25°C		+85°C		Unit	Condition			
		Min	Max	Min	Max	Min	Max					
I _E	Power Supply Drain Current	—	—	—	41	—	—	mAdc	Inputs and outputs open			
V _{OH}	Logic "1" Output Voltage	-1.045	-0.815	-0.96	-0.75	-0.89	-0.64	Vdc	V _{ILmin} to Pin 12, I _L @ Pin 3			
V _{OL}	Logic "0" Output Voltage	-1.89	-1.65	-1.85	-1.62	-1.83	-1.575	Vdc	V _{IHmax} to Pin 12, I _L @ Pin 3			
V _{BIAS} ¹	Bias Voltage	-3.6	-3.3	-3.75	-3.45	-3.9	-3.6	Vdc	V _{ILmin} to Pin 12			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V _{P-P}	Peak-to-Peak Tank Voltage	—	—	—	—	400	—	—	—	—	mV	See Figure 3
V _{dc}	Output Duty Cycle	—	—	—	—	50	—	—	—	—	%	
f _{max} ²	Oscillation Frequency	—	225	—	200	225	—	—	225	—	MHz	

1. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.
2. Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.

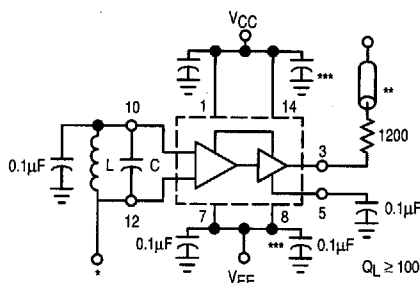
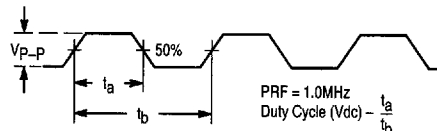


Figure 3. Test Circuit and Waveforms

- * Use high impedance probe (>1.0 Megohm must be used).
- ** The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.
- *** Bypass only that supply opposite ground.



OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least "2" V_{BE} above

V_{EE} ($\approx 1.4V$ for positive supply operation).

When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

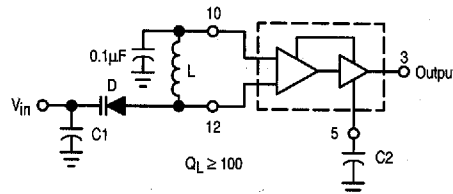
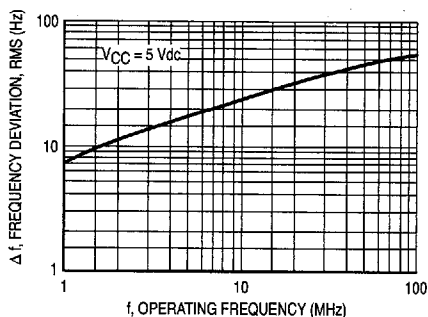


Figure 4. The MC1648 Operating in the Voltage Controlled Mode



Oscillator Tank Components
(Circuit of Figure 4)

f MHz	D	L μH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15

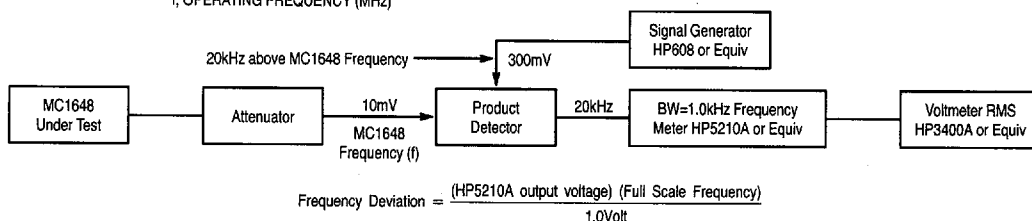


Figure 5. Noise Deviation Test Circuit and Waveform

MC1648

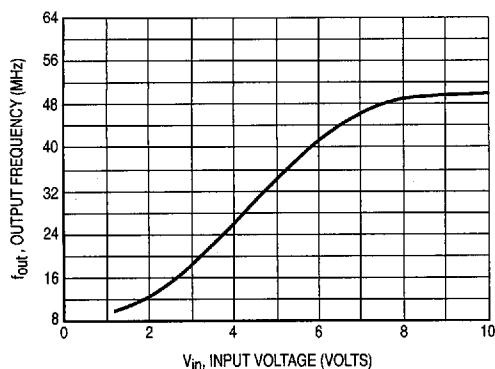
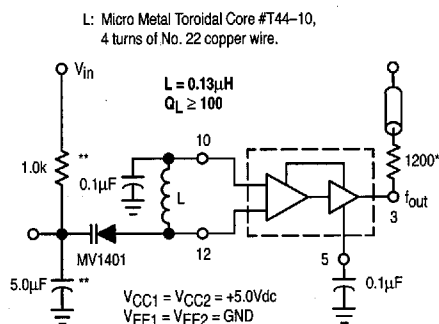


Figure 6



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

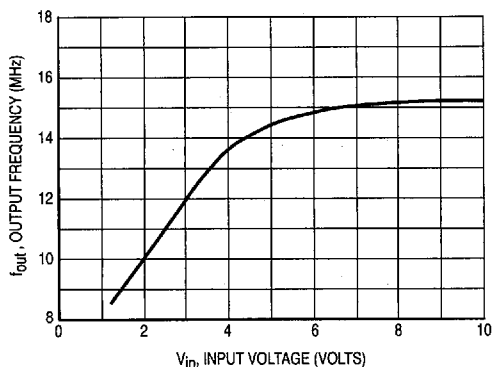
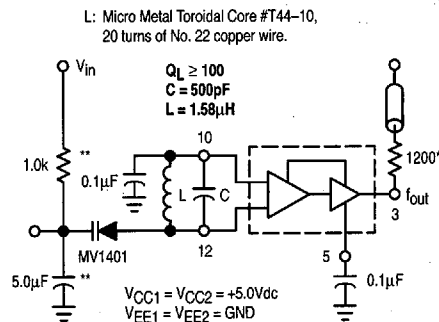


Figure 7



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

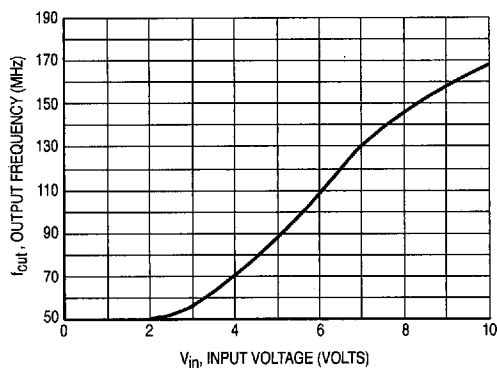
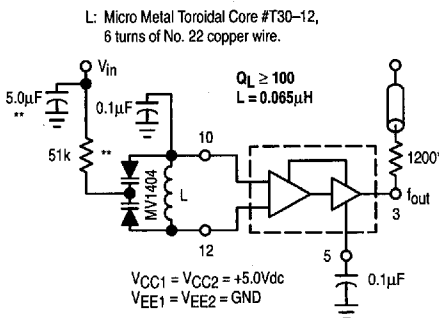


Figure 8



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figure 6, Figure 7 and Figure 8. Figure 6 and Figure 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6.0pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1.0k Ω resistor in Figure 6 and Figure 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51k Ω) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{\max}}{f_{\min}} = \frac{\sqrt{C_D(\max) + C_S}}{\sqrt{C_D(\min) + C_S}}$$

$$\text{where } f_{\min} = \frac{1}{2\pi\sqrt{L(C_D(\max) + C_S)}}$$

CS = shunt capacitance (input plus external capacitance)

CD = varactor capacitance as a function of bias voltage

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1.0MHz and 50MHz a 0.1 μ F capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC to the most positive power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1.0k Ω minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{\text{out}} = Nf_{\text{ref}}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see

Motorola Brochure BR504/D, Electronic Tuning Address Systems, (ETAS).

Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to VEE.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0Vdc supply. To extend the useful range of the device (maintain a square wave output above 175MHz), a resistor is added to the AGC circuit at pin 5 (1.0 kohm minimum).

Figure 12 shows the MC1648 operating from +5.0Vdc and +9.0Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figure 13 and Figure 14 for 100MHz and 10MHz operation. The total collector load includes R in parallel with R_D of L1 and C1 at resonance. The optimum value for R at 100MHz is approximately 850 ohms.

MC1648

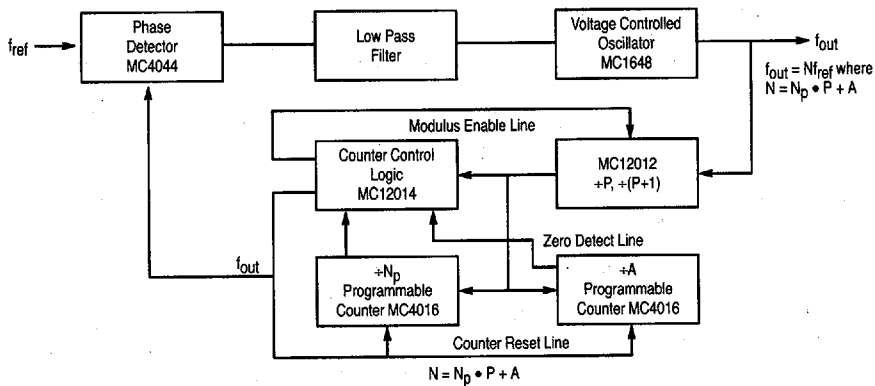


Figure 9. Typical Frequency Synthesizer Application

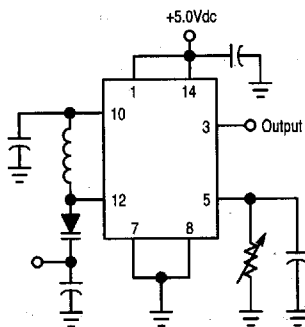


Figure 10. Method of Obtaining a Sine-Wave Output

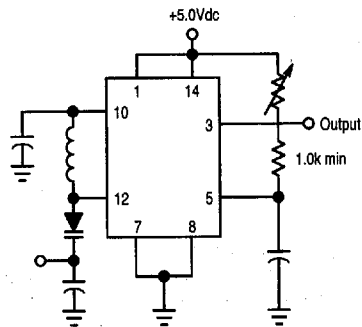


Figure 11. Method of Extending the Useful Range of the MC1648 (Square Wave Output)

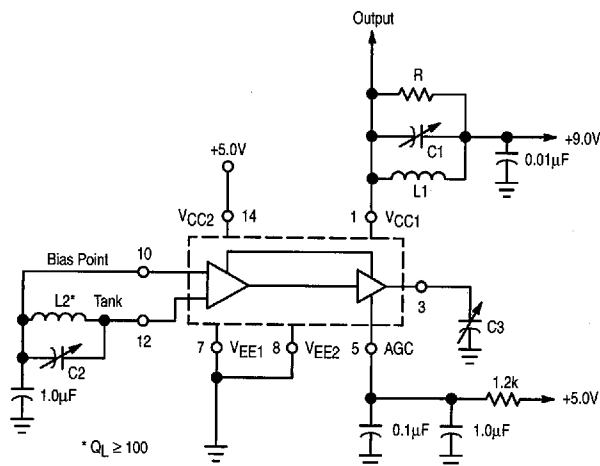
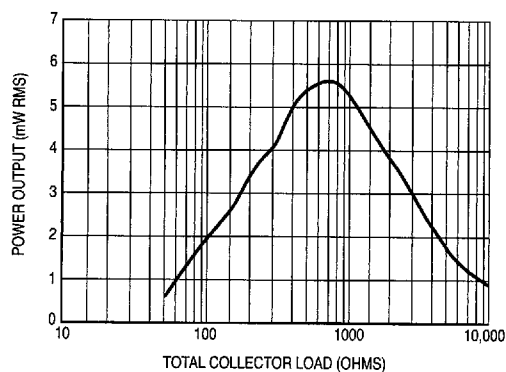
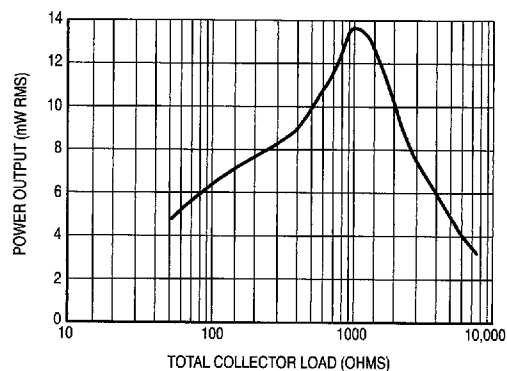


Figure 12. Circuit Used for Collector Output Operation



See test circuit, Figure 12, $f = 100\text{MHz}$
 $C3 = 3.0\text{--}35\text{pF}$
 Collector Tank
 $L1 = 0.22\mu\text{H}$ $C1 = 1.0\text{--}7.0\text{pF}$
 $R = 50\Omega\text{--}10\text{k}\Omega$
 R_p of $L1$ and $C1 = 11\text{k}\Omega$ @ 100MHz Resonance
 Oscillator Tank
 $L2 = 4$ turns #20 AWG 3/16" ID
 $C2 = 1.0\text{--}7.0\text{pF}$

Figure 13. Power Output versus Collector Load



See test circuit, Figure 12, $f = 10\text{MHz}$
 $C3 = 470\text{pF}$
 Collector Tank
 $L1 = 2.7\mu\text{H}$ $C1 = 24\text{--}200\text{pF}$
 $R = 50\Omega\text{--}10\text{k}\Omega$
 R_p of $L1$ and $C1 = 6.8\text{k}\Omega$ @ 10MHz Resonance
 Oscillator Tank
 $L2 = 2.7\mu\text{H}$
 $C2 = 16\text{--}150\text{pF}$

Figure 14. Power Output versus Collector Load

refer to Section 4 for a further discussion.

3.6 EXTERNAL COMPONENTS

There are a few external passive components required in order for the FCG to properly operate. are shown in Figure 3.6. Their recommended values are specified in Table 3.6. All resistor values are $\pm 5\%$ and capacitor values are $\pm 10\%$.

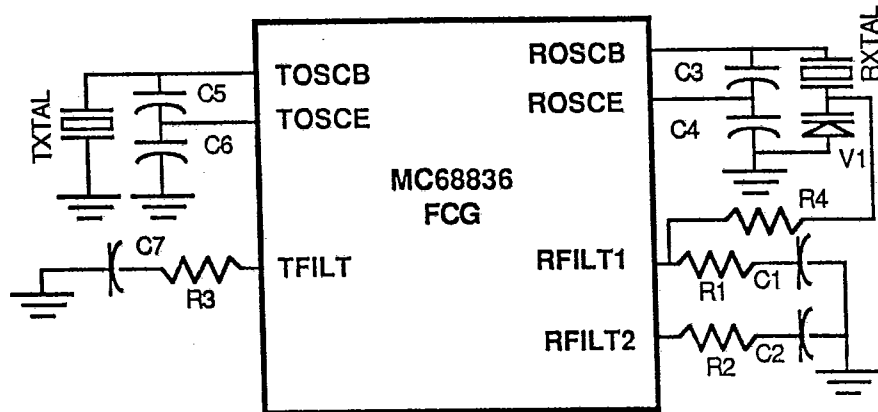


Figure 3.6
External Components

Name	Value	Function
C1	470 pF	Rx main PLL filter
C2	3300 pF	Rx frequency multiplier filter
C3	30 pF	Rx VCXO
C4	30 pF	Rx VCXO
C5	20 pF	Tx oscillator
C6	20 pF	Tx oscillator
C7	3300 pF	Tx frequency multiplier filter
R1	24 k Ω	Rx main PLL filter
R2	470 Ω	Rx frequency multiplier filter
R3	470 Ω	Tx frequency multiplier filter
R4	10k Ω	VCXO Control Signal
V1	MMBV105GL	Varactor Diode

Table 3.6 - Recommended Passive Component Values

3.6.1 Receive Crystal

The receiver requires an external crystal for proper operation. As the receiver crystal oscillator is a VCXO (Voltage Controlled Crystal Oscillator), certain parameters of the crystal must be specified. 3.6.1 indicates the important parameters. None of the parameters is particularly difficult to specify. Motional capacitance and spurious response are not normally specified. Some crystal manufacturers specify the C0/Cm (static capacitance to motional capacitance) ratio to specify pullability. Motional capacitance is relatively high to allow increased pullability.

which vibrate at the applied frequency. When the applied frequency is at a mechanically resonant frequency, the effective series resistance becomes low and the vibration amplitude increases. With high drive or low C_0/C_m ratios (266 is a relatively low C_0/C_m ratio), the mechanical vibrations can become uniform and cause resonances to occur near the desired frequency. If the equivalent series resistance becomes low enough at the spurious resonance, the oscillator may begin operating at that frequency rather than the desired frequency. Typically, spurious responses occur above the desired frequency within a few hundred kHz. The specification below requires that spurious responses be at least 20 dB below the main response. This is a good safe level which will not allow the oscillator to operate at a spurious frequency.

Load capacitance is widely misunderstood so this section provides a brief discussion. Load capacitance is defined as the total effective capacitance presented across the crystal resonator pins. As the load capacitance changes, the resonant frequency of the oscillator network, including the crystal capacitance, changes. Since a crystal resonator has a very large L/C ratio, it dominates the resonant frequency equation. Therefore, relatively large changes in external components result in a small change in the overall resonant frequency. Figure 3.6.1a is a model of the VCXO including internal parasitic capacitances. Figure 3.6.1b shows the transformation of the circuit model to the load capacitance model.

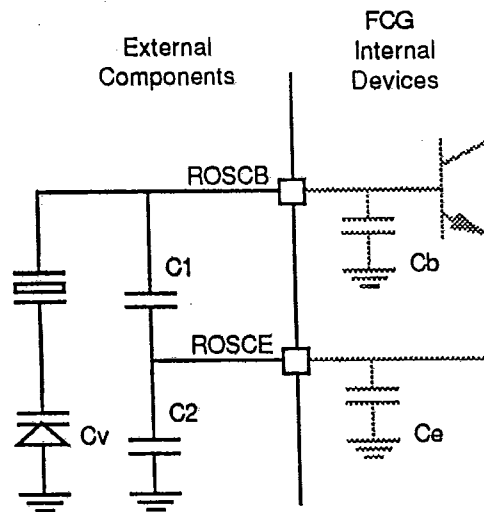


Figure 3.6.1a
VCXO Model

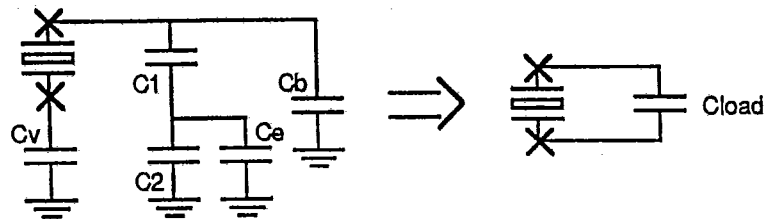


Figure 3.6.1b
Load Capacitance Model

$$C_{load} \approx \frac{C_v (C_1 C_2 + C_1 C_e + C_1 C_b + C_2 C_b)}{C_1 (C_2 + C_e + C_b) + C_2 C_b + C_v (C_1 + C_2 + C_e)}$$

$C_1 = 30 \text{ pF}$
 $C_2 = 30 \text{ pF}$
 $C_v = 12 \text{ pF}$
 $C_b = 7 \text{ pF}$
 $C_e = 7 \text{ pF}$

Substituting values, C_{load} becomes 7.8 pF. For correlation purposes, 10 pF is specified. The manufacturer will load the crystals with 10 pF and measure the resonant frequency. While the crystal is pulled further (per ΔpF) at lower load capacitances, the oscillator becomes more sensitive; variation in capacitance of any component (or stray) can move the resonant frequency out of specification. 10 pF is a good compromise between pullability and sensitivity to capacitor value variations. Note that the MMBV105GL is a 10 pF device when measured at 4V. When the control voltage is at a nominal value, the capacitance is near 12 pF. With the recommended tuning resistor, R4, the varactor can enter conduction at low tuning voltages and have a high value capacitance (shunted by a relatively low value resistor). This provides even more tuning range.

Table 3.6.1 lists the recommended parameters for the receive crystal. Manufacturers have evaluated these specifications and found them to be reasonable.

<u>Parameter</u>	<u>Value</u>	<u>Units</u>
Frequency	20.833333	MHz
Load Capacitance	10	pF
Frequency Tolerance	± 10	PPM
Aging	± 2	PPM/Year
Temperature Stability (0°C to 70°C)	± 15	PPM
Oscillation Mode	Fundamental	

Parameters at 25°C \pm 2°C, drive level = 0.5 mW

Shunt Capacitance (max)	8	pF
Motional Capacitance (min)	30	fF (femtoFarads)
C0/Cm ratio (max)	267	-
Series Resistance (max)	20	Ω
Spurious Responses (max)	> 5dB below main within 500 kHz	

Table 3.6.1
Receive Crystal Specifications

3.6.2 Transmit Crystal

The transmit crystal is simpler in that it is a standard microprocessor crystal. The FDDI specification requires that the transmitter operate at 125MHz \pm 50 PPM so the FCG needs a transmit crystal at 12.5000 MHz with a total frequency tolerance of \pm 50PPM (over time and temperature). To set the crystal oscillation frequency, the load capacitance must be selected.

In this case, as one of the crystal pins is connected to Vss, C_1 is the capacitance that would be measured by a capacitance meter at the TOSCB pin. All stray and pin capacitances should be included in C_1 . Figure 3.6.2 is a simple model of the oscillator and the stray capacitances associated with the pins. Note that a capacitance meter cannot be used to measure the capacitance at this point as there are free-running signals internal to the chip which interfere with the measurement of the meter. Other techniques such as analog network analyzers may be used. The simple model of Figure 3.6.2 is sufficiently accurate for most applications.

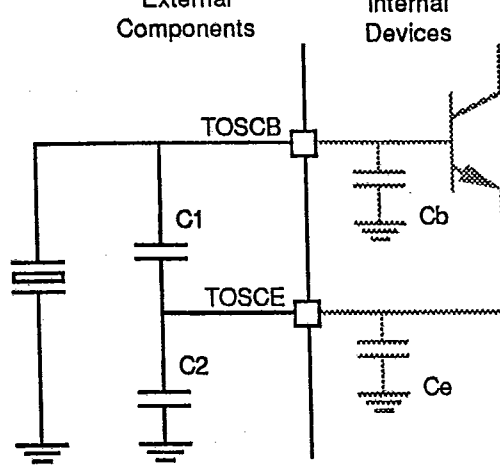


Figure 3.6.2
Transmitter Crystal Oscillator

As an example say C1 and C2 are 20 pF and Ce and Cb are each 7 pF. The equivalent capacitance is 18 pF. As it turns out, these values work just about perfectly for an 18 pF crystal. Experiments in the laboratory have demonstrated proper frequency operation with these values. Table 3.6.2 lists the recommended transmit crystal parameters.

<u>NAME</u>	<u>VALUE</u>	<u>UNITS</u>
Frequency	25.00000	MHz
Load Capacitance	18	pF
Frequency Tolerance	±10	PPM
Aging	±2	PPM/Year
Temperature Stability	±15	PPM
Oscillation Mode	Fundamental	-

Parameters at 25°C ±2°C, drive level = 0.5 mW

Shunt Capacitance (max)	8	pF
Motional Capacitance (typ)	10	fF
Series Resistance (max)	20	Ω
Spurious Responses (max)	> 5dB below main within 500 kHz	

Table 3.6.2
Transmit Crystal Specifications

There are three PLL filters associated with the FCG, one for each PLL. Each filter determines the dynamic characteristics of its PLL. In the case of the two frequency multipliers, the requirements are similar (the divide ratios) so the same filter components are selected. The transmitter loop bandwidth is 60 kHz and the receiver loop bandwidth is 500 kHz when the recommended component values are used. Lock-up time for these PLLs is about 2 μ s.

The clock recovery PLL has different requirements. It is expected to remain stable in a relatively high noise environment so its loop bandwidth is quite low. In this case, the recommended component values result in a loop bandwidth of about 7 kHz. Lock-up time will be in the range of 70 to 100 μ s.

The phase detector gain coefficient (K_{ϕ}) for the three PLLs is about 1.59×10^{-4} A/radian. The VCO gain coefficient (K_V) is about 7.2×10^8 radian/V-sec for the two frequency multiplier PLLs. For the clock recovery PLL, K_V is about 5.2×10^3 radian/V-sec. These coefficients will allow the user to fine-tune PLL performance in a particular application. **Note:** These parameters are not guaranteed but are estimates of what the user will see.

This section describes some applications for the FCG device. Since the FCG can operate as a master or slave, an application of a dual attached station is described. A brief discussion of PC board techniques is also provided.

4.1 DUAL ATTACHED STATION

There are two basic configurations for the FCG: master and slave. In the master mode, it is the clock source. SYMCLK and BYTCLK are generated for use by the rest of the system. When operating as a slave, the FCG uses TCLKIN as the clock source. In both cases, on the receive side, RSCLK is generated by the FCG (in general, the receive clock is asynchronous from the transmit clock.) The FCG automatically switches between master and slave operation. If a signal is present on TCLKIN, its signal will be used as clock data on the TDATA bus into the chip. If TCLKIN is idle, the signal from the on-chip crystal oscillator will be used. Figure 4.1 shows a dual attached station where one FCG is the system clock master and the other is a slave. The slave FCG has its on-chip crystal oscillator disabled and uses TCLKIN as the reference. Note that SYMCLK and BYTCLK are still produced by the slave device, but they are delayed from TCLKIN. In this mode, these signals are not used to clock data in the slave FCG; they should not be used as timing references.

For a large system such as a concentrator where many PHY blocks are implemented, it may be convenient to provide a master clock for the system. In this case, all FCGs would be operated as slaves and all timing would be derived from the distributed system clock.

Figure 4.1 does not show the receive crystal oscillator or the loop filters; they must still be implemented using the recommended components.

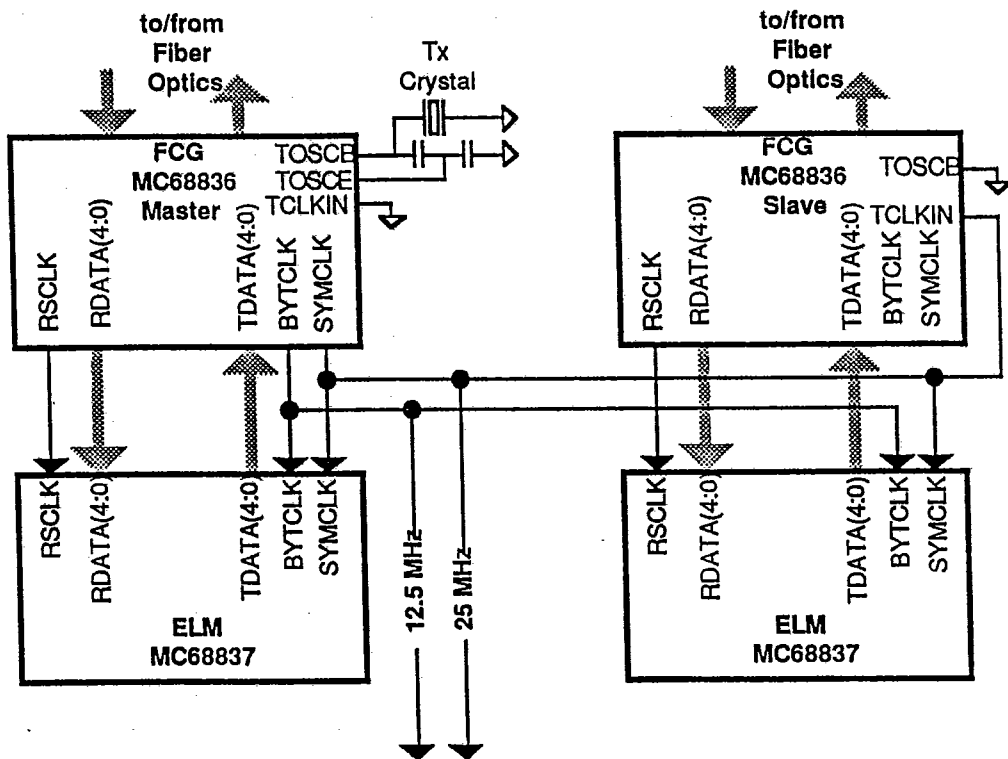


Figure 4.1
Dual Attached Station