P-channel enhancement mode MOS transistor

PHP109

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

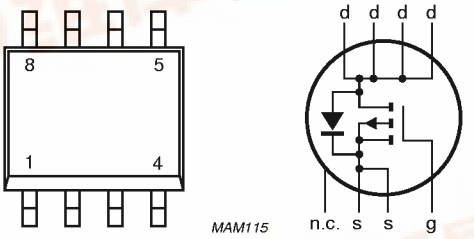

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	–5	A
R_{DSon}	drain-source on-state resistance	I_D = –2.5 A; V_{GS} = –10 V	–	0.09	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–5	A
I_{DM}	peak drain current	note 2	–	–20	A
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W
		T_{amb} = 25 °C; note 3	–	2.7	W
		T_{amb} = 25 °C; note 4	–	1.15	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–3	A
I_{SM}	peak pulsed source current	note 2	–	–12	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

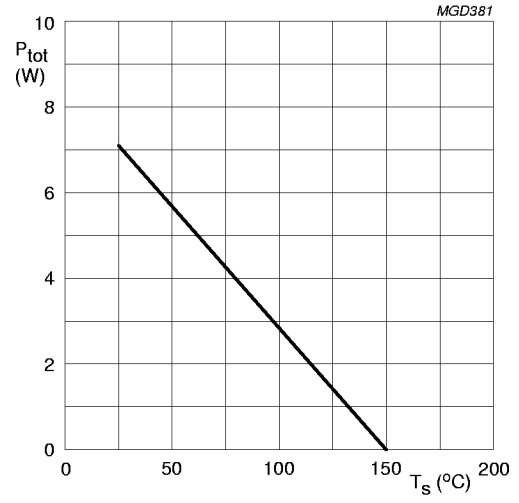
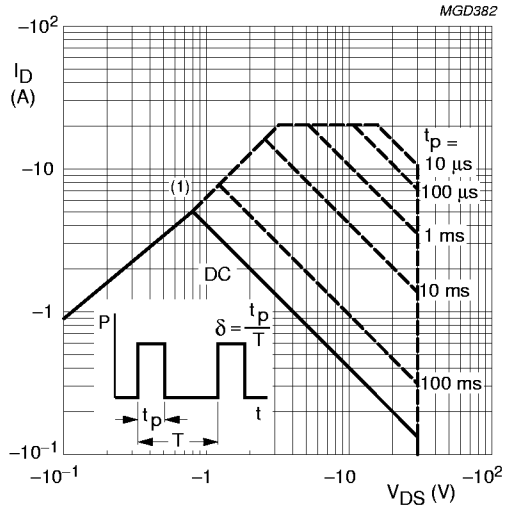


Fig.2 Power derating curve.



δ = 0.01; T_S = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	17.5	K/W

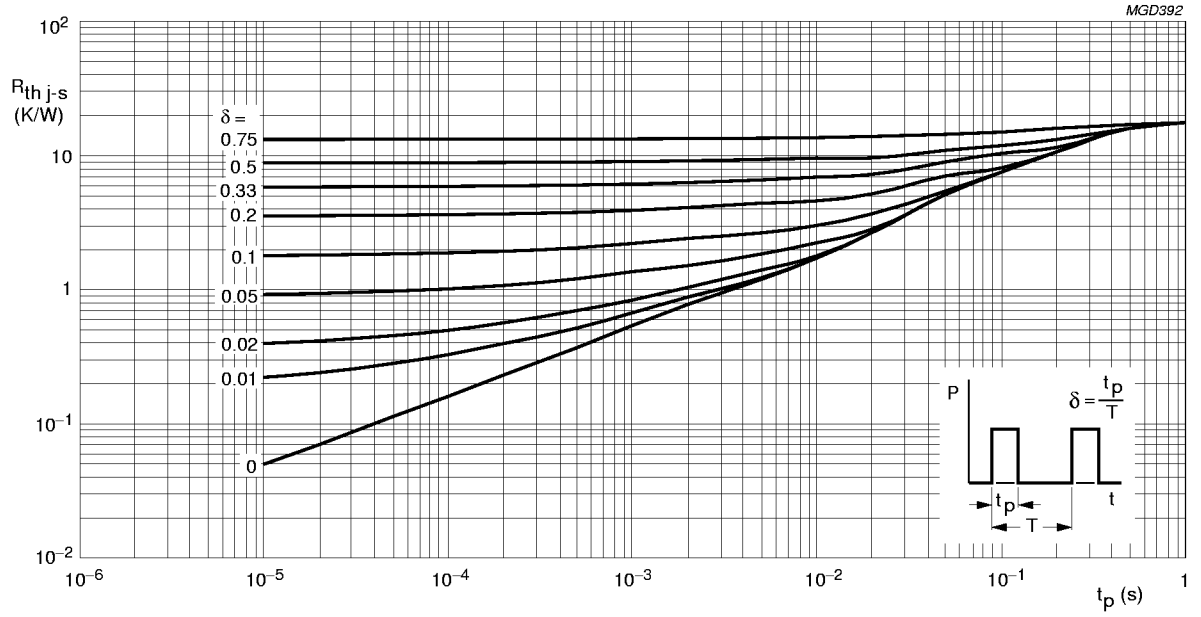
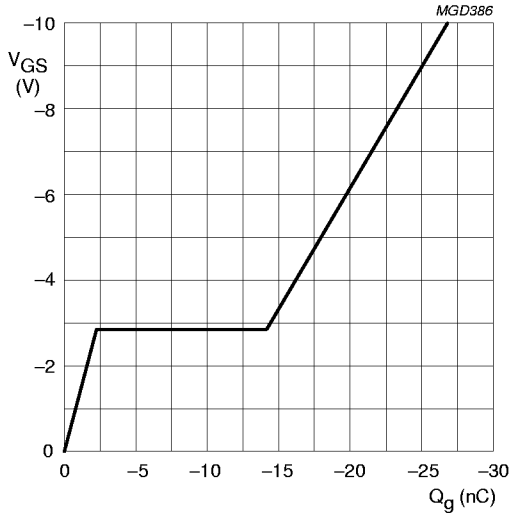


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

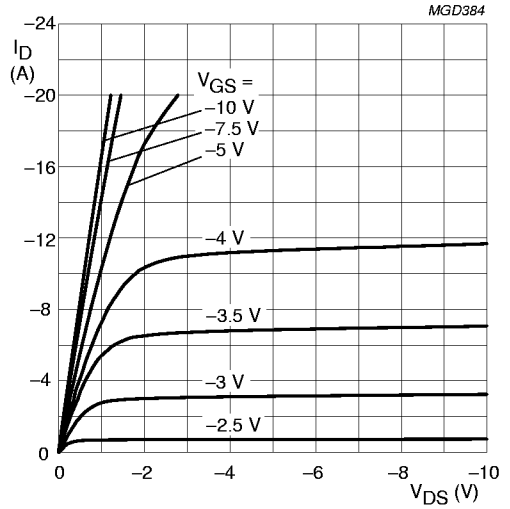
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1.25 A	–	–	0.15	Ω
		V_{GS} = −10 V; I_D = −2.5 A	–	–	0.09	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	825	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	350	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	150	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	30	40	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	3	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	12	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	7	–	ns
t_f	fall time		–	10	–	ns
t_{on}	turn-on switching time		–	17	35	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	60	–	ns
t_r	rise time		–	40	–	ns
t_{off}	turn-off switching time		–	100	200	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	70	–	ns



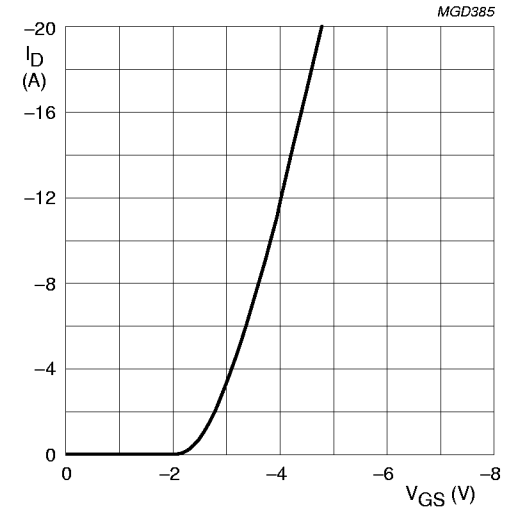
V_{DD} = −15 V; I_D = −2.5 A.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



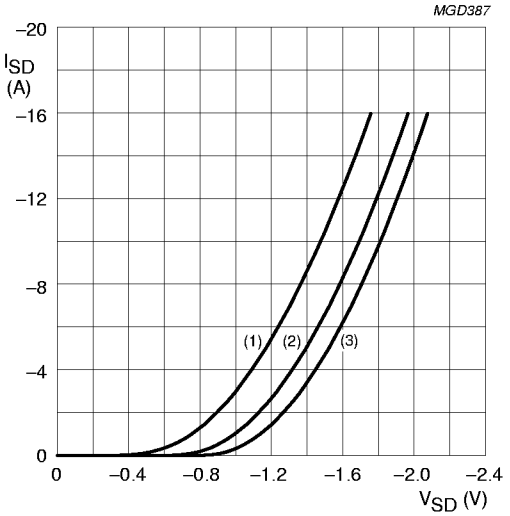
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



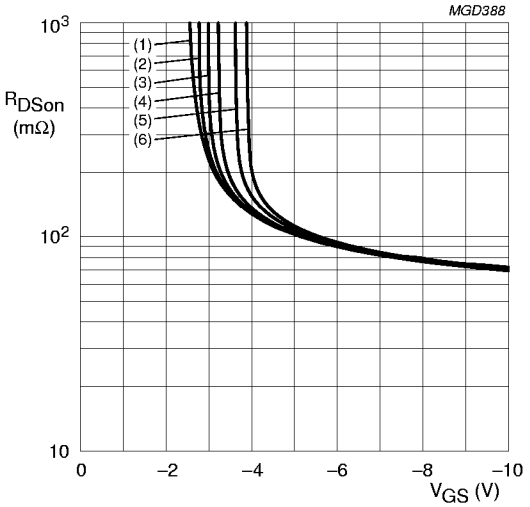
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

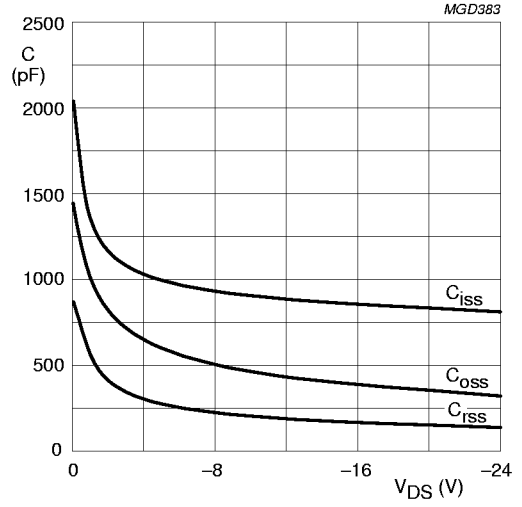
Fig.8 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

(1) I_D = −100 mA.
(2) I_D = −500 mA.
(3) I_D = −1.25 A.
(4) I_D = −2.5 A.
(5) I_D = −5 A.
(6) I_D = −7 A.

Fig.9 Drain source on-state resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

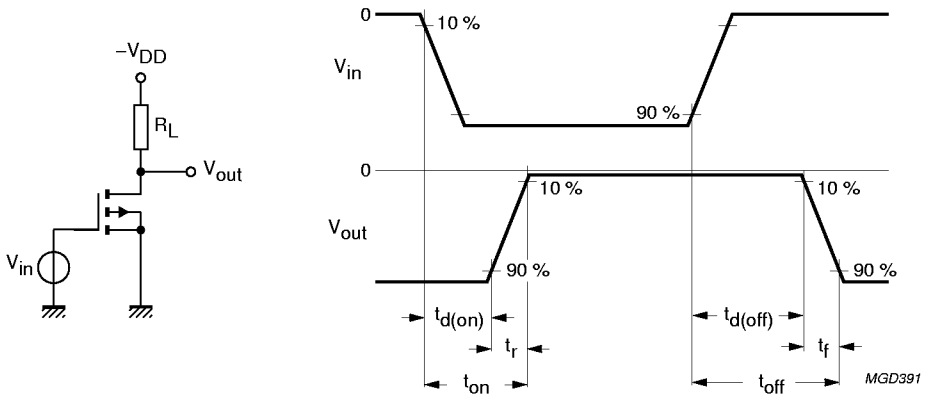
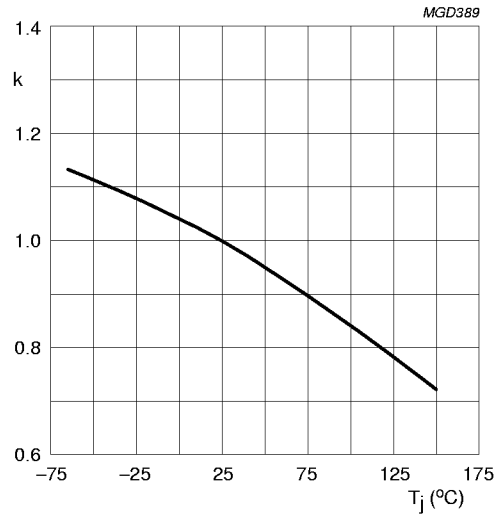


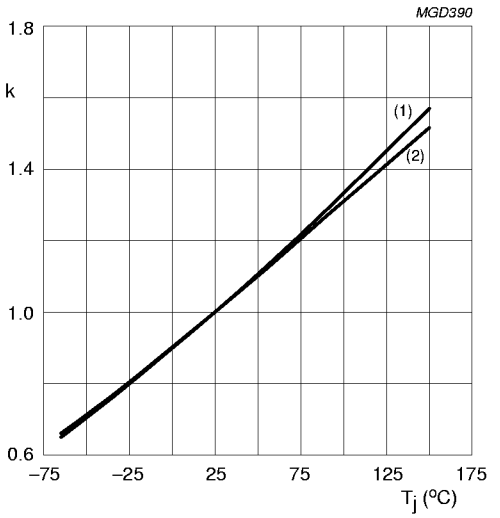
Fig.11 Switching times test circuit and input and output waveforms.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

R_{DSon} at:

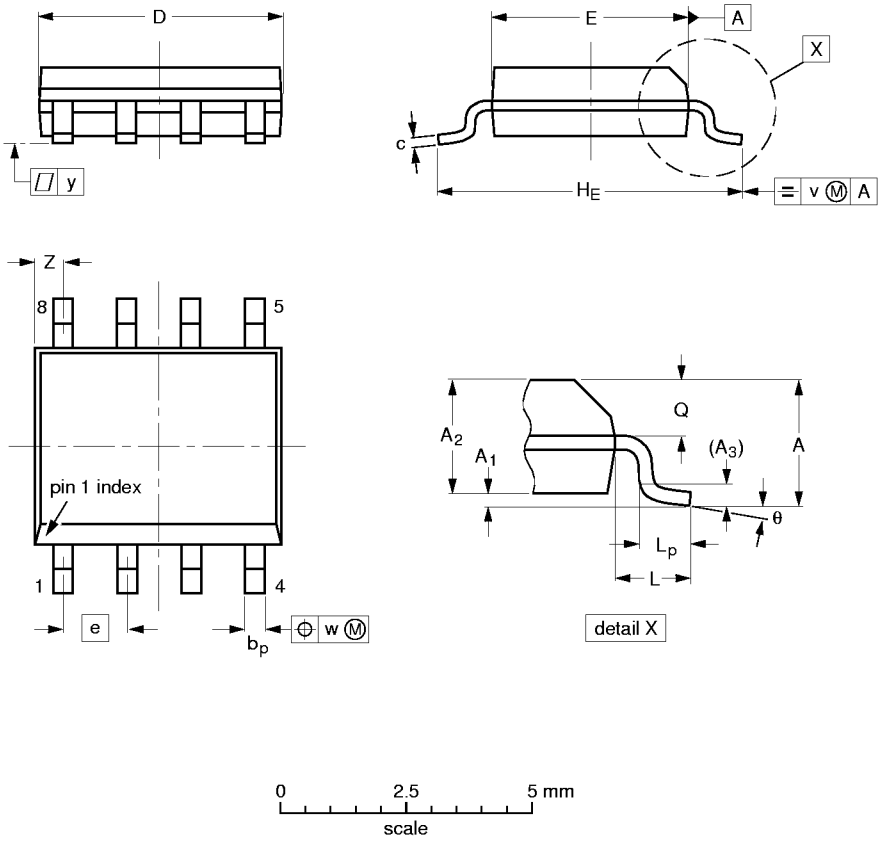
(1) $V_{GS} = -10$ V; $I_D = -2.5$ A.

(2) $V_{GS} = -4.5$ V; $I_D = -1.25$ A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22