



ACS08MS

Radiation Hardened Quad 2-Input AND Gate

July 1998

Features

- QML Qualified Per MIL-PRF-38535 Requirements
- 1.25Micron Radiation Hardened SOS CMOS
- Radiation Environment
 - Latch-up Free Under any Conditions
 - Total Dose 3×10^5 RAD(Si)
 - SEU Immunity $<1 \times 10^{-10}$ Errors/Bit/Day
 - SEU LET Threshold $>100\text{MeV}/(\text{mg}/\text{cm}^2)$
- Input Logic Levels . . . $V_{IL} = (0.3)(V_{CC})$, $V_{IH} = (0.7)(V_{CC})$
- Output Current $\pm 8\text{mA}$ (Min)
- Quiescent Supply Current $100\mu\text{A}$ (Max)
- Propagation Delay 15ns (Max)

Applications

- High Speed Control Circuits
- Sensor Monitoring
- Low Power Designs

Description

The Radiation Hardened ACS08MS is a Quad 2-Input AND Gate. For each gate, a HIGH level on both the A and B inputs results in a HIGH level on the Y output. A LOW level on either the A or B input results in a LOW level on the Y output. All inputs are buffered and the outputs are designed for balanced propagation delay and transition times.

The ACS08MS is fabricated on a CMOS Silicon on Sapphire (SOS) process, which provides an immunity to Single Event Latch-up and the capability of highly reliable performance in any radiation environment. These devices offer significant power reduction and faster performance when compared to ALSTTL types.

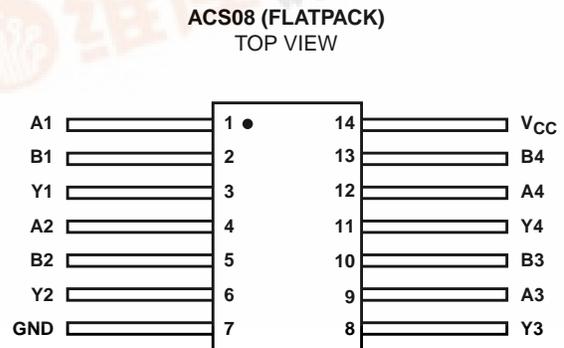
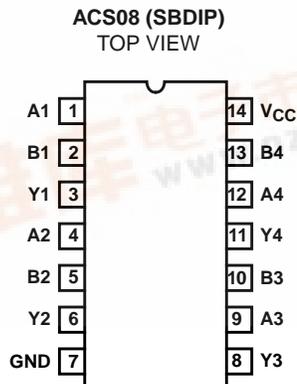
Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACS08 are contained in SMD 5962-95651. A "hot-link" is provided on our homepage with instructions for downloading. www.intersil.com/data/sm/index.asp

Ordering Information

ORDERING NUMBER	INTERNAL MARKETING NUMBER	TEMP. RANGE (°C)	PACKAGE	DESIGNATOR
5962F9565101VCC	ACS08DMSR	-55 to 125	14 Ld SBDIP	CDIP2-T14
ACS08D/SAMPLE	ACS08D/SAMPLE	25	14 Ld SBDIP	CDIP2-T14
5962F9565101VXC	ACS08KMSR	-55 to 125	14 Ld Flatpack	CDFP4-F14
ACS08K/SAMPLE	ACS08K/SAMPLE	25	14 Ld Flatpack	CDFP4-F14
5962F9565101V9A	ACS08HMSR	25	Die	N/A

Pinouts



ACS08MS

Die Characteristics

DIE DIMENSIONS:

Size: 2390 μ m x 2390 μ m (94 mils x 94 mils)
Thickness: 525 μ m \pm 25 μ m (20.6 mils \pm 1 mil)
Bond Pad: 110 μ m x 110 μ m (4.3 mils x 4.3 mils)

METALLIZATION: Al

Metal 1 Thickness: 0.7 μ m \pm 0.1 μ m
Metal 2 Thickness: 1.0 μ m \pm 0.1 μ m

SUBSTRATE POTENTIAL:

Unbiased Insulator

PASSIVATION

Type: Phosphorous Silicon Glass (PSG)
Thickness: 1.30 μ m \pm 0.15 μ m

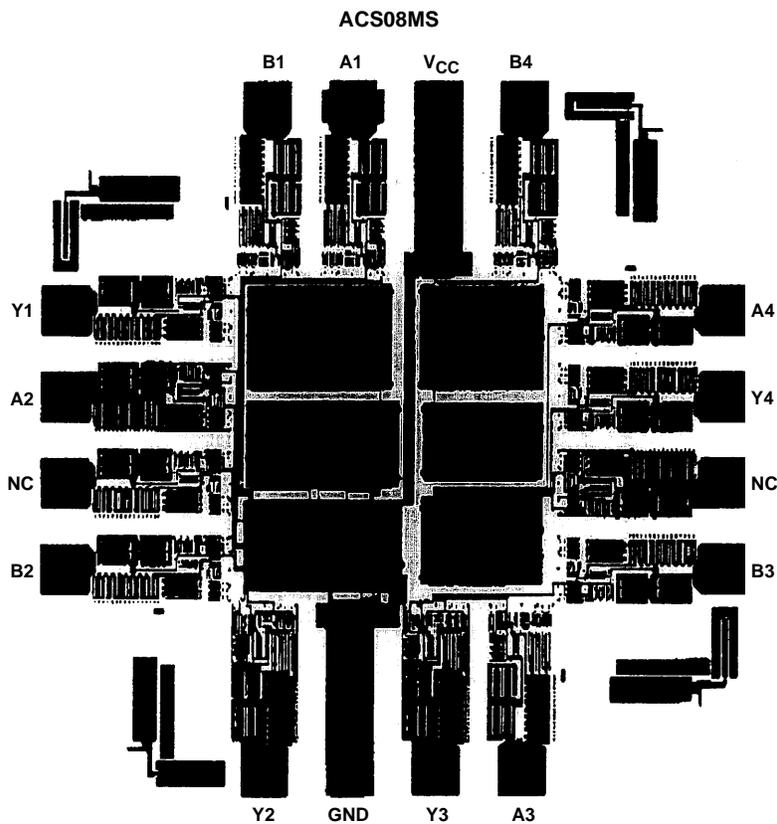
SPECIAL INSTRUCTIONS:

Bond V_{CC} First

ADDITIONAL INFORMATION:

Worst Case Density: <2.0 x 10⁵ A/cm²
Transistor Count: 176

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029