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WINBOND
LPC I/O
W83697HF

Revision: 2.0 Date: April 14, 2005

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1. GENERAL DESCRIPTION

The W83697HF is evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (Low Pin Count) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. With this additional freedom, we can implement more devices on a single chip as demonstrated in W83697HF's integration of Game Port and MIDI Port. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83697HF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83697HF greatly reduces the number of components required for interfacing with floppy disk drives. The W83697HF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s.

The W83697HF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps which support higher speed modems. In addition, the W83697HF provides IR functions: IrDA 1.0 (SIR for 1.152K bps) and TV remote IR (Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83697HF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The W83697HF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode (VCC is off).

The W83697HF is made to fully comply with Microsoft© PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.

The W83697HF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, They are very important for a entertainment or consumer computer.

The W83697HF provides Flash ROM interface. That can support up to 4M legacy flash ROM.

The W83697HF support hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly. Moreover, W83697HF support the Smart Fan control system, including the thermal Cruise™" and speed Cruise™" functions. Smart Fan can make system more stable and user friendly.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Include all the features of Winbond I/O W83877TF
- Integrate Hardware Monitor functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and under run conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Win95/98 driver

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - --- 5, 6, 7 or 8-bit characters
  - --- Even, odd or no parity bit generation/detection
  - --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - --- Loop-back controls for communications link fault isolation

--- Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR with Wake-Up function.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axes (X, Y) and two buttons (S1,S2) controllers

MIDI Port

- The baud rate is 31.25 K baud rate
- 16-byte input FIFO
- 16-byte output FIFO

Flash ROM Interface

- Support up to 4M flash ROM

General Purpose I/O Ports

- 48 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, watch dog timer output, power LED output, infrared I/O pins, suspend LED output, Beep output
- Functional in power down mode

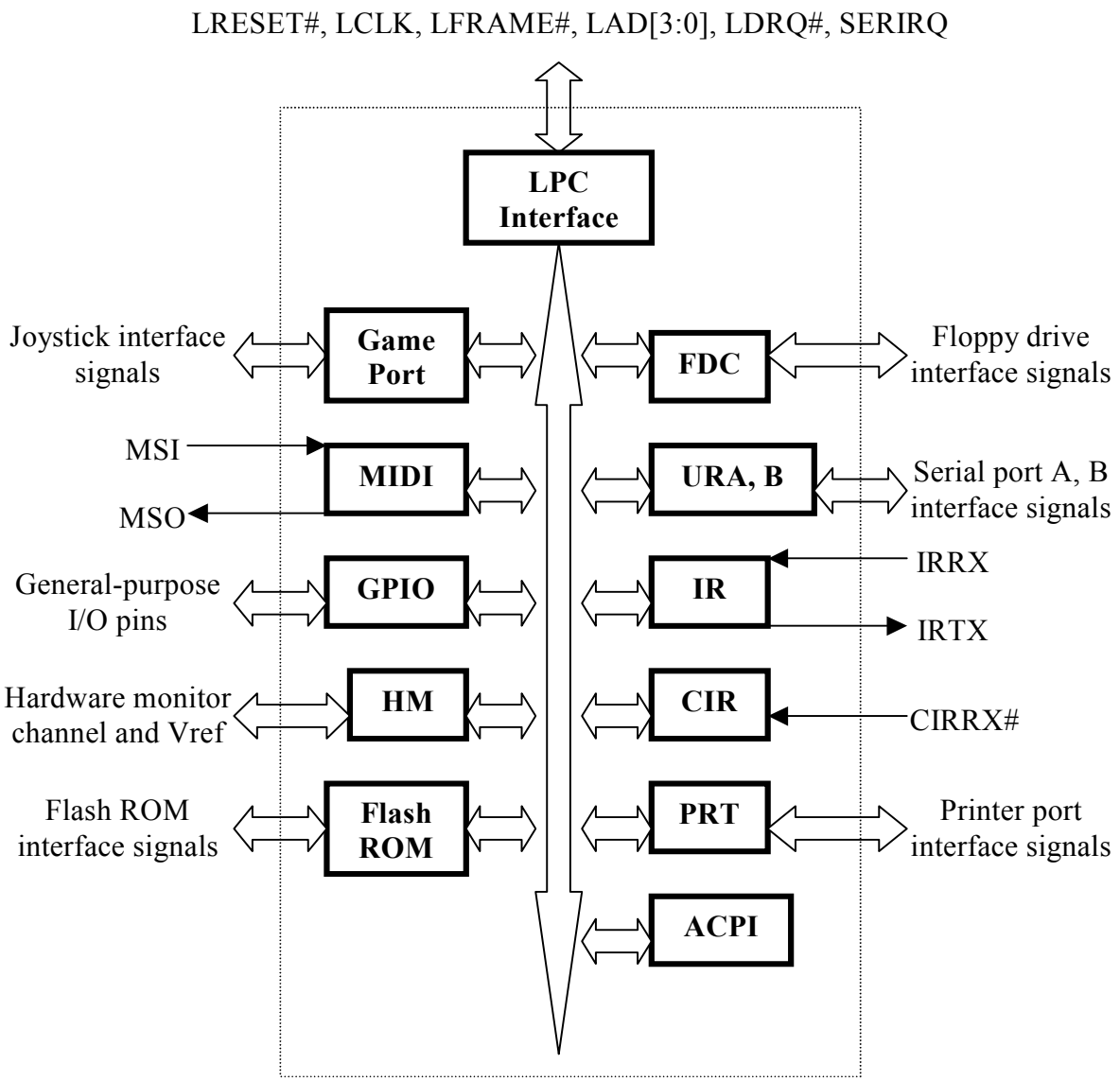
Hardware Monitor Functions

- Smart fan control system, support thermal Cruise™ and speed Cruise™
- 2 thermal inputs from optionally remote thermistors or 2N3904 transistors or Pentium™ II/III thermal diode output
- 6 positive voltage inputs (typical for +12V, -12V, +5V, -5V, +3.3V, Vcore)
- 2 intrinsic voltage monitoring (typical for Vbat, +5VSB)
- 2 fan speed monitoring inputs
- 2 fan speed control
- Build in Case open detection circuit
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points for all monitored items
- Over temperature indicate output
- Automatic Power On voltage detection Beep
- Issue SMI#, IRQ, OVT# to activate system protection
- Winbond Hardware Doctor™ Support
- Intel LDCM™ / Acer ADM™ compatible

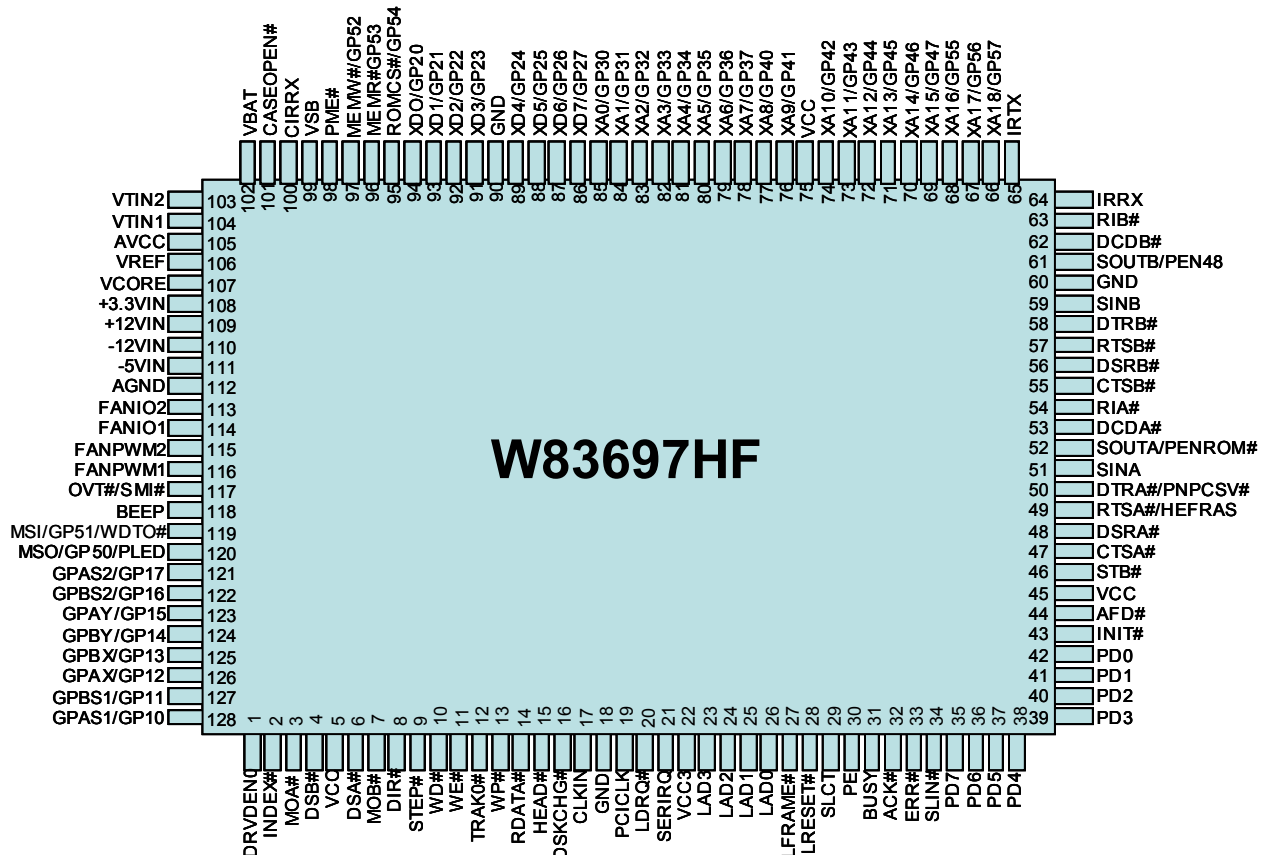
Package

- 128-pin PQFP

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PIN DESCRIPTION

Note: Please refer to Section 10.2 DC CHARACTERISTICS for details

PIN DESCRIPTION	
I/O_{8t}	TTL level bi-directional pin with 8mA source-sink capability
I/O_{12t}	TTL level bi-directional pin with 12mA source-sink capability
I/O_{24t}	TTL level bi-directional pin with 24 mA source-sink capability
I/O_{12tp3}	3.3V TTL level bi-directional pin with 12mA source-sink capability
I/O_{12ts}	TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability
I/O_{24ts}	TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/O_{24tsp3}	3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/OD_{12t}	TTL level bi-directional pin and open-drain output with 12mA sink capability
I/OD_{24t}	TTL level bi-directional pin and open-drain output with 24mA sink capability
I/OD_{24c}	CMOS level bi-directional pin and open-drain output with 24mA sink capability
I/OD_{24a}	Bi-directional pin with analog input and open-drain output with 24mA sink capability
I/OD_{12ts}	TTL level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD_{24ts}	TTL level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD_{12cs}	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD_{16cs}	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD_{24cs}	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD_{12csd}	CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open-drain output with 12mA sink capability
I/OD_{12csu}	CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open-drain output with 12mA sink capability
O_4	Output pin with 4 mA source-sink capability
O_8	Output pin with 8 mA source-sink capability
O_{12}	Output pin with 12 mA source-sink capability
O_{16}	Output pin with 16 mA source-sink capability
O_{24}	Output pin with 24 mA source-sink capability
O_{12p3}	3.3V output pin with 12 mA source-sink capability
O_{24p3}	3.3V output pin with 24 mA source-sink capability
OD_8	Open-drain output pin with 8 mA sink capability
OD_{12}	Open-drain output pin with 12 mA sink capability
OD_{24}	Open-drain output pin with 24 mA sink capability
OD_{12p3}	3.3V open-drain output pin with 12 mA sink capability

PIN DESCRIPTION	
IN_t	TTL level input pin
IN_{tp3}	3.3V TTL level input pin
IN_{td}	TTL level input pin with internal pull down resistor
IN_{tu}	TTL level input pin with internal pull up resistor
IN_{ts}	TTL level Schmitt-trigger input pin
IN_{tsp3}	3.3V TTL level Schmitt-trigger input pin
IN_c	CMOS level input pin
IN_{cu}	CMOS level input pin with internal pull up resistor
IN_{cd}	CMOS level input pin with internal pull down resistor
IN_{cs}	CMOS level Schmitt-trigger input pin
IN_{csu}	CMOS level Schmitt-trigger input pin with internal pull up resistor

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	17	IN_{tp3}	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	98	OD_{12p3}	Generated PME event.
PCICLK	19	IN_{tsp3}	PCI clock 33 MHz input.
LDRQ#	20	O_{12p3}	Encoded DMA Request signal.
SERIRQ	21	I/O_{12tp3}	Serial IRQ input/Output.
LAD[3:0]	23-26	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	27	IN_{tsp3}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	28	IN_{tsp3}	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	2	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	3	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSB#	4	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
MOB#	7	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	12	IN_{csu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	13	IN_{csu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	14	IN_{csu}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
HEAD#	15	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	16	IN_{csu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

5.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	29	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC.
WE2#			EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	30	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WD2#		OD_{12}	EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC.
			EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.
BUSY	31	IN_{t}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
MOB2#		OD_{12}	EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC.
			EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
ACK#	32	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSB2#		OD_{12}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC. EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
ERR#	33	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
HEAD2#		OD_{12}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD#pin of FDC. EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.
SLIN#	34	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STEP2#		OD_{12}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
INIT#	43	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DIR2#		OD_{12}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
AFD#	44	OD_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DRVDEN0		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
STB#	46	OD_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INDEX2#		IN_{ts}	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: TRAK02#
TRAK02#		IN_{ts}	This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: WP2#
		IN_{ts}	This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: RDATA2#
RDATA2#		IN_{ts}	This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSKCHG2#		In_{ts}	EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD5	37	I/O_{12ts} - -	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6 MOA2#	36	I/O_{12ts} - OD_{12}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD7 DSA2#	35	I/O_{12ts} - OD_{12}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

5.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	47 55	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	48 56	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	49	O_8 IN_{cd}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
RTSB#	57	O_8	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
DTRA# PNPCSV#	50	O_8 IN_{cd}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
DTRB#	58	O_8	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	51 59	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENROM#	52	O_8 IN_{cd}	UART A Serial Output. It is used to transmit serial data out to the communication link. During power on reset , this pin is pulled down internally and is defined as PENROM#, which provides the power on value for CR24 bit 1. A 4.7kΩ is recommended if intends to pull up .
SOUTB PEN48	61	O_8 IN_{cd}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
DCDA# DCDB#	53 62	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	54 63	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

5.5 Infrared Port

SYMBOL	PIN	I/O	FUNCTION
IRRX	64	IN_{ts}	Alternate Function Input: Infrared Receiver input. General purpose I/O port 3 bit 6.
IRTX	65	O_{12}	Alternate Function Output: Infrared Transmitter Output. General purpose I/O port 3 bit 7.
CIRRX#	100	IN_t	Consumer IR receiving input. This pin can Wake-Up system from $S5_{cold}$.

5.6 Flash ROM Interface

SYMBOL	PIN	I/O	FUNCTION
XA18-XA16 GP57-GP55	66-68	O_{12} I/OD_{12t}	Flash ROM interface Address[18:16] General purpose I/O port 5 bit7-5
XA15-XA10 GP47-GP42	69-74	O_{12} I/OD_{12t}	Flash ROM interface Address[15:10] General purpose I/O port 4 bit7-2
XA9-XA8 GP41-GP40	76-77	O_{12} I/OD_{12t}	Flash ROM interface Address[9:8] General purpose I/O port 4 bit1-0
XA7-XA0 GP37-GP30	78-85	O_{12} I/OD_{12t}	Flash ROM interface Address[7:0] General purpose I/O port 3 bit7-0
XD7-XD4 GP27-GP24	86-89	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus[7:4] General purpose I/O port 2 bit7-4
XD3-XD0 GP23-GP20	91-94	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus [3:0] General purpose I/O port 2 bit3-0
ROMCS# GP54	95	O_{12} I/OD_{12t}	Flash ROM interface Chip Select General purpose I/O port 5 bit4
MEMR# GP53	96	O_{12} I/OD_{12t}	Flash ROM interface Memory Read Enable General purpose I/O port 5 bit3
MEMW# GP52	97	O_{12} I/OD_{12t}	Flash ROM interface Memory Write Enable General purpose I/O port 5 bit2

5.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	FUNCTION
CASEOPEN#	101	IN_t	CASE OPEN. An active low signal from an external device when case is opened.
VBAT	102	Power	Battery Voltage Input
VTIN2	103	AIN	Temperature sensor 2 input. It is used for CPU temperature detect.
VTIN1	104	AIN	Temperature sensor 1 input. It is used for system temperature detect.
VREF	106	AOUT	Reference Voltage Output.
VCORE	107	AIN	0V to 4.096V FSR Analog Inputs.
+3.3VIN	108	AIN	0V to 4.096V FSR Analog Inputs.
+12VIN	109	AIN	0V to 4.096V FSR Analog Inputs.
-12VIN	110	AIN	0V to 4.096V FSR Analog Inputs.
-5VIN	111	AIN	0V to 4.096V FSR Analog Inputs.
FANIO[2:1]	113-114	I/O_{12ts}	0V to +5V amplitude fan tachometer input. Alternate Function: Fan on-off control output. These multifunctional pins can be programmable input or output.
FANPWM[2:1]	115-116	O_{12}	Fan speed control. Use the Pulse Width Modulation (**PWM**) knowledge to control the Fan's RPM.
OVT# / SMI#	117	OD_{24} OD_{24}	Over temperature Shutdown Output. It indicated the VTIN1 or VTIN2 is over temperature limit. System Management Interrupt.
BEEP	118	OD_8	Beep function for hardware monitor. This pin is low after system reset.

5.8 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
MSI	119	INt	MIDI serial data input .
GP51		I/OD_{12t}	General purpose I/O port 5 bit 1.
WDTO#		O_{12}	Alternate Function : Watch dog timer output.
MSO	120	O_{12}	MIDI serial data output.
GP50		I/OD_{12t}	General purpose I/O port 5 bit 0.
PLED		O_{12}	Alternate Function Output(Default) Power LED output, this signal is low after system reset.
GPAS2	121	INcsu	Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default)
GP17		I/OD_{12csu}	General purpose I/O port 1 bit 7.
GPBS2	122	INcsu	Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default)
GP16		I/OD_{12csu}	General purpose I/O port 1 bit 6.
GPAY	123	I/OD_{12cs}	Joystick I timer pin. this pin connect to Y positioning variable resistors for the Joystick. (Default)
GP15		I/OD_{12cs}	General purpose I/O port 1 bit 5.
GPBY	124	I/OD_{12cs}	Joystick II timer pin. this pin connect to Y positioning variable resistors for the Joystick. (Default)
GP14		I/OD_{12cs}	General purpose I/O port 1 bit 4.
GPBX	125	I/OD_{12cs}	Joystick II timer pin. this pin connect to X positioning variable resistors for the Joystick. (Default)
GP13		I/OD_{12cs}	General purpose I/O port 1 bit 3.
GPAX	126	I/OD_{12cs}	Joystick I timer pin. this pin connect to X positioning variable resistors for the Joystick. (Default)
GP12		I/OD_{12cs}	General purpose I/O port 1 bit 2.
GPBS1	127	INcsu	Active-low, Joystick II switch input 1. This pin has an internal pull-up resistor. (Default)
GP11		I/OD_{12csu}	General purpose I/O port 1 bit 1.
GPAS1	128	INcsu	Active-low, Joystick I switch input 1. This pin has an internal pull-up resistor. (Default)
GP10		I/OD_{12csu}	General purpose I/O port 1 bit 0.

5.9 Power Pins

SYMBOL	PIN	FUNCTION
VCC	5, 45, 75,	+5V power supply for the digital circuitry.
VSB	99	+5V stand-by power supply for the digital circuitry.
VCC3V	22	+3.3V power supply for driving 3V on host interface.
AVCC	105	Analog VCC input. Internally supplier to all analog circuitry.
AGND	112	Internally connected to all analog circuitry. The ground reference for all analog inputs.
GND	18, 60, 90,	Ground.

6. HARDWARE MONITOR

6.1 General Description

The W83697HF can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stable and properly. W83697HF provides LPC interface to access hardware .An 8-bit analog-to-digital converter (ADC) was built inside W83697HF. The W83697HF can simultaneously monitor 7 analog voltage inputs, 2 fan tachometer inputs, 2 remote temperature, one case-open detection signal. The remote temperature sensing can be performed by thermistors, or 2N3904 NPN-type transistors, or directly from Intel™ Deschutes CPU thermal diode output. Also the W83697HF provides: 2 PWM (pulse width modulation) outputs for the fan speed control; beep tone output for warning; SMI#(through serial IRQ), OVT#, GPO# signals for system protection events.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, or Intel™ LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and maskable interrupts. An optional beep tone could be used as warning signal when the monitored parameters is out of the preset range.

6.2 Access Interface

The W83697HF provides two interface for microprocessor to read/write hardware monitor internal registers.

6.2.1 LPC interface

The first interface uses LPC Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The other higher bits of these ports is set by W83697HF itself. The general decoded address is set to port 295h and port 296h. These two ports are described as following:

Port 295h: Index port.

Port 296h: Data port.

The register structure is showed as the Figure 9.1

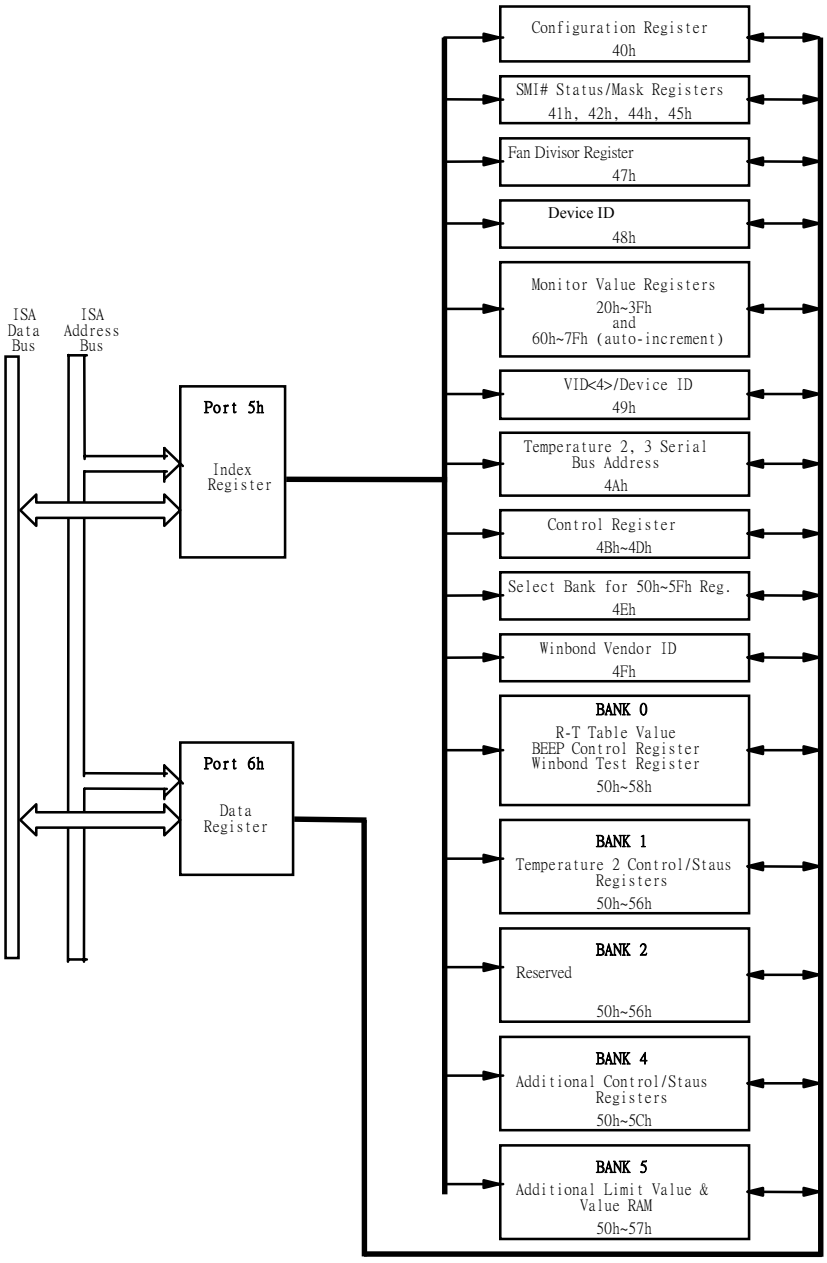
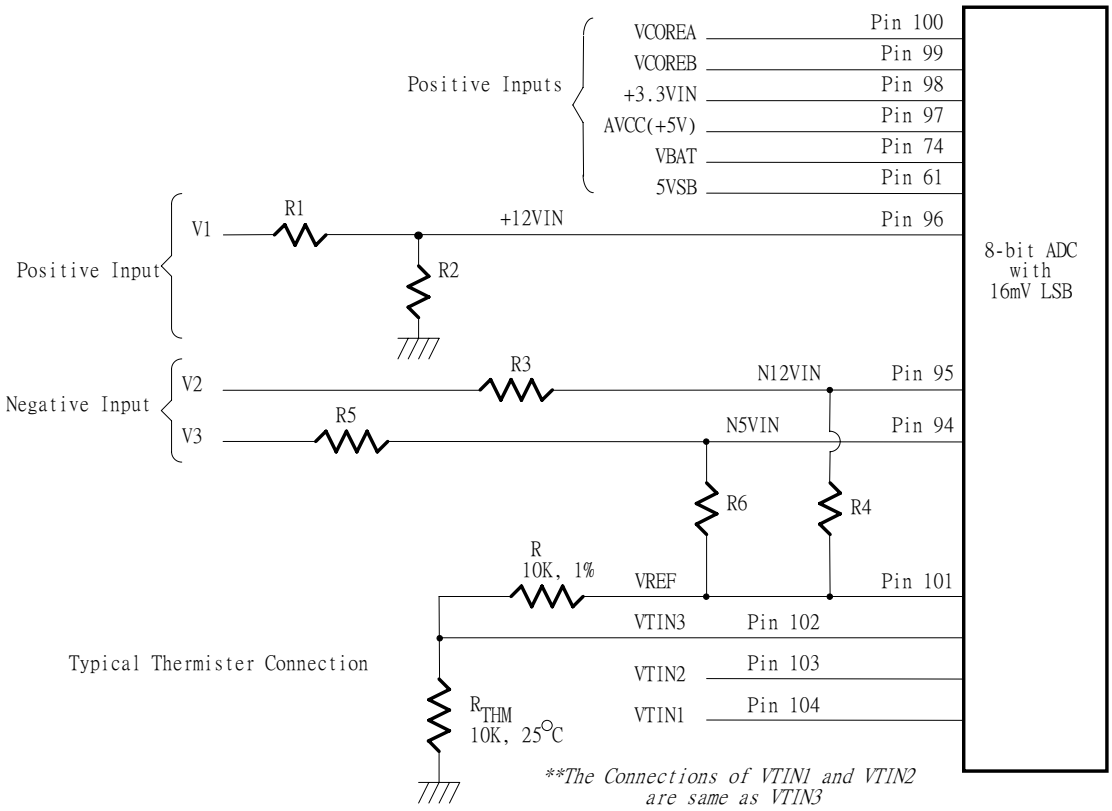


Figure 9.1 : ISA interface access diagram

6.3 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage, +3.3V, battery and 5VSB voltage can directly connected to these analog inputs. The +12V,-12V and -5V voltage inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 9.2 shows.



6.3.1 Monitor over 4.096V voltage

The input voltage +12VIN can be expressed as following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN can be subject to less than 4.096V for the maximun input range of the 8-bit ADC. The Pin 97 is connected to the power supply VCC with +5V. There are two functions in this pin with 5V. The first function is to supply internal analog power in the W83697HF and the second function is that this voltage with 5V is connected to internal serial resistors to monitor the +5V voltage. The value of two serial resistors are 34K ohms and 50K ohms so that input voltage to ADC is 2.98V which is less than 4.096V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{50K\Omega}{50K\Omega + 34K\Omega} \cong 2.98V$$

where VCC is set to 5V.

The Pin 61 is connected to 5VSB voltage. W83697HF monitors this voltage and the internal two serial resistors are 17K Ω and 33K Ω so that input voltage to ADC is 3.3V which less than 4.096V of ADC maximum input voltage.

6.3.2 Monitor negative voltage

The negative voltage should be connected two series resistors and a positive voltage VREF (is equal to 3.6V). In the Figure 9.2, the voltage V2 and V3 are two negative voltage which they are -12V and -5V respectively. The voltage V2 is connected to two serial resistors then is connected to another terminal VREF which is positive voltage. So as that the voltage node N12VIN can be obtain a posedge voltage if the scales of the two serial resirtors are carefully selected. It is recommanded from Winbond that the scale of two serial resistors are R3=232K ohms and R4=56K ohm. The input voltage of node N12VIN can be calculated by following equation.

$$N12VIN = (VREF + |V_2|) \times (\frac{232K\Omega}{232K\Omega + 56K\Omega}) + V_2$$

where VREF is equal 3.6V.

If the V2 is equal to -12V then the voltage is equal to 0.567V and the converted hexdecimal data is set to 35h by the 8-bit ADC with 16mV-LSB.This monitored value should be converted to the real negative votage and the express equation is shown as follows.

$$V_2 = \frac{N12VIN - VREF \times \beta}{1 - \beta}$$

Where β is 232K/(232K+56K). If the N2VIN is 0.567 then the V2 is approximately equal to -12V.

The another negative voltage input V3 (approximate -5V) also can be evaluated by the similar method and the serial resistors can be selected with R5=120K ohms and R6=56K ohms by the Winbond recommended. The expression equation of V3 With -5V voltage is shown as follows.

$$V_3 = \frac{N5VIN - VREF \times \gamma}{1 - \gamma}$$

Where the γ is set to 120K/(120K+56K). If the monitored ADC value in the N5VIN channel is 0.8635, VREF=3.6V and the parameter γ is 0.6818 then the negative voltage of V3 can be evalated to be -5V.

6.3.3 Temperature Measurement Machine

The temperature data format is 8-bit two's-complement for sensor 2 and 9-bit two's-complement for sensor 1. The 8-bit temperature data can be obtained by reading the CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1 CR[50h] and the LSB from the Bank1 CR[51h] bit 7. The format of the temperature data is show in Table 1.

Temperature	8-Bit Digital Output		9-Bit Digital Output	
	8-Bit Binary	8-Bit Hex	9-Bit Binary	9-Bit Hex
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Table 2.

6.3.3.1 Monitor temperature from thermistor:

The W83697HF can connect three thermistors to measure three different envirment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 9.2, the themistor is connected by a serial resistor with 10K Ohms, then connect to VREF (Pin 101).

6.3.3.2 Monitor temperature from Pentium II™ thermal diode or bipolar transistor 2N3904

The W83697HF can alternate the thermistor to Pentium II™ (Deschutes) thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 9.3. The pin of Pentium II™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin VTINx in the W83697HF. The resistor R=30K ohms should be connected to VREF to supply the diode bias current

and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied togeter to act as a thermal diode.

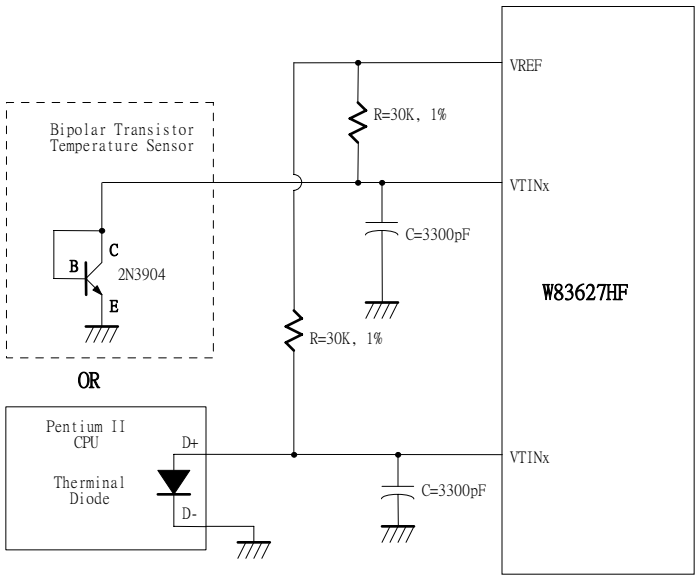


Figure 9.3

6.4 FAN Speed Count and FAN Speed Control

6.4.1 Fan Speed Count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 9.4.

Determine the fan counter according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

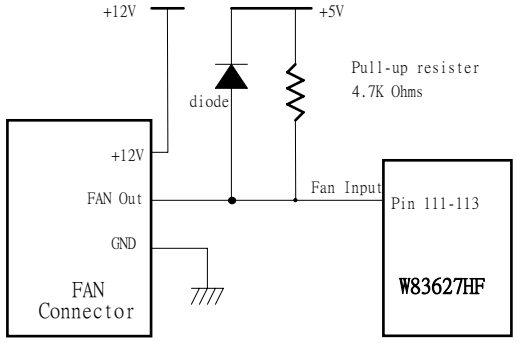
In other words, the fan speed counter has been read from register CR28 or CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

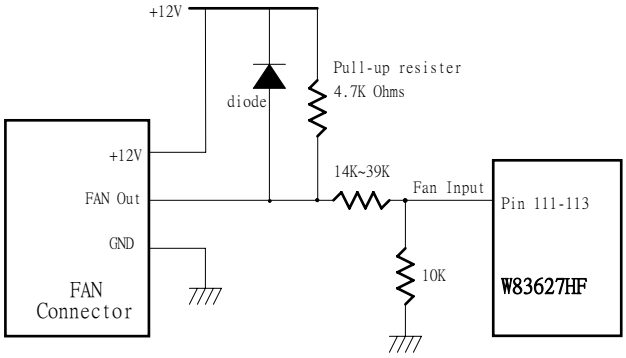
The default divisor is 2 and defined at CR47.bit7~4, CR4B.bit7~6, and Bank0 CR5D.bit5~7 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, PRM, and count.

Divisor	Nominal PRM	Time per Revolution	Counts	70% RPM	Time for 70%
1	8800	6.82 ms	*153*	6160	9.74 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

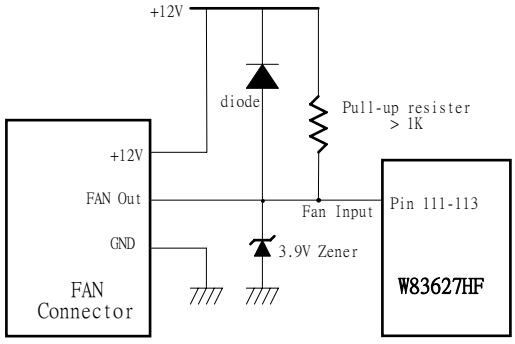
Table 1.



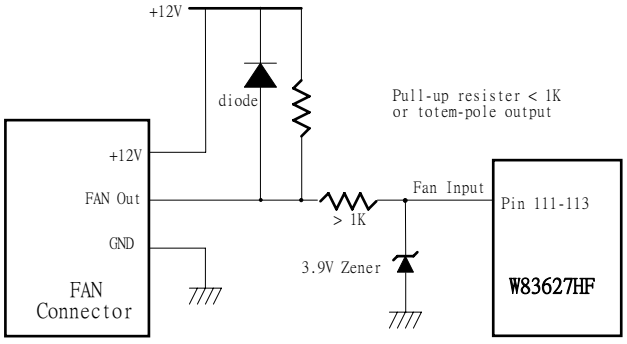
Fan with Tach Pull-Up to +5V



Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator



Fan with Tach Pull-Up to +12V and Zener Clamp



Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Zener Clamp

Figure 9.4

6.4.2 Fan Speed Control

The W83697HF provides 2 sets for fan PWM speed control. The duty cycle of PWM can be programmed by a 8-bit registers which are defined in the Bank0 CR5A and CR5B. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The PWM clock frequency also can be program and defined in the Bank0.CR5C . The application circuit is shown as follows.

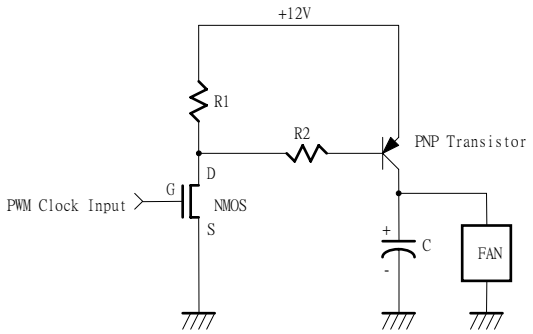


Figure 9.5

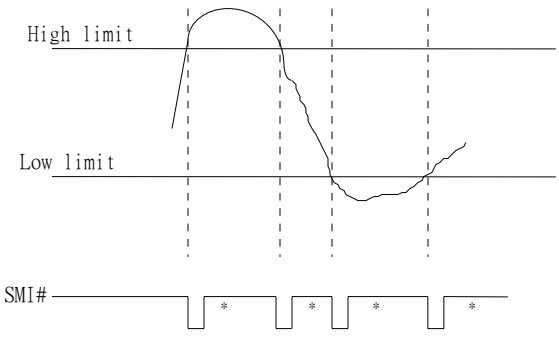
6.5 SMI# Interrupt Mode

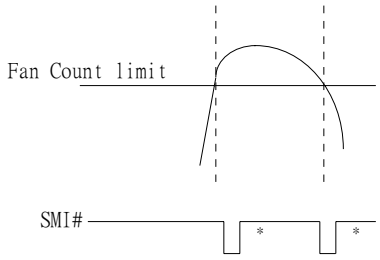
6.5.1 Voltage SMI# mode

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 9.6)

6.5.2 Fan SMI# mode

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 9.7)





*Interrupt Reset when Interrupt Status Registers are read

Figure 9.6 Figure 9.7

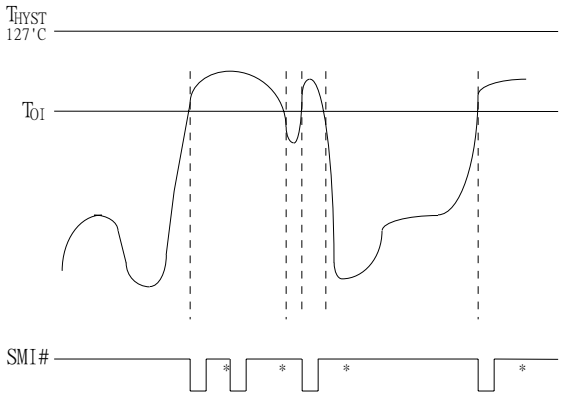
6.5.3 The W83697HF temperature sensor 1 SMI# interrupt has two modes

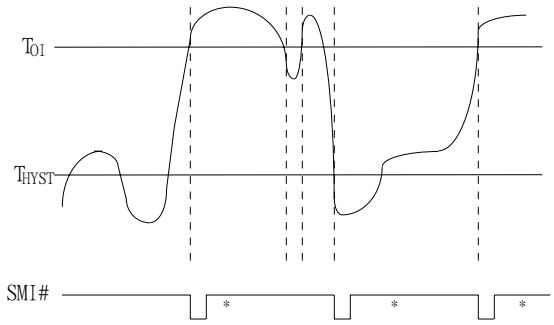
(1) Comparator Interrupt Mode

Setting the T_{HYST} (Temperature Hysteresis) limit to 127°C will set temperature sensor 1 SMI# to the Comparator Interrupt Mode. Temperature exceeds T_O (Over Temperature) Limit causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_O , the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_O. (Figure 9.8)

(2) Two-Times Interrupt Mode

Setting the T_{HYST} lower than T_O will set temperature sensor 1 SMI# to the Two-Times Interrupt Mode. Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST} , the interrupt will not occur. (Figure 9.9)





*Interrupt Reset when Interrupt Status Registers are read

Figure 9.8 Figure 9.9

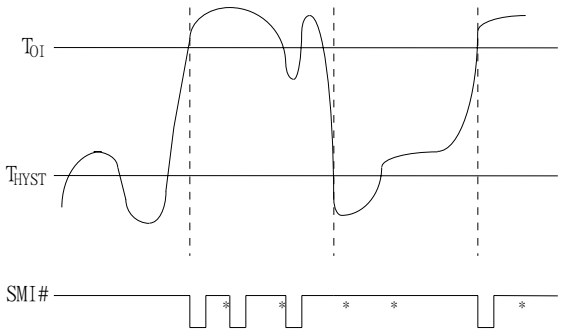
6.5.4 The W83697HF temperature sensor 2 SMI# interrupt has two modes and it is programmed at CR[4Ch] bit 6.

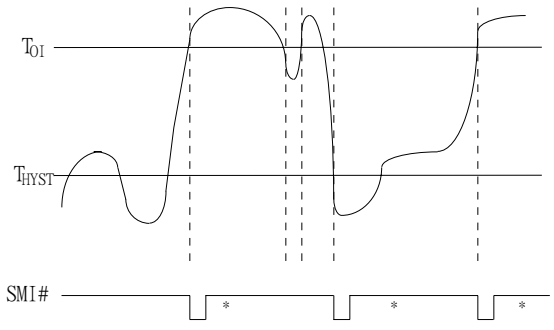
(1) Comparator Interrupt Mode

Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 9.10)

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 9.11)





*Interrupt Reset when Interrupt Status Registers are read

Figure 9.10 Figure 9.11

6.6 OVT# Interrupt Mode

The OVT# signal is only related with temperature sensor 2 (VTIN2).

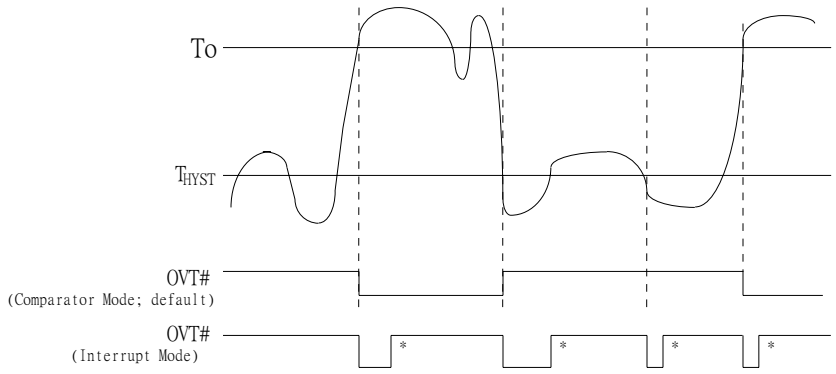
6.6.1 The W83697HF temperature sensor 2 Over-Temperature (OVT#) has the following modes

(1) Comparator Mode:

Setting Bank1/2 CR[52h] bit 2 to 0 will set OVT# signal to comparator mode. Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 9.12)

(2) Interrupt Mode:

Setting Bank1/2 CR[52h] bit 2 to 1 will set OVT# signal to interrupt mode. Setting Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor 2 or sensor 3 registers. Temperature exceeding T_O , then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O , then reset, if the temperature remains above T_{HYST} , the OVT# will not be activated again.(Figure 9.12)



*Interrupt Reset when Temperature 2/3 is read

6.7 REGISTERS AND RAM

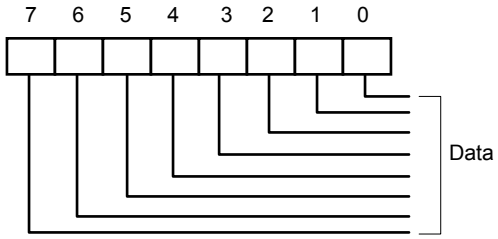
Address Register (Port x5h)

Data Port: Port x5h

Power on Default Value 00h

Attribute: Bit 6:0 Read/write , Bit 7: Read Only

Size: 8 bits



Bit7: Read Only

The logical 1 indicates the device is busy because of a Serial Bus transaction or another LPC bus transaction. With checking this bit, multiple LPC drivers can use W83697HF hardware monitor without interfering with each other or a Serial Bus driver.

It is the user's responsibility not to have a Serial Bus and LPC bus operations at the same time.

This bit is:

Set: with a write to Port x5h or when a Serial Bus transaction is in progress.

Reset: with a write or read from Port x6h if it is set by a write to Port x5h.

Bit 6-0: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Busy (Power On default 0)	Address Pointer (Power On default 00h)						
	A6	A5	A4	A3	A2	A1	A0

Address Pointer Index (A6-A0)

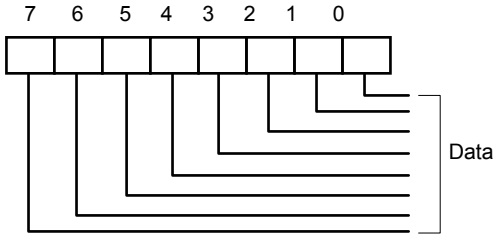
Registers and RAM	A6-A0 in Hex	Power On Value of Registers: <k7:0>in Binary	Notes
Configuration Register	40h	00001000	
Interrupt Status Register 1	41h	00000000	Auto-increment to the address of Interrupt Status Register 2 after a read or write to Port x6h.
Interrupt Status Register 2	42h	00000000	
SMI#Ý Mask Register 1	43h	00000000	Auto-increment to the address of SMIÝ Mask Register 2 after a read or write to Port x6h.
SMIÝ Mask Register 2	44h	00000000	
NMI Mask Register 1	45h	00000000	AUTO-INCREMENT TO THE ADDRESS OF NMI MASK REGISTER 2 AFTER A READ OR WRITE TO PORT X6H
NMI Mask Register 2	46h	01000000	
Fan Divisor Register	47h	<7:4> = 0101;	
Reserved	48h		
Device ID Register	49h	<7:1> = 0000001	
Reserved	4Ah		
Reserved	4Bh		
SMI#/OVT# Property Select Register	4Ch	<7:0> = 00000000	
FAN IN/OUT and BEEP Control Register	4Dh	<7:0> = 00010101	
Register 50h-5Fh Bank Select Register	4Eh	<7> = 1; <6:3> = Reserved; <2:0> = 000	
Winbond Vendor ID Register	4Fh	<7:0> = 01011100 (High Byte) <7:0> = 10100011 (Low Byte)	

Address Pointer Index (A6-A0), continued

Registers and RAM	A6-A0 in Hex	Power On Value of Registers: <k7:0>in Binary	Notes
POST RAM	00-1Fh		Auto-increment to the next location after a read or write to Port x6h and stop at 1Fh.
Value RAM	20-3Fh		
Value RAM	60-7Fh		Auto-increment to the next location after a read or write to Port x6h and stop at 7Fh.
Temperature 2 Registers	Bank1 50h-56h		
Reserved	Bank2 50h-56h		
Additional Configuration Registers	Bank4 50h-5Dh		

Data Register (Port x6h)

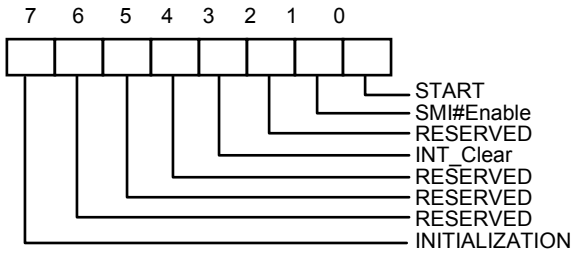
Data Port:	Port x6h
Power on Default Value	00h
Attribute:	Read/write
Size:	8 bits



Bit 7-0: Data to be read from or to be written to RAM and Register.

Configuration Register — Index 40h

Register Location:	40h
Power on Default Value	01h
Attribute:	Read/write
Size:	8 bits



Bit 7: A one restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.

Bit 6: Reserced

Bit 5: Reserved

Bit 4: Reserved

Bit 3: A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: Reserved

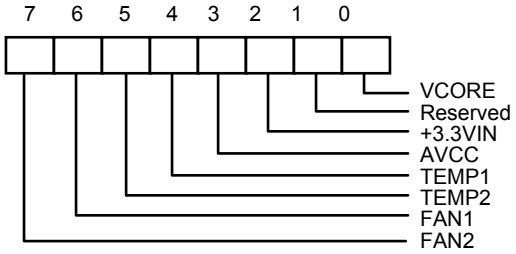
Bit 1: A one enables the SMI# Interrupt output.

Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

Interrupt Status Register 1— Index 41h

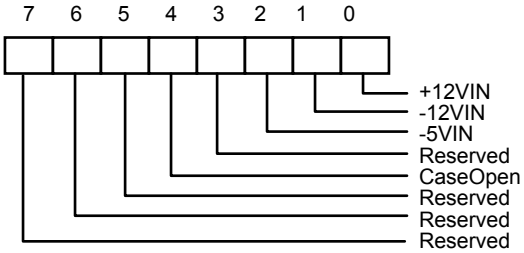
Register Location:	41h
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7: A one indicates the fan count limit of FAN2 has been exceeded.
Bit 6: A one indicates the fan count limit of FAN1 has been exceeded.
Bit 5: A one indicates a High limit of VTIN2 has been exceeded from temperature sensor 2.
Bit 4: A one indicates a High limit of VTIN1 has been exceeded from temperature sensor 1.
Bit 3: A one indicates a High or Low limit of +5VIN has been exceeded.
Bit 2: A one indicates a High or Low limit of +3.3VIN has been exceeded.
Bit 1: Reserved
Bit 0: A one indicates a High or Low limit of VCORE has been exceeded.

Interrupt Status Register 2 — Index 42h

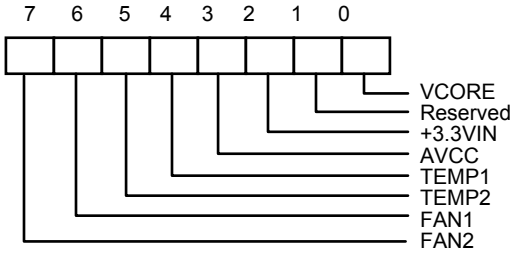
Register Location:	42h
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7-6:Reserved.This bit should be set to 0.
Bit 5: Reserved.
Bit 4: A one indicates case has been opened.
Bit 3: Reserved.
Bit 2: A one indicates a High or Low limit of -5VIN has been exceeded.
Bit1: A one indicates a High or Low limit of -12VIN has been exceeded.
Bit0: A one indicates a High or Low limit of +12VIN has been exceeded.

SMI# Mask Register 1 — Index 43h

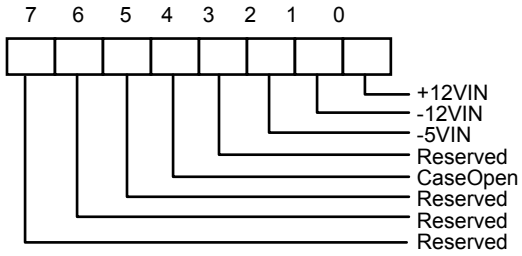
Register Location:	43h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

SMI# Mask Register 2 — Index 44h

Register Location:	44h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



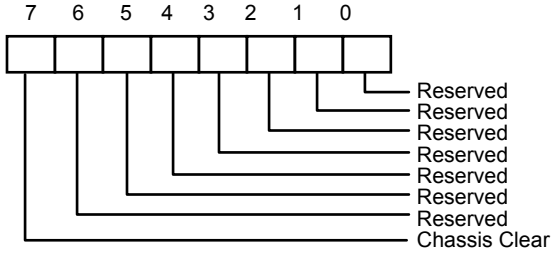
Bit 7-6: Reserved. This bit should be set to 0.

Bit 5-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Reserved Register — Index 45h

Chassis Clear Register -- Index 46h

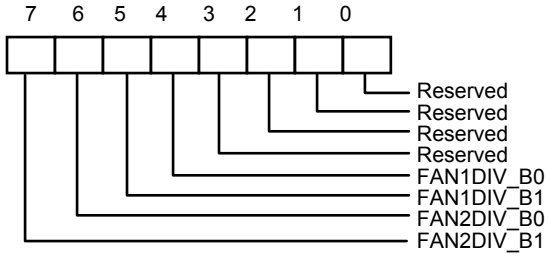
Register Location: 46h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Set 1 , clear case open event. This bit self clears after clearing case open event.
Bit 6-0:Reserved. This bit should be set to 0.

Fan Divisor Register — Index 47h

Register Location: 47h
Power on Default Value 5fh
Attribute: Read/Write
Size: 8 bits



Bit 7-6: FAN2 Speed Control.
Bit 5-4: FAN1 Speed Control.
Bit 3-0: Reserved
Note : Please refer to Bank0 CR[5Dh] , Fan divisor table.

Value RAM — Index 20h- 3Fh or 60h - 7Fh (auto-increment)

Address A6-A0	Address A6-A0 with Auto-Increment	Description
20h	60h	VCORE reading
21h	61h	Reserved
22h	62h	+3.3VIN reading
23h	63h	AVCC(+5V) reading
24h	64h	+12VIN reading
25h	65h	-12VIN reading
26h	66h	-5VIN reading
27h	67h	Temperature sensor 1 reading
28h	68h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	69h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Bh	6Bh	VCORE High Limit
2Ch	6Ch	VCORE Low Limit
2Dh	6Dh	Reserved
2Eh	6Eh	Reserved
2Fh	6Fh	+3.3VIN High Limit
30h	70h	+3.3VIN Low Limit
31h	71h	AVCC(+5V) High Limit
32h	72h	AVCC(+5V) Low Limit
33h	73h	+12VIN High Limit
34h	74h	+12VIN Low Limit
35h	75h	-12VIN High Limit

Value RAM — Index 20h- 3Fh or 60h - 7Fh (auto-increment), continued

Address A6-A0	Address A6-A0 with Auto-Increment	Description
36h	76h	-12VIN Low Limit
37h	77h	-5VIN High Limit
38h	78h	-5VIN Low Limit
39h	79h	Temperature sensor 1 (VTIN1) High Limit
3Ah	7Ah	Temperature sensor 1 (VTIN1) Hysteresis Limit
3Bh	7Bh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	7Ch	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	7Dh	Reserved.
3E- 3Fh	7E- 7Fh	Reserved

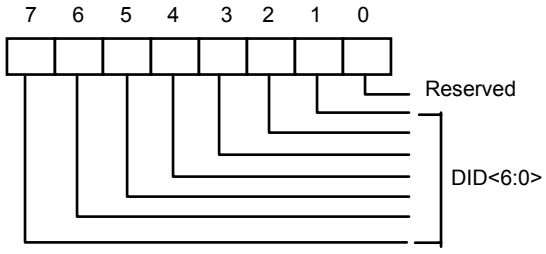
Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

Device ID Register - Index 49h

Register Location: 49h

Power on Default Value <7:1> is 000,0001 binary

Size: 8 bits



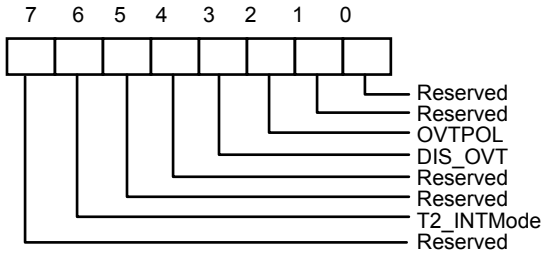
Bit 7-1: Read Only - Device ID<6:0>

Bit 0 : Reserved

Reserved - Index 4Bh

SMI#/OVT# Property Select Register- Index 4Ch

Register Location:	4Ch
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



Bit 7: Reserved. User Defined.

Bit6: Set to 1, the SMI# output type of Temperature 2(VTIN2) is set to Comparator Interrupt mode. Set to 0, the SMI# output type is set to Two-Times Interrupt mode. (default 0)

Bit5: Reserved. User Defined.

Bit 4: Reserved

Bit 3: Disable temperature sensor 2 over-temperature (OVT) output if set to 1. Default 0, enable OVT(Temp 2) output through pin OVT#.

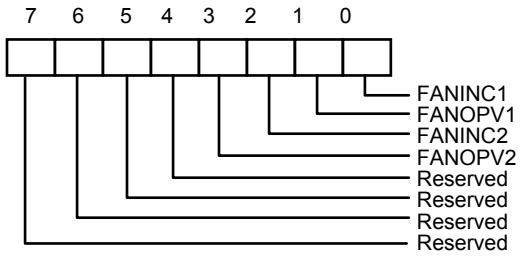
Bit 2: Over-temperature polarity. Write 1, OVT# active high. Write 0, OVT# active low. Default 0.

Bit 1: Reserved.

Bit 0: Reserved.

FAN IN/OUT and BEEP Control Register- Index 4Dh

Register Location:	4Dh
Power on Default Value	15h
Attribute:	Read/Write
Size:	8 bits



Bit 7~4: Reserved.

Bit 3: FAN 2 output value if FANINC2 sets to 0. Write 1, then pin 113 always generate logic high signal. Write 0, pin 113 always generates logic low signal. This bit default 0.

Bit 2: FAN 2 Input Control. Set to 1, pin 113 acts as FAN clock input, which is default value. Set to 0, this pin 113 acts as FAN control signal and the output value of FAN control is set by this register bit 3.

Bit 1: FAN 1 output value if FANINC1 sets to 0. Write 1, then pin 114 always generate logic high signal. Write 0, pin 114 always generates logic low signal. This bit default 0.

Bit 0: FAN 1 Input Control. Set to 1, pin 114 acts as FAN clock input, which is default value. Set to 0, this pin 114 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

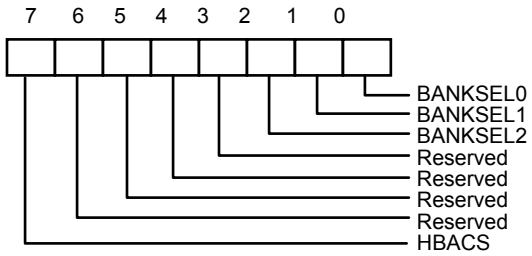
Register 50h ~ 5Fh Bank Select Register - Index 4Eh

Register Location: 4Eh

Power on Default Value 80h

Attribute: Read/Write

Size: 8 bits



Bit 7: HBACS- High byte access. Set to 1, access Register 4Fh high byte register.

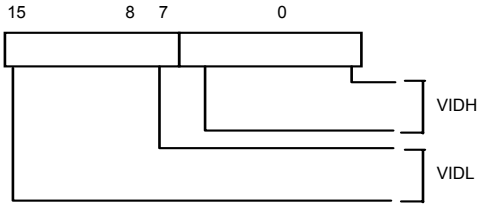
Set to 0, access Register 4Fh low byte register. Default 1.

Bit 6-3: Reserved. This bit should be set to 0.

Bit 2-0: Index ports 0x50~0x5F Bank select.

Winbond Vendor ID Register - Index 4Fh (No Auto Increase)

Register Location:	4Fh
Power on Default Value	<15:0> = 5CA3h
Attribute:	Read Only
Size:	16 bits



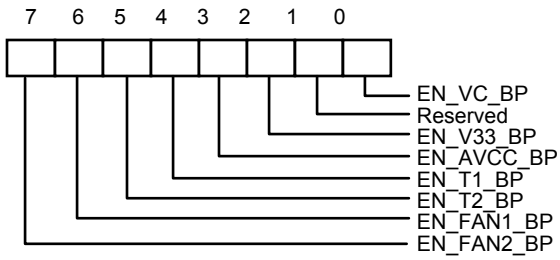
Bit 15-8: Vendor ID High Byte if CR4E.bit7=1.Default 5Ch.

Bit 7-0: Vendor ID Low Byte if CR4E.bit7=0. Default A3h.

Winbond Test Register -- Index 50h - 55h (Bank 0)

BEEP Control Register 1-- Index 56h (Bank 0)

Register Location:	56h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



Bit 7: Enable BEEP Output from FAN 2 if the monitor value exceed the limit value. Write 1, enable BEEP output, which is default value.

Bit 6: Enable BEEP Output from FAN 1 if the monitor value exceed the limit value. Write 1, enable BEEP output, which is default value.

Bit 5: Enable BEEP Output from Temperature Sensor 2 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0

Bit 4: Enable BEEP output for Temperature Sensor 1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0

Bit 3: Enable BEEP output from AVCC (+5V), Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 2: Enable BEEP output from +3.3V. Write 1, enable BEEP output, which is default value.

Bit 1: Reserved

Bit 0: Enable BEEP Output from VCORE if the monitor value exceed the limits value. Write 1, enable BEEP output, which is default value

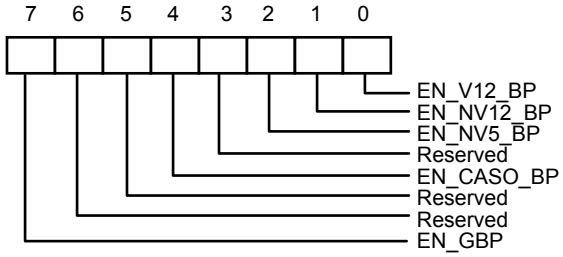
BEEP Control Register 2-- Index 57h (Bank 0)

Register Location: 57h

Power on Default Value 80h

Attribute: Read/Write

Size: 8 bits



Bit 7: Enable Global BEEP. Write 1, enable global BEEP output. Default 1. Write 0, disable all BEEP output.

Bit 6: Reserved. This bit should be set to 0.

Bit5: Reserved

Bit 4: Enable BEEP output for case open if case opend. Write 1, enable BEEP output. Default 0.

Bit 3: Reserved

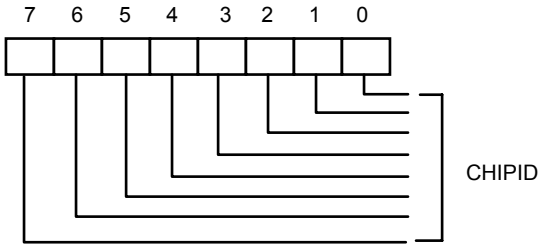
Bit 2: Enable BEEP output from -5V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 1: Enable BEEP output from -12V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 0: Enable BEEP output from +12V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Chip ID -- Index 58h (Bank 0)

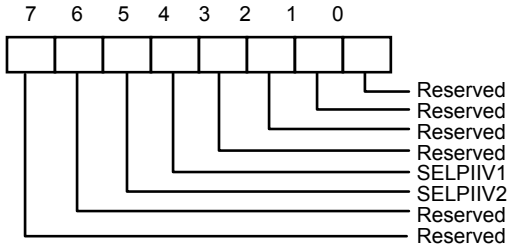
Register Location: 58h
Power on Default Value 60h
Attribute: Read Only
Size: 8 bits



Bit 7: Winbond Chip ID number. Read this register will return 60h.

Reserved Register -- Index 59h (Bank 0)

Register Location: 59h
Power on Default Value <7>=0 and <6:4> = 111 and <3:0> = 0000
Attribute: Read/Write
Size: 8 bits



Bit 7-6: Reserved

Bit 5: Temperature sensor diode 2. Set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode.

Bit 4: Temperature sensor diode 1. Set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode.

Bit 3-0: Reserved

Reserved -- Index 5Ah (Bank 0)

Reserved -- Index 5Bh (Bank 0)

Reserved -- Index 5Ch (Bank 0)

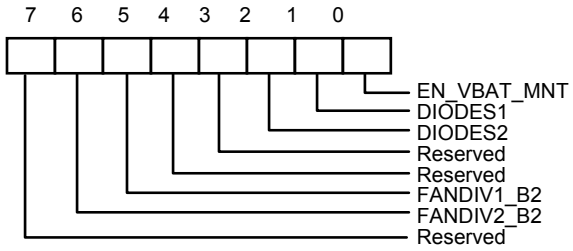
VBAT Monitor Control Register -- Index 5Dh (Bank 0)

Register Location: 5Dh

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: Reserved.

Bit 6: Fan2 divisor Bit 2.

Bit 5: Fan1 divisor Bit 2.

Bit 4 –3 : Reserved.

Bit 2: Sensor 2 type selection. Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.

Bit 1: Sensor 1 type selection. Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.

Bit 0: Set to 1, enable battery voltage monitor. Set to 0, disable battery voltage monitor. If enable this bit, the monitor value is value after one monitor cycle. Note that the monitor cycle time is at least 300ms for W83697HF hardware monitor.

Fan divisor table:

Bit 2	Bit 1	Bit 0	Fan Divisor	Bit 2	Bit 1	Bit 0	Fan Divisor
0	0	0	1	1	0	0	16
0	0	1	2	1	0	1	32
0	1	0	4	1	1	0	64
0	1	1	8	1	1	1	128

Reserved Register -- 5Eh (Bank 0)

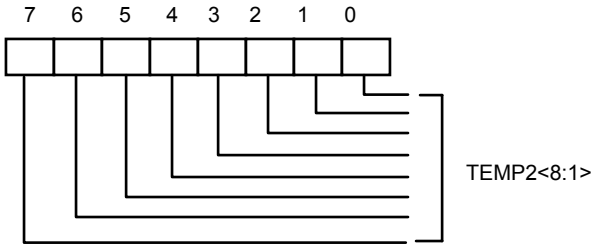
Reserved Register -- 5Fh (Bank 0)

Temperature Sensor 2 Temperature (High Byte) Register - Index 50h (Bank 1)

Register Location: 50h

Attribute: Read Only

Size: 8 bits



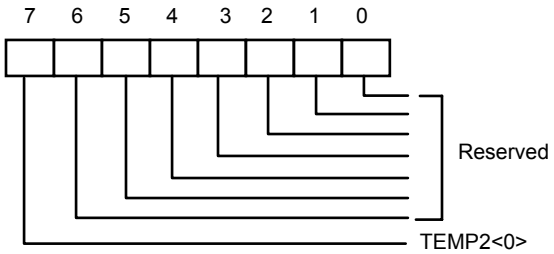
Bit 7: Temperature <8:1> of sensor 2, which is high byte, means 1°C.

Temperature Sensor 2 Temperature (Low Byte) Register - Index 51h (Bank 1)

Register Location: 51h

Attribute: Read Only

Size: 8 bits



Bit 7: Temperature <0> of sensor2, which is low byte, means 0.5°C.

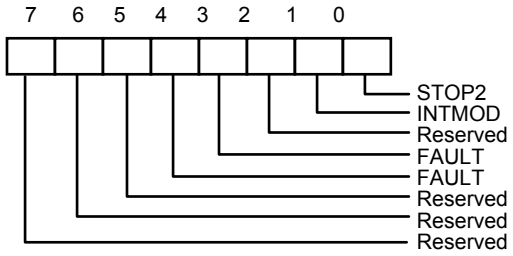
Bit 6-0: Reserved.

Temperature Sensor 2 Configuration Register - Index 52h (Bank 1)

Register Location: 52h

Power on Default Value 00h

Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - OVT# Interrupt mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

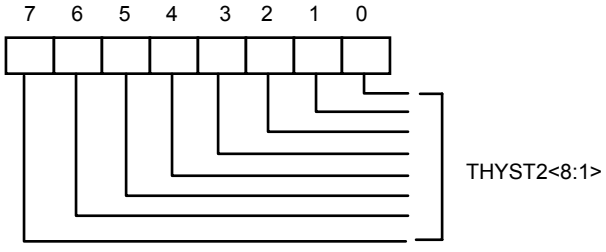
Temperature Sensor 2 Hysteresis (High Byte) Register - Index 53h (Bank 1)

Register Location: 53h

Power on Default Value 4Bh

Attribute: Read/Write

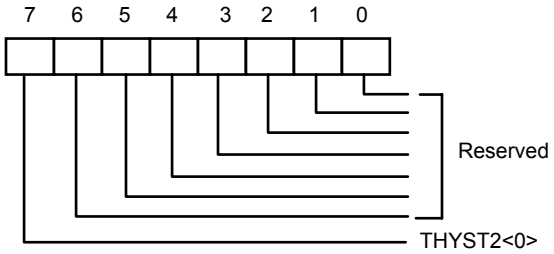
Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

Temperature Sensor 2 Hysteresis (Low Byte) Register - Index 54h (Bank 1)

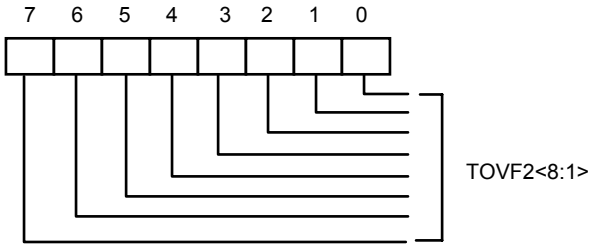
Register Location: 54h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Hysteresis temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

Temperature Sensor 2 Over-temperature (High Byte) Register - Index 55h (Bank 1)

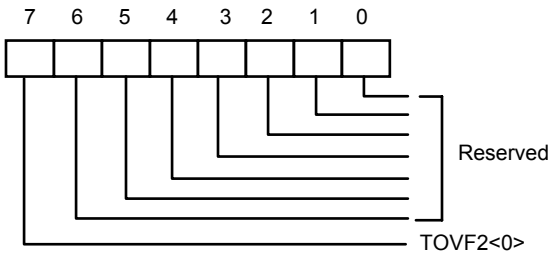
Register Location: 55h
Power on Default Value 50h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

Temperature Sensor 2 Over-temperature (Low Byte) Register - Index 56h (Bank 1)

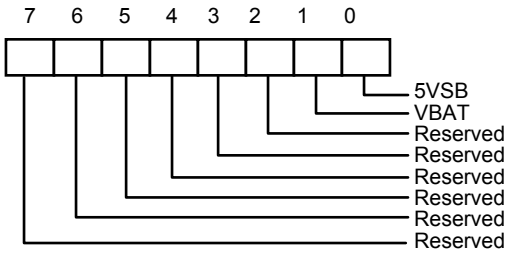
Register Location: 56h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Over-temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

Interrupt Status Register 3 -- Index 50h (BANK4)

Register Location: 50h
Power on Default Value 00h
Attribute: Read Only
Size: 8 bits



Bit 7-2: Reserved.
Bit 1: A one indicates a High or Low limit of VBAT has been exceeded.
Bit 0: A one indicates a High or Low limit of 5VSB has been exceeded.

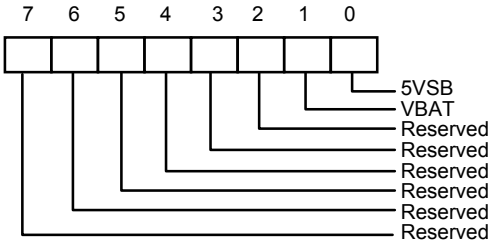
SMI# Mask Register 3 -- Index 51h (BANK 4)

Register Location: 51h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-2: Reserved.

Bit 1: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Reserved Register -- Index 52h (Bank 4)

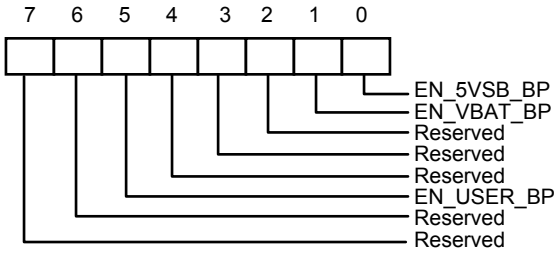
BEEP Control Register 3-- Index 53h (Bank 4)

Register Location: 53h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: Reserved.

Bit 5: User define BEEP output function. Write 1, the BEEP is always active. Write 0, this function is inactive. (Default 0)

Bit 4-2: Reserved.

Bit 1: Enable BEEP output from VBAT. Write 1, enable BEEP output, which is default value.

Bit 0: Enable BEEP Output from 5VSB. Write 1, enable BEEP output, which is default value.

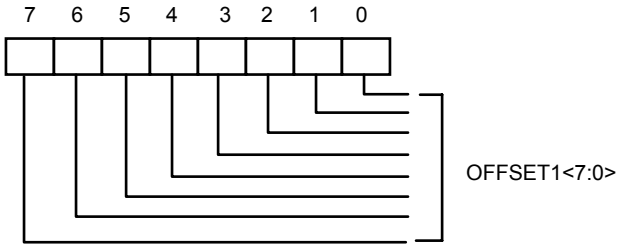
Temperature Sensor 1 Offset Register -- Index 54h (Bank 4)

Register Location: 54h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-0: Temperature 1 base temperature. The temperature is added by both monitor value and offset value.

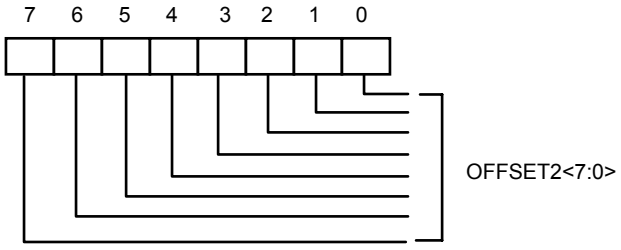
Temperature Sensor 2 Offset Register -- Index 55h (Bank 4)

Register Location: 55h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-0: Temperature 2 base temperature. The temperature is added by both monitor value and offset value.

Reserved Register -- Index 57h--58h

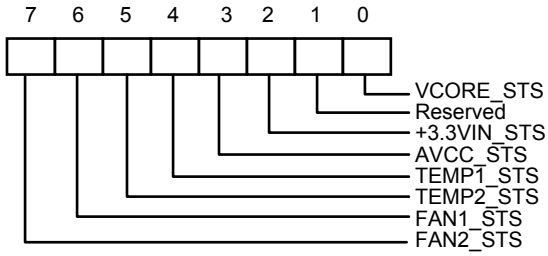
Real Time Hardware Status Register I -- Index 59h (Bank 4)

Register Location: 59h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits



Bit 7: FAN 2 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 6: FAN 1 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 5: Temperature sensor 2 Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.

Bit 4: Temperature sensor 1 Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.

Bit 3: AVCC Voltage Status. Set 1, the voltage of +5V is over the limit value. Set 0, the voltage of +5V is in the limit range.

Bit 2: +3.3V Voltage Status. Set 1, the voltage of +3.3V is over the limit value. Set 0, the voltage of +3.3V is in the limit range.

Bit 1: Reserved

Bit 0: VCORE Voltage Status. Set 1, the voltage of VCORE A is over the limit value. Set 0, the voltage of VCORE A is in the limit range.

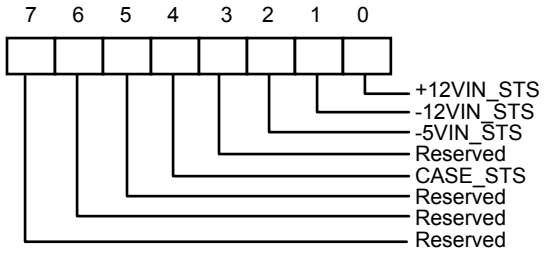
Real Time Hardware Status Register II -- Index 5Ah (Bank 4)

Register Location: 5Ah

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits



Bit 7-6: Reserved

Bit 5: Reserved

Bit 4: Case Open Status. Set 1, the case open sensor is sensed the high value. Set 0

Bit 3: Reserved

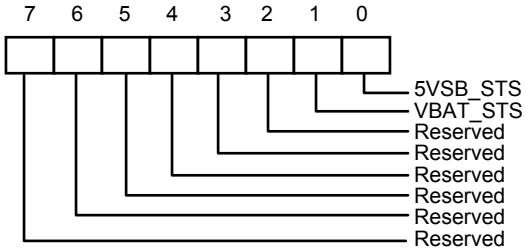
Bit 2: -5V Voltage Status. Set 1, the voltage of -5V is over the limit value. Set 0, the voltage of -5V is during the limit range.

Bit 1: -12V Voltage Status. Set 1, the voltage of -12V is over the limit value. Set 0, the voltage of - 12V is during the limit range.

Bit 0: +12V Voltage Status. Set 1, the voltage of +12V is over the limit value. Set 0, the voltage of +12V is in the limit range.

Real Time Hardware Status Register III -- Index 5Bh (Bank 4)

Register Location:	5Bh
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7-2: Reserved.

Bit 1: VBAT Voltage Status. Set 1, the voltage of VBAT is over the limit value. Set 0, the voltage of VBAT is during the limit range.

Bit 0: 5VSB Voltage Status. Set 1, the voltage of 5VSB is over the limit value. Set 0, the voltage of 5VSB is in the limit range.

Reserved Register -- Index 5Ch (Bank 4)

Reserved Register -- Index 5Dh (Bank 4)

Value RAM 2— Index 50h - 5Ah (auto-increment) (BANK 5)

Address A6-A0 Auto-Increment	Description
50h	5VSB reading
51h	VBAT reading
52h	Reserved
53h	Reserved
54h	5VSB High Limit
55h	5VSB Low Limit.
56h	VBAT High Limit
57h	VBAT Low Limit

Winbond Test Register -- Index 50h (Bank 6)

FAN 1 Pre-Scale Register--Index00h(Bank 0)

Power on default [7:0] = 0000-0001 b

Bit	Name	Read/Write	Description
7	PWM_CLK_SEL1	Read/Write	**PWM Input Clock Select.** This bit select Fan 1 input clock to pre-scale divider. 0: 24 MHz 1: 180 KHz
6-0	PRE_SCALE1[6:0]	Read/Write	**Fan 1 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 1 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 01h: divider is 1 02h: divider is 2 03h: divider is 3 : :

PWM frequency = (Input Clock / Pre-scale) / 256

FAN 1 Duty Cycle Select Register-- 01h (Bank 0)

Power on default [7:0] 1111,1111 b

Bit	Name	Read/Write	Description
7-0	F1_DC[7:0]	Read/Write	**FanPWM1 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan 1 control mode, read this register will return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX/256*100%) during one cycle.

FAN 2 Pre-Scale Register-- Index 02h

Power on default [7:0] = 0000,0001 b

Bit	Name	Read/Write	Description
7	PWM_CLK_SEL2	Read/Write	**PWM 2 Input Clock Select.** This bit select Fan 2 input clock to pre-scale divider. 0: 1 MHz 1: 125 KHz
6-0	PRE_SCALE2[6:0]	Read/Write	**Fan 2 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 01h: divider is 1 02h: divider is 2 03h: divider is 3 : :

PWM frequency = (Input Clock / Pre-scale) / 256

FAN2 Duty Cycle Select Register-- Index 03h

Power on default [7:0] = 1111,1111 b

Bit	Name	Read/Write	Description
7-0	F2_DC[7:0]	Read/Write	**FanPWM2 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan 2 control mode, read this register will return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is XX/256*100% during one cycle.

FAN Configuration Register-- Index 04h

Power on default [7:0] = 0000,0000 b

Bit	Name	Read/Write	Description
7-2	Reserved	Read/Write	Reserved
5-4	FAN2_MODE	Read/Write	FAN 2 PWM Control Mode. 00 - Manual PWM Control Mode. (Default) 01 - Thermal Cruise mode. 10 - Fan Speed Cruise Mode. 11 - Reserved.
3-2	FAN1_MODE	Read/Write	FAN 1 PWM Control Mode. 00 - Manual PWM Control Mode. (Default) 01 - Thermal Cruise mode. 10 - Fan Speed Cruise Mode. 11 - Reserved.
1	FAN2_OB	Read/Write	**Enable Fan 2 as Output Buffer.** Set to 0, FANPWM2 can drive logical high or logical low. Set to 1, FANPWM2 is open-drain
0	FAN1_OB	Read/Write	**Enable Fan 1 as Output Buffer.** Set to 1, FANPWM1 can drive logical high or logical low. Set to 1, FANPWM1 is open-drain

VTIN1 Target Temperature Register/ Fan 1 Target Speed Register -- Index 05h

Power on default [7:0] = 0000,0000 b

CPUT1 target temperature register for Thermal Cruise mode.

Bit	Name	Read/Write	Description
7	Reserved	Read/Write	**Reserved.**
6-0	TEMP_TAR_T1[6:0]	Read/Write	**VTIN1 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit3-2 is 01.

Fan 1 target speed register for Fan Speed Cruise mode.

Bit	Name	Read/Write	Description
7-0	SPD_TAR_FAN1[7:0]	Read/Write	**Fan 1 Target Speed Control.** Only for Fan Speed Cruise Mode while CR84h bit3-2 is 10.

VTIN2 Target Temperature Register/ Fan 2 Target Speed Register -- Index 06h

Power on - [7:0] = 0000,0000 b

CPUT2 target temperature register for Thermal Cruise mode.

Bit	Name	Read/Write	Description
7	Reserved	Read/Write	**Reserved.**
6-0	TEMP_TAR_T2[6:0]	Read/Write	**VTIN2 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit5-4 is 01.

Fan 2 target speed register for Fan Speed Cruise mode.

Bit	Name	Read/Write	Description
7-0	SPD_TAR_FAN2[7:0]	Read/Write	**Fan 2 Target Speed Control.** Only for Fan Speed Cruise Mode while CR84h bit5-4 is 10.

Tolerance of Target Temperature or Target Speed Register -- Index 07h

Power on default [7:0] = 0001,0001 b

Tolerance of CPUT1/CPUT2 target temperature register.

Bit	Name	Read/Write	Description
7-4	TOL_T2[3:0]	Read/Write	**Tolerance of VTIN2 Target Temperature.** Only for Thermal Cruise mode.
3-0	TOL_T1[3:0]	Read/Write	**Tolerance of VTIN1 Target Temperature.** Only for Thermal Cruise mode.

Tolerance of Fan 1/2 target speed register.

Bit	Name	Read/Write	Description
7-4	TOL_FS2[3:0]	Read/Write	**Tolerance of Fan 2 Target Speed Count.** Only for Fan Speed Cruise mode.
3-0	TOL_FS1[3:0]	Read/Write	**Tolerance of Fan 1 Target Speed Count.** Only for Fan Speed Cruise mode.

Fan 1 PWM Stop Duty Cycle Register -- Index 08h

Power on default [7:0] = 0000,0001 b

Bit	Name	Read/Write	Description
7-0	STOP_DC1[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this value. This register should be written a non-zero minimum PWM stop duty cycle.

Fan 2 PWM Stop Duty Cycle Register -- 09h (Bank 0)

Power on default [7:0] = 0000,0001 b

Bit	Name	Read/Write	Description
7-0	STOP_DC2[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this register value. This register should be written a non-zero minimum PWM stop duty cycle.

Fan 1 Start-up Duty Cycle Register -- Index 0Ah

Power on default [7:0] = 0000,0001 b

Bit	Name	Read/Write	Description
7-0	START_DC1[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle.

Fan 2 Start-up Duty Cycle Register -- Index 0Bh

Power on default [7:0] = 0000,0001 b

Bit	Name	Read/Write	Description
7-0	START_DC2[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle.

Fan 1 Stop Time Register -- Index 0Ch

Power on default [7:0] = 0011,1100 b

Bit	Name	Read/Write	Description
7-0	STOP_TIME1[7:0]	Read/Write	In Thermal Cruise mode, this register determines the time of which PWM duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default value is 6 seconds.

Fan 2 Stop Time Register -- Index 0Dh

Power on default [7:0] = 0011,1100 b

Bit	Name	Read/Write	Description
7-0	STOP_TIME2[7:0]	Read/Write	In Thermal Cruise mode, this register determines the time of which PWM duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default value is 6 seconds.

Fan Step Down Time Register -- Index 0Eh

Power on defualt [7:0] = 0000,1010 b

Bit	Name	Read/Write	Description
7-0	STEP_UP_T[7:0]	Read/Write	The time interval, which is 0.1 second unit, to decrease PWM duty in Smart Fan Control mode.

Fan Step Up Time Register -- Index 0Fh

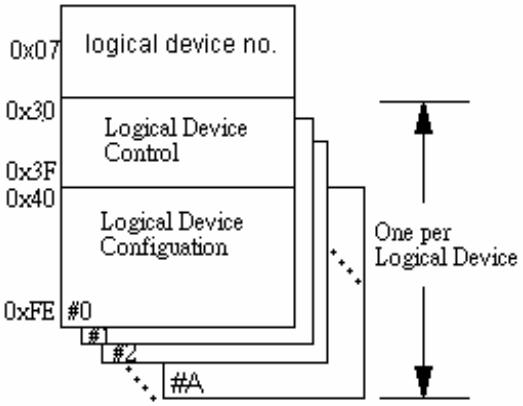
Power on default [7:0] = 0000,1010 b

Bit	Name	Read/Write	Description
7-0	STEP_DOWN_T[7:0]	Read/Write	The time interval, which is 0.1 second unit, to increase PWM duty in Smart Fan Control mode.

7. CONFIGURATION REGISTER

7.1 Plug and Play Configuration

The W83697HF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83697HF, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), CIR (Consumer IR, logical device 6), GPIO1 (logical device 7), GPIO5(logical device 8),GPIO2 ~GPIO4(logical device 9), ACPI ((logical device A), and Hardware monitor (logical device B). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



7.2 Compatible PnP

7.2.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	address and value
0	write 87h to the location 2Eh twice
1	write 87h to the location 4Eh twice

After Power-on reset, the value on RTSA# (pin 49) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration

registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

7.2.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83697HF enters the default operating mode. Before the W83697HF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

7.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh on PC/AT systems; the EFDRs are read/write registers with port address 2Fh or 4Fh on PC/AT systems.

7.3 Configuration Sequence

To program W83697HF configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

7.3.1 Enter the extended function mode

To place the chip into the extended function mode, two successive wrtites of 0x87 must be applied to Extended Function Enable Registers(EFERs, i.e. 2Eh or 4Eh).

7.3.2 Configurate the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register(EFIR) and Extended Function Data Register(EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).
First, write the Logical Device Number (i.e.,0x07) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip(Global) Control Registers, this step is not required.
Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

7.3.3 Exit the extended function mode

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

7.3.4 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;-------------------------------------------------------------------------------
; Enter the extended function mode ,interruptible double-write    |
;-------------------------------------------------------------------------------
MOV    DX,2EH
MOV AL,87H
OUT    DX,AL
OUT    DX,AL
;-------------------------------------------------------------------------
; Configurate logical device 1, configuration register CRF0   |
;-------------------------------------------------------------------------
MOV    DX,2EH
MOV    AL,07H
OUT    DX,AL           ; point to Logical Device Number Reg.
MOV    DX,2FH
MOV    AL,01H
OUT    DX,AL           ; select logical device 1
;
MOV    DX,2EH
MOV    AL,F0H
OUT    DX,AL           ; select CRF0
MOV    DX,2FH
MOV AL,3CH
OUT    DX,AL           ; update CRF0 with value 3CH
;---------------------------------------
; Exit extended function mode     |
;---------------------------------------
MOV    DX,2EH
MOV AL,AAH
OUT    DX,AL
```

7.4 Chip (Global) Control Register

CR02 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: SWRST --> Soft Reset.

CR07

Bit 7 - 0: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20

Bit 7 - 0: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x 60 (read only).

CR21

Bit 7 - 0: DEVREVB7 - DEBREVB0 --> Device Rev = 0x1X (read only).

X : Version change number .(Bit 3~0).

CR22 (Default 0xff)

Bit 7~ 5: Reserved.

Bit 4: HMPWD

= 0 Power down

= 1 No Power down

Bit 3: URBPWD

= 0 Power down

= 1 No Power down

Bit 2: URAPWD

= 0 Power down

= 1 No Power down

Bit 1: PRTPWD

= 0 Power down

= 1 No Power down

Bit 0: FDCPWD

= 0 Power down

= 1 No Power down

CR23 (Default 0x00)

Bit 7 ~ 1: Reserved.

Bit 0: IPD (Immediate Power Down). When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default 0x00)

Bit 7 : Reserved.

Bit 6: CLKSEL(Enable 48Mhz)

= 0 The clock input on Pin 1 should be 24 Mhz.

= 1 The clock input on Pin 1 should be 48 Mhz.

The corresponding power-on setting pin is SOUTB (pin 61).

Bit[5:4]: ROM size select

= 00 1M

= 01 2M

= 10 4M

= 11 Reserved

Bit3:MEMW# Select (PIN97)

= 0 MEMW# Disable

= 1 MEMW# Enable

Bit2:Reserved

Bit1 : Enable Flash ROM Interface

= 0 Flash ROM Interface is enabled after hardware reset

= 1 Flash ROM Interface is disabled after hardware reset

This bit is read only, and set/reset by power-on setting pin. The corresponding power-on setting pin is PENROM#(pin 52)

Bit 0: PNPCSV#

= 0 The Compatible PnP address select registers have default values.

= 1 The Compatible PnP address select registers have no default value.

The corresponding power-on setting pin is DTRA# (pin 50).

CR25 (Default 0x00)

Bit 7 ~ 4: Reserved

Bit 3: URBTRI

Bit 2: URATRI

Bit 1: PRTTRI

Bit 0: FDCTRI.

CR26 (Default 0x00)

Bit 7: SEL4FDD

= 0 Select two FDD mode.

= 1 Select four FDD mode.

Bit 6: HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is RTSA #(pin 49).

HEFRAS Address and Value

= 0 Write 87h to the location 2E twice.

= 1 Write 87h to the location 4Etwice.

Bit 5: LOCKREG

= 0 Enable R/W Configuration Registers.

= 1 Disable R/W Configuration Registers.

Bit4: Reserved

Bit 3: DSFDLGRQ

= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2: DSPRLGRQ

= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1: DSUALGRQ

= 0Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

Bit 0: DSUBLGRQ

= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit 7 - 3: Reserved.

Bit 2 - 0: PRTMODS2 - PRTMODS0

= 0xx Parallel Port Mode

= 100 Reserved

= 101 External FDC Mode

= 110 Reserved

= 111 External two FDC Mode

CR29 (GPIO1,5(50~51) & Game port & MIDI port Select default 0x00)

Bit 7 : Port Select (select Game Port or General Purpose I/O Port 1)

= 0 Game Port

= 1 General Purpose I/O Port 1 (pin121~128 select function GP10~GP17)

Bit [6:5] : (Pin119)

00 MSI

01 WDTO#

10 Reserved

11 GP51

Bit[4:3] : (Pin 120)

00 MSO

01 PLED

10 Reserved

11 GP50

Bit 2 :(Pin117)

OVT# & SMI Select(Pin117)

= 0 OVT#

= 1 SMI#

Bit 1~0 : Reserved

CR2A(GPIO2 ~ 5& Flash ROM Interface Select

Default 0xFF if PENROM# = 0 during

POR, default 0x00 otherwise)

Bit 7 : (PIN 86 ~89 & 91 ~94)

= 0 GPIO 2

= 1 Flash IF (xD7 ~ XD0)

Bit 6 : (PIN 78 ~ 85)

= 0 GPIO 3

= 1 Flash IF (XA7 ~ XA0)

Bit 5 : (PIN 69 ~ 74 & 76 ~77)

= 0 GPIO 4

= 1 Flash IF (XA!5 ~ XA10 & XA7 ~ A0)

Bit 4: (PIN 66 ~ 68 & 95 ~ 97)

= 0 GPIO 5(GP52 ~ 57)

= 1 Flash IF(XA18 ~ XA16 , ROMCS#, MEMR #, MEMW#)

Bit 0~3 : Reserved

7.5 Logical Device 0 (FDC)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xf0 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for FDC.

CR74 (Default 0x02 if PNPCSV = 0 during POR, default 0x04 otherwise)

Bit 7 - 3: Reserved.

Bit 2 - 0: These bits select DRQ resource for FDC.

= 0x00 DMA0

= 0x01 DMA1

= 0x02 DMA2

= 0x03 DMA3

= 0x04 - 0x07 No DMA active

CRF0 (Default 0x0E)

FDD Mode Register

Bit 7: FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

= 0 The internal pull-up resistors of FDC are turned on.(Default)

= 1 The internal pull-up resistors of FDC are turned off.

Bit 6: INTVERTZ

This bit determines the polarity of all FDD interface signals.

= 0 FDD interface signals are active low.

= 1 FDD interface signals are active high.

Bit 5: DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4: Swap Drive 0, 1 Mode

= 0 No Swap (Default)

= 1 Drive and Motor select 0 and 1 are swapped.

Bit 3 - 2 Interface Mode

= 11 AT Mode (Default)

= 10 (Reserved)

= 01 PS/2

= 00 Model 30

Bit 1: FDC DMA Mode

= 0 Burst Mode is enabled

= 1 Non-Burst Mode (Default)

Bit 0: Floppy Mode

= 0 Normal Floppy Mode (Default)

= 1 Enhanced 3-mode FDD

CRF1 (Default 0x00)

Bit 7 - 6: Boot Floppy

= 00 FDD A

= 01 FDD B

= 10 FDD C

= 11 FDD D

Bit 5, 4: Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit 3 - 2: Density Select

= 00 Normal (Default)

= 01 Normal

= 10 1 (Forced to logic 1)

= 11 0 (Forced to logic 0)

Bit 1: DISFDDWR

= 0 Enable FDD write.

= 1 Disable FDD write(forces pins WE, WD stay high).

Bit 0: SWWP

= 0 Normal, use WP to determine whether the FDD is write protected or not.

= 1 FDD is always write-protected.

CRF2 (Default 0xFF)

Bit 7 - 6: FDD D Drive Type

Bit 5 - 4: FDD C Drive Type

Bit 3 - 2: FDD B Drive Type

Bit 1 - 0: FDD A Drive Type

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7: Reserved.

Bit 6: Precomp. Disable.

= 1 Disable FDC Precompensation.

= 0 Enable FDC Precompensation.

Bit 5: Reserved.

Bit 4 - 3: DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

= 00 Select Regular drives and 2.88 format

= 01 3-mode drive

= 10 2 Meg Tape

= 11 Reserved

Bit 2: Reserved.

Bit 1:0: DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

Drive Rate Table Select		Data Rate		Selected Data Rate		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0(pin 2)	DRVDEN1(pin 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

7.6 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0x78 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundary (EPP not supported) or

[0x100:0xFF8] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for Parallel Port.

CR74 (Default 0x04)

Bit 7 - 3: Reserved.

Bit 2 - 0: These bits select DRQ resource for Parallel Port.

0x00=DMA0

0x01=DMA1

0x02=DMA2

0x03=DMA3

0x04 - 0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7: Reserved.

Bit 6 - 3: ECP FIFO Threshold.

Bit 2 - 0: Parallel Port Mode (CR28 PRTMODS2 = 0)

= 100 Printer Mode (Default)

= 000 Standard and Bi-direction (SPP) mode

= 001 EPP - 1.9 and SPP mode

= 101 EPP - 1.7 and SPP mode

= 010 ECP mode

= 011 ECP and EPP - 1.9 mode

= 111 ECP and EPP - 1.7 mode.

7.7 Logical Device 2 (UART A)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x04 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00)

Bit 7 - 2: Reserved.

Bit 1 - 0: SUACLKB1, SUACLKB0

= 00 UART A clock source is 1.8462 Mhz (24MHz/13)

= 01 UART A clock source is 2 Mhz (24MHz/12)

= 10 UART A clock source is 24 Mhz (24MHz/1)

= 11 UART A clock source is 14.769 Mhz (24mhz/1.625)

7.8 Logical Device 3 (UART B)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x02, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x03 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 2.

CRF0 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3: RXW4C

= 0 No reception delay when SIR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2: TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 - 0: SUBCLKB1, SUBCLKB0

= 00 UART B clock source is 1.8462 Mhz (24MHz/13)

= 01 UART B clock source is 2 Mhz (24MHz/12)

= 10 UART B clock source is 24 Mhz (24MHz/1)

= 11 UART B clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (Default 0x00)

Bit 7: Reserved.

Bit 6: IRLOCSEL. IR I/O pins' location select.

= 0 Through SINB/SOUTB.

= 1 Through IRRX/IRTX.

Bit 5: IRMODE2. IR function mode selection bit 2.

Bit 4: IRMODE1. IR function mode selection bit 1.

Bit 3: IRMODE0. IR function mode selection bit 0.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	high
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

Bit 2: HDUPLX. IR half/full duplex function select.

= 0 The IR function is Full Duplex.

= 1 The IR function is Half Duplex.

Bit 1: TX2INV.

= 0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

= 1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0: RX2INV.

= 0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.

= 1 inverse the SINB pin of UART B function or IRRX pin of IR function

7.9 Logical Device 6 (CIR)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select CIR I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for CIR.

7.10 Logical Device 7 (Game Port GPIO Port 1)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activate Game Port./GP1

= 0 Game Port/GP1 is inactive.

CR60, CR 61 (Default 0x02, 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the Game Port base address [0x100:0xFFF] on 8 byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select the GPIO1 base address [0x100:0xFFF] on 1 byte boundary

IO address : CRF1 base address

CRF0 (GP10-GP17 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP10-GP17 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

7.11 Logical Device 8 (MIDI Port and GPIO Port 5)

CR30 (MIDI Port Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 MIDI/GP5 port is Activate

= 0 MIDI/GP5 port is inactive.

CR60, CR 61 (Default 0x03, 0x30 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the MIDI Port base address [0x100:0xFFF] on 2byte boundary.

CR62, CR 63 (Default 0x00, 0x00)

These two registers select the GPIO5 base address [0x100:0xFFF] on 4byte boundary.

IO address : CRF1 base address

IO address + 1: CRF3 base address

IO address + 2 : CRF4 base address

IO address + 3 : CRF5 base address

CR70 (Default 0x09 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for MIDI Port.

RF0 (GP5 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP5 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP5 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (PLED mode register. Default 0x00)

Bit 7 ~ 3 : Reserved .

Bit 2: select WDTO# count mode.

= 0 second

= 1 minute

Bit 1 ~ 0: select PLED mode

= 00 Power LED pin is tri-stated.

= 01 Power LED pin is droved low.

= 10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle.

= 11 Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

CRF4 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit 7 - 0:

= 0x00 Time-out Disable

= 0x01 Time-out occurs after 1 second/minute

= 0x02 Time-out occurs after 2 second/minutes

= 0x03 Time-out occurs after 3 second/minutes

.....

= 0xFF Time-out occurs after 255 second/minutes

CRF5 (Default 0x00)

Bit 7 ~ 6 : Reserved .

Bit 5: Force Watch Dog Timer Time-out, Write only*

= 1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 4: Watch Dog Timer Status, R/W

= 1 Watch Dog Timer time-out occurred.

= 0 Watch Dog Timer counting

Bit 3 -0: These bits select IRQ resource for Watch Dog. Setting of 2 selects SMI.

7.12 Logical Device 9 (GPIO Port 2 ~ GPIO Port 4)

CR30 (Default 0x00)

Bit 7 ~ 3: Reserved.

Bit 2: = 1 Activate GPIO4.

= 0 GPIO4 is inactive

Bit 1: = 1 Activate GPIO3.

= 0 GPIO3 is inactive

Bit 0: = 1 Activate GPIO2.

= 0 GPIO2 is inactive.

CR60, 61(Default 0x00, 0x00).

These two registers select the GP2,3,4 base address(0x100:FFE) ON 3 bytes boundary.

IO address: : CRF1 base address

IO address + 1 : CRF3 base address

IO address + 2 : CRF7 base address

CRF0 (GP2 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP2 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP2 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (GP3 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF4 (GP3 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF5 (GP3 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF6 (GP4 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF7 (GP4 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF8 (GP5 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

7.13 Logical Device A (ACPI)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.
= 0 Logical device is inactive.

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resources for $\overline{SMI}/\overline{PME}$

CRE0 (Default 0x00)

Bit7 : ENCIRWAKEUP. Enable CIR to wake-up system.
= 0 Disable CIR wake up function
= 1 Enable CIR wake up function

Bit 5 : CIR_STS. This bit is cleared by reading 1 this register.
= 0 Disable
= 1 Enable

Bit6, 4 ~ 0 : Reserved

CRE 1 (Default 0x00) CIR wake up index register

The range of CIR wake up index register is 0x20 ~ 0x2F.

CRE 2 CIR wake up data register

This register holds the value of wake up key register indicated by CRE1. This register can be read/written.

CRE5 (Default 0x00)

Bit 7 : Reserved

Bit 6 ~ 0 :Compared Code Length . When the compared codes are storage in the data register, these data length should be written to this register.

CRE6 (Default 0x00)

Bit 7 - 6: Reserved.

Bit 5 - 0: CIR Baud Rate Divisor. The clock base of CIR is 32khz, so that the baud rate is 32khz divided by (CIR Baud Rate Divisor + 1).

CRE7 (Default 0x00)

Bit 7 - 3: Reserved.

Bit 2:Reset CIR Power-On function. After using CIR power-on, the software should write logical 1 to restart CIR power-on function.

Bit 1: Invert RX Data.

= 1 Inverting RX Data.

= 0 Not inverting RX Data.

Bit 0: Enable Demodulation.

= 1 Enable received signal to demodulate.

= 0 Disable received signal to demodulate.

CRF0 (Default 0x00)

Bit 7: CHIPPME. Chip level auto power management enable.

= 0 disable the auto power management functions

= 1 enable the auto power management functions.

Bit 6: CIRPME. Consumer IR port auto power management enable.

= 0 disable the auto power management functions

= 1 enable the auto power management functions.

Bit 5: MIDIPME. MIDI port auto power management enable.

= 0 disable the auto power management functions

= 1 enable the auto power management functions.

Bit 4: Reserved. Return zero when read.

Bit 3: PRTPME. Printer port auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

Bit 2: FDCPME. FDC auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

Bit 1: URAPME. UART A auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

Bit 0: URBPME. UART B auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

CRF1 (Default 0x00)

Bit 7: WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.

= 0 the chip is in the sleeping state.

= 1 the chip is in the working state.

Bit 6 - 5: Devices' trap status.

Bit 4: Reserved. Return zero when read.

Bit 3 - 0: Devices' trap status.

CRF3 (Default 0x00)

Bit 7 ~ 4: Reserved. Return zero when read.

Bit 3 ~ 0: Device's IRQ status.

These bits indicate the IRQ status of the individual device respectively. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 3: PRTIRQSTS. printer port IRQ status.

Bit 2: FDCIRQSTS. FDC IRQ status.

Bit 1: URAIRQSTS. UART A IRQ status.

Bit 0: URBIRQSTS. UART B IRQ status.

CRF4 (Default 0x00)

Bit 7 ~ 4: Reserved. Return zero when read.

Bit 3 ~ 0: These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a1. Writing a 0 has no effect.

Bit 3: HMIRQSTS. Hardware monitor IRQ status.

Bit 2: WDTIRQSTS. Watch dog timer IRQ status.

Bit 1: CIRIRQSTS. Consumer IR IRQ status.

Bit 0: MIDIIRQSTS. MIDI IRQ status.

CRF6 (Default 0x00)

Bit 7 ~ 4: Reserved. Return zero when read.

Bit 3 ~ 0: Enable bits of the $\overline{PME}$/$\overline{SMI}$ generation due to the device's IRQ.

These bits enable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to any IRQ of the devices.

$\overline{SMI}$/$\overline{PME}$ logic output = (PRTIRQEN and PRTIRQSTS) or (FDCIRQEN and FDCIRQSTS) or (URAIRQEN and URAIRQSTS) or (URBIRQEN and URBIRQSTS) or

(HMIRQEN and HMIRQSTS) or (WDTIRQEN and WDTIRQSTS) or

(IRQIN3EN and IRQIN3STS) or (IRQIN2EN and IRQIN2STS) or

(IRQIN1EN and IRQIN1STS) or (IRQIN0EN and IRQIN0STS)

Bit 3: PRTIRQEN.

= 0 disable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to printer port's IRQ.

= 1 enable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to printer port's IRQ.

Bit 2: FDCIRQEN.

= 0 disable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to FDC's IRQ.

= 1 enable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to FDC's IRQ.

Bit 1: URAIRQEN.

= 0 disable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to UART A's IRQ.

= 1 enable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to UART A's IRQ.

Bit 0: URBIRQEN.

= 0 disable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to UART B's IRQ.

= 1 enable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to UART B's IRQ.

CRF7 (Default 0x00)

Bit 7 ~ 4: Reserved. Return zero when read.

Bit 3 ~ 0: Enable bits of the $\overline{SMI}$/$\overline{PME}$ generation due to the GPIO IRQ function or device's IRQ.

Bit 3: HMIRQEN.

= 0 disable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to hardware monitor's IRQ.

= 1 enable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to hardware monitor's IRQ.

Bit 2: WDTIRQEN.

= 0 disable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to watch dog timer's IRQ.

= 1 enable the generation of an $\overline{SMI}$/$\overline{SMI}$ interrupt due to watch dog timer's IRQ.

Bit 1: CIRIRQEN.

= 0 disable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to CIR's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to CIR's IRQ.

Bit 0: MIDIIRQEN.

= 0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

= 1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

CRF9 (Default 0x00)

Bit 7 - 3: Reserved. Return zero when read.

Bit 2: PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

= 0 the power management events will generate an $\overline{SMI}$ event.

= 1 the power management events will generate an $\overline{PME}$ event.

Bit 1: FSLEEP: This bit selects the fast expiry time of individual devices.

= 0 1 S

= 1 8 mS.

Bit 0: SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

= 0 neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

= 1 an $\overline{SMI}$ or $\overline{PME}$ event will be generated.

7.14 Logical Device B (Hardware Monitor)

CR30 (Default 0x00)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select Hardware Monitor base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Hardware Monitor.

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (5V)	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
RTC Battery Voltage V_{BAT}	2.2 to 4.0	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 DC Characteristics

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	I_{BAT}			2.4	uA	V_{BAT} = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	I_{BAT}			2.0	mA	V_{SB} = 5.0 V, All ACPI pins are not connected.
I/O_{8t} - TTL level bi-directional pin with 8mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12t} - TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{24t} - TTL level bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12ts} - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24ts} - TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 Ma

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24tsp3} – 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{12t} - TTL level bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{24t} - TTL level bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
$I/OD24_c$ - CMOS level bi-directional pin and open drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{24a} - Bi-directional pin with analog input and open-drain output with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12cs} - CMOS level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD16$_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD24$_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD12$_{csd}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD12$_{csu}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O_4 - Output pin with 4mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
O_8 - Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
O_{12} - Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{16} - Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA
O_{24} - Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} - 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{24p3} - 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD_8 - Open drain output pin with 8mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
OD_{12} - Open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} - 3.3V open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

DC Characteristics, continued

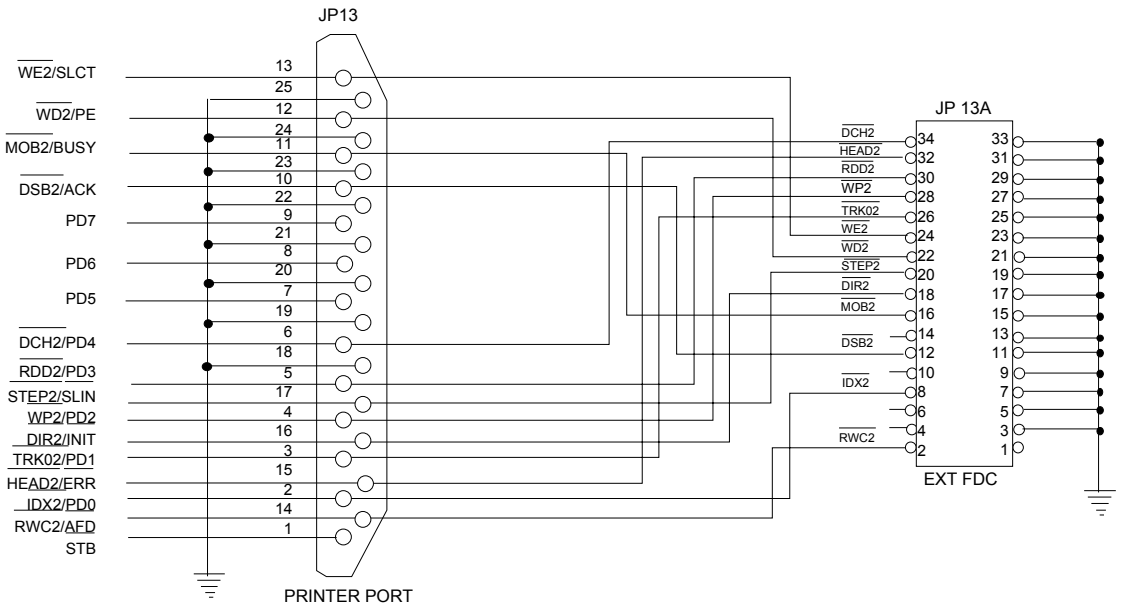
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tp3} - 3.3V TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{td} - TTL level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tu} - TTL level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	V_{DD} = 5 V
Hystersis	V_{TH}	0.8	1.0		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp3} - 3.3 V TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.8	1.0		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_c - CMOS level input pin						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{cu} - CMOS level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{cd} - CMOS level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{cs} - CMOS level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{csu} - CMOS level Schmitt-trigger input pin with internal pull up resistor						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

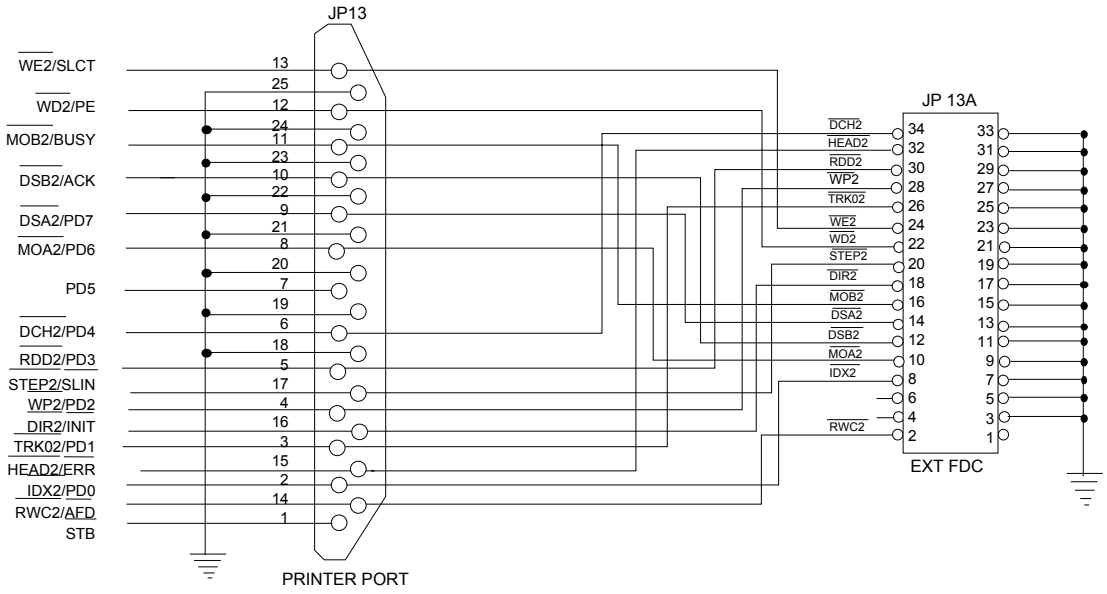
9. APPLICATION CIRCUITS

9.1 Parallel Port Extension FDD



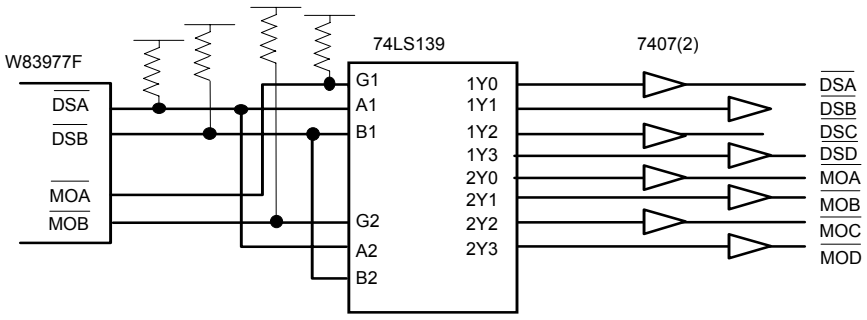
Parallel Port Extension FDD Mode Connection Diagram

9.2 Parallel Port Extension 2FDD



Parallel Port Extension 2FDD Connection Diagram

9.3 Four FDD Mode

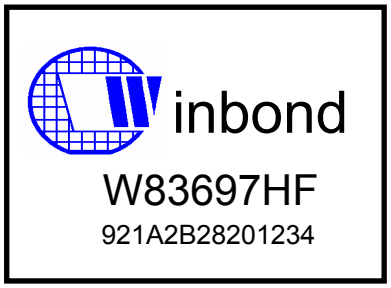


10. ORDERING INSTRUNCTION

PART NO.	PACKAGE	REMARKS
W83697HF	128-pin QFP	

11. HOW TO READ THE TOP MARKING

Example: The top marking of W83697HF

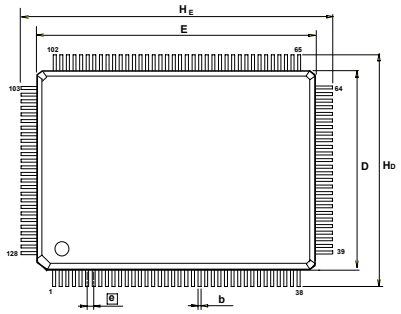


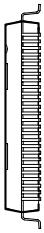
1st line: Winbond logo
2nd line: the type number: W83697HF
3th line: the tracking code 921 A 2 C 28201234

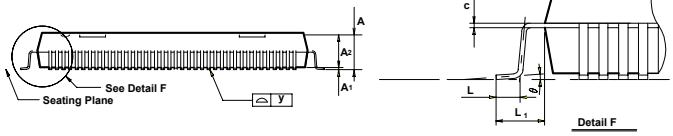
821: packages made in '98, week 21
A: assembly house ID; A means ASE, S means SPIL.... etc.
2: Winbond internal use.
B: IC revision; A means version A, B means version B
282012345: wafer production series lot number

12. PACKAGE DIMENSIONS

(128-pin PQFP)





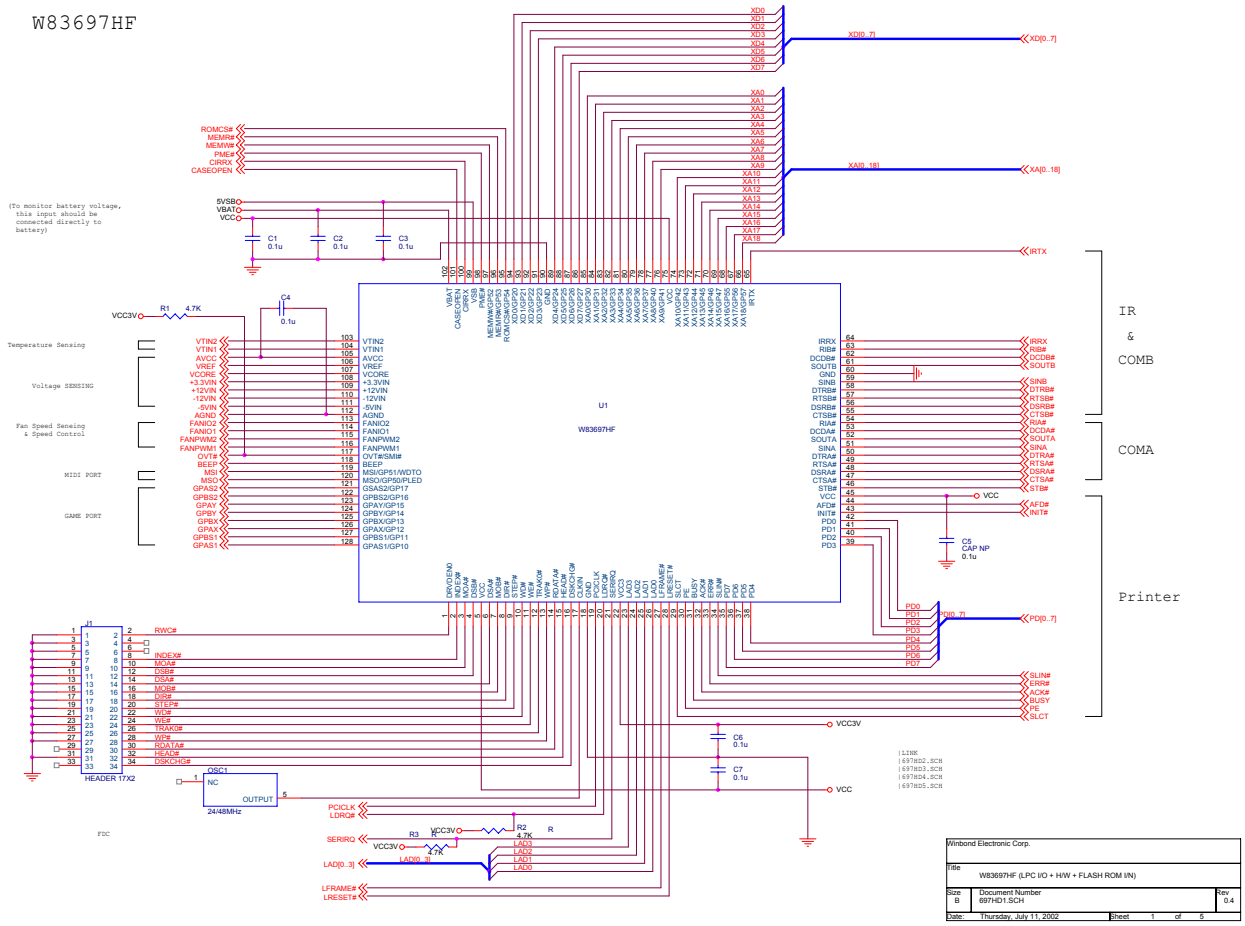


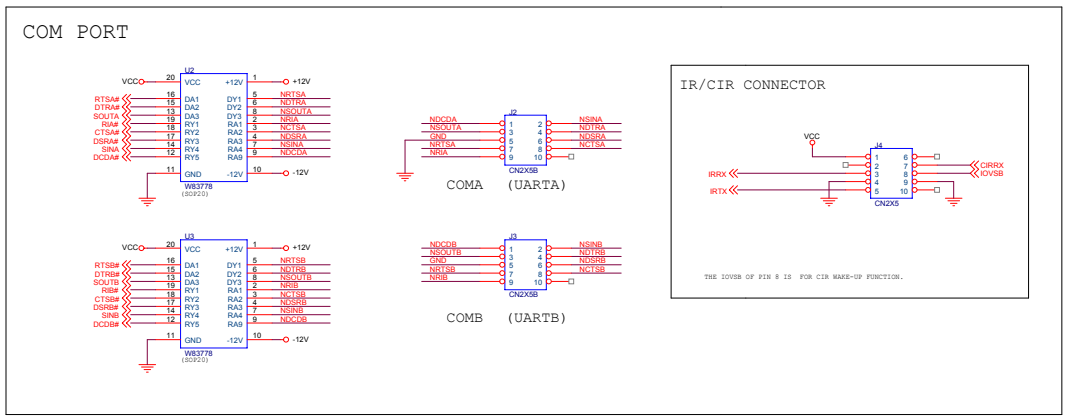
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

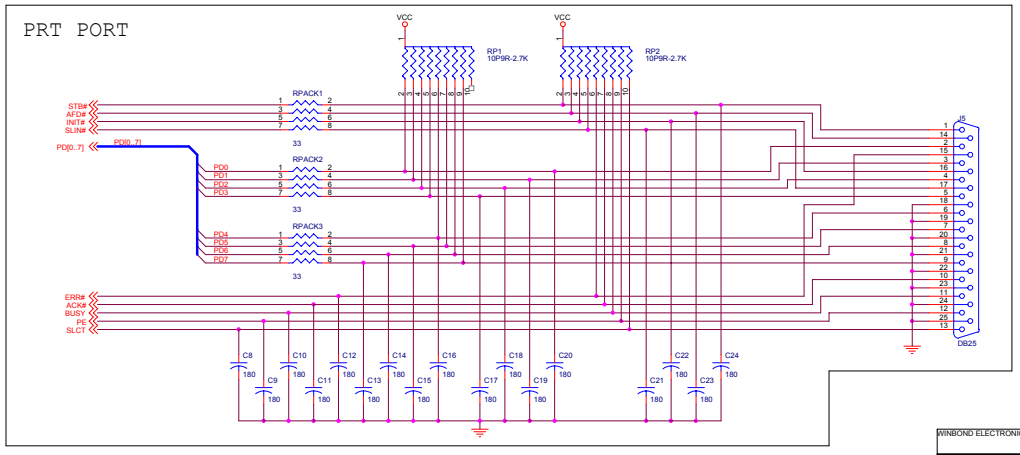
Note:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

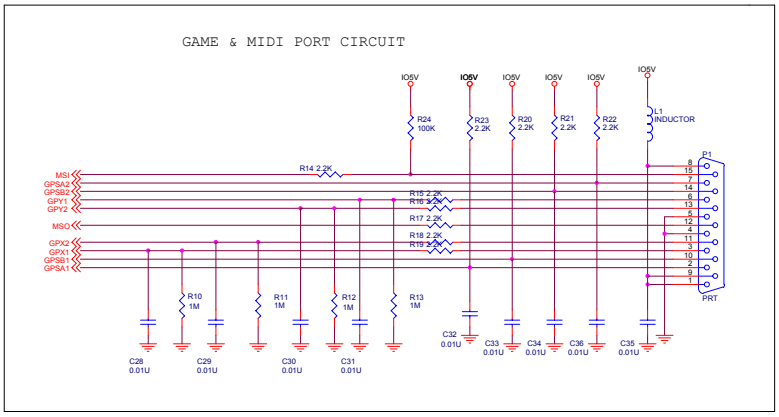
13. APPENDIX A: DEMO CIRCUIT

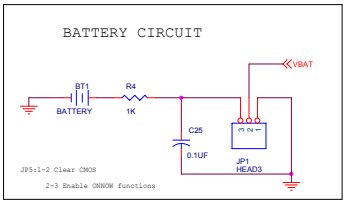


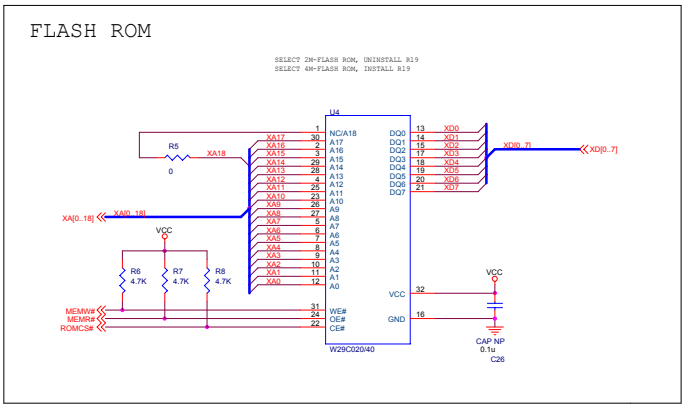


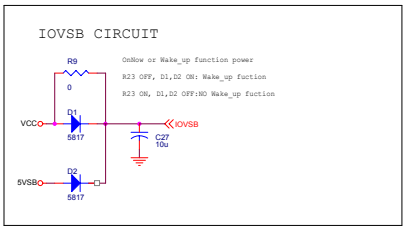


WINBOND ELECTRONICS CORP.		
Title: W83697HF (LPC I/O + H/W + FLASH ROM I/F)		
Size: B	Document Number: 697HD2.SCH	Rev: 0.4
Date: Thursday, July 11, 2002	Sheet 2 of 5	









WINBOND ELECTRONICS CORP.		
Title: W83697HF (LPC I/O + H/W + FLASH ROM I/F)		
Size: B	Document Number: 697HD3.SCH	Rev: 0.4
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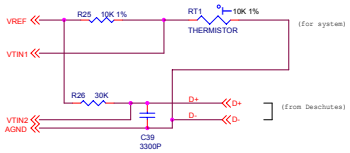
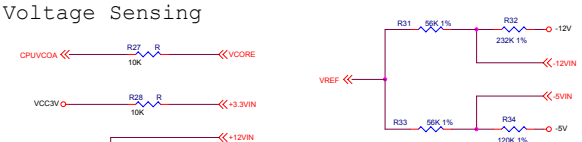
Hardware Monitor circuits

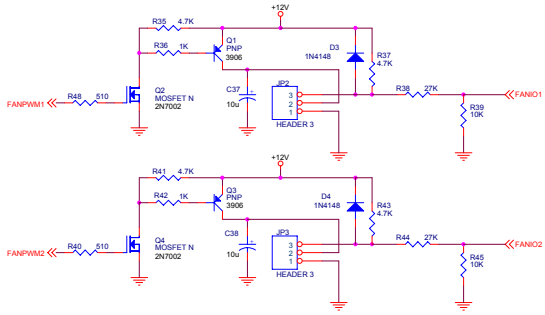
Temperature Sensing



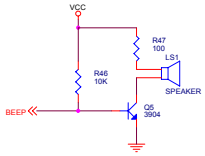
Voltage Sensing

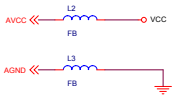


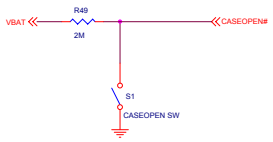
PWM Circuit for FAN speed control



Beep Circuits







Winbond Electronic Corp.			
Title: W83697HF (LPC I/O+ H/W + FLASH ROM I/F)			
Size: B	Document Number: 697HD4.SCH		Rev: 0.4
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The version 0.1 is first schematics for W83697HF

The version 0.2 change

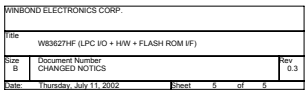
1.update 697's library

2.The sheet 4 in Case open block,part 74HC14 is U4A & U4B changed to U5A & U5B

The version 0.3 chage

1.Case-Open circuit(in page 4)

The version 0.4 chage
add a pull high resistor 100K in midiin(in page 3)



REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.40	08/23/99	N.A.	First published. For Beta Site customers only
0.41	11/15/99	98, 107, 116	H/W monitor register correction
0.50	11/15/00	All	New composition
1.0	12/17/02		New update
1.1	02/18/03	5, 6	Add Block Diagram
1.2	June 24, 2003	1.P7 2.P17~18 3.P74 4.P99	1. Add pin buffer type description of OD8. 2. Update the functional description of Pin117~126. 3. Update the chip control register CR29 4. Add VOH of O12p3, O24p and OD8 description in DC specication 5. The pin name DTO" were replaced by DTO#" 6 H/W monitor data correction
2.0	April 14, 2005	98	ADD Important Notice

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