COMPENSATING THE FEEDBACK LOOP FOR THE Si3400 AND Si3401

1. Introduction

The Si3400 and Si3401 reference designs are available for many output voltages (e.g., 3.3, 5, 9, 12 V) and output capacitor types. In general, Silicon Laboratories strongly recommends using these standard designs to minimize risk and ensure robust performance. Refer to the design databases posted on the Si3400/01 documentation page on the Silicon Labs website for more information:

- EVB Data Sheets
  - Si3400-EVB
  - Si3401-EVB
  - Si3400ISO-EVB
  - Si3401ISO-EVB
- EVB Reference Design Databases (Schematics and Layout)
  - Si3400-EVB
  - Si3401-EVB
  - Si3400ISO-EVB
  - Si3401ISO-EVB

However, some designers may want to consider other cases of output filtering, input filtering, inductors, etc. for a variety of reasons (cost, footprint, availability, etc.).

While it would be desirable to use circuit simulation to optimize the feedback loop, it is very difficult to get reliable information about important factors such as capacitor ESR. Also, the stabilizing effect of the input side hot-swap switch and input filter ESR must be taken into account, which is not straightforward for commonly available SPICE implementations. For these reasons, the feedback loop must be experimentally optimized if a known reference design is not used.

The application note outlines the general process for compensating the feedback loop experimentally. In case a predefined compensation and output filter is not used, it is strongly recommended that this procedure be followed to ensure robust performance.

1.1. Breaking the feedback loop

The feedback loop is broken and a transformer is used to inject an ac signal across the break. Using a transformer allows the loop stability to be measured in a closed loop system with whatever load a filtering is present. The loop is broken at the output and at the point sensing the output voltage. The transformer ac and dc impedance must be small compared to the impedance sensing the output voltage.

Figures 1 and 2 show the recommended transformer placement for the non-isolated and isolated reference designs.

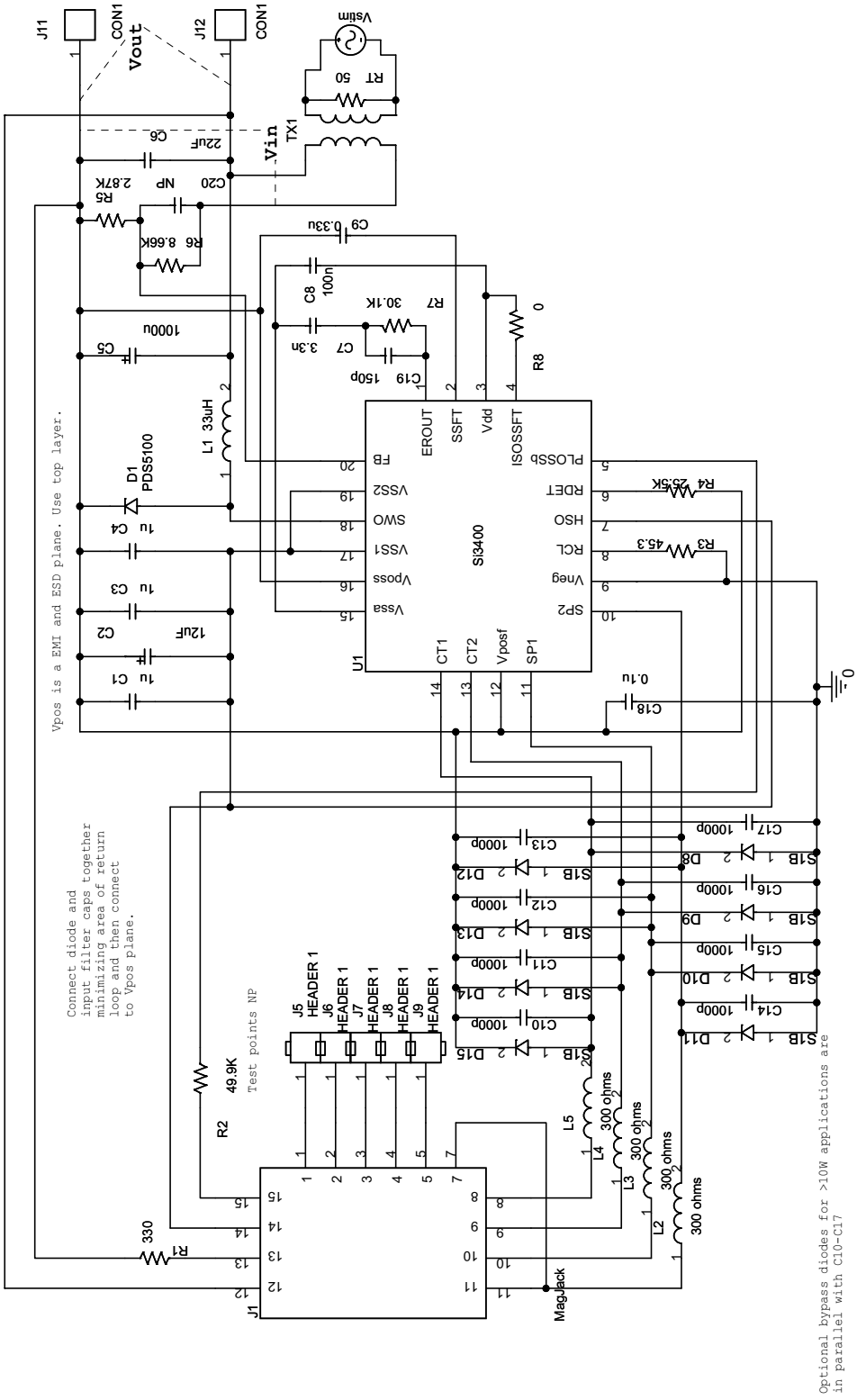

Figure 1. Non-Isolated

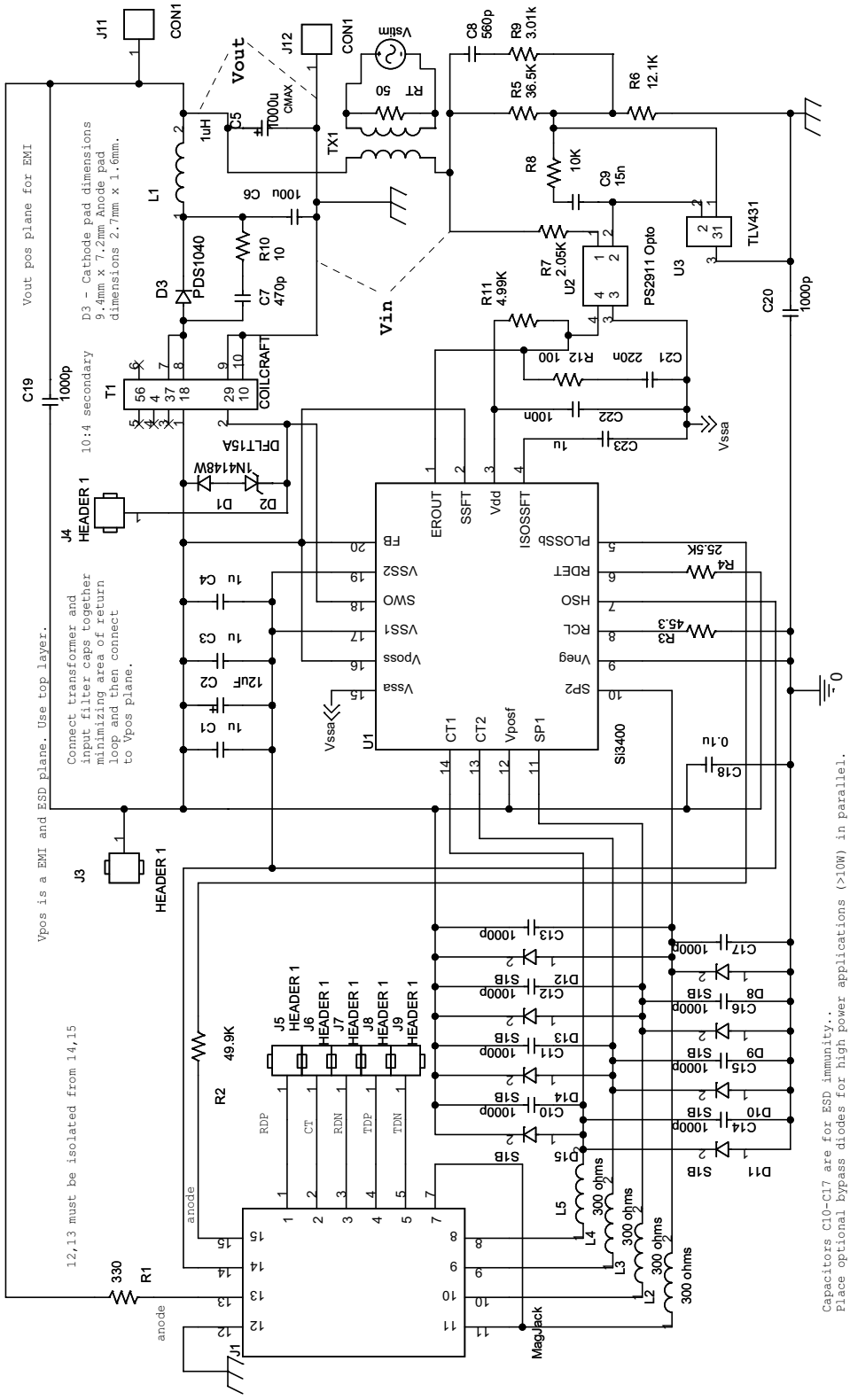

Figure 2. Isolated

A commercially available phase gain meter optimized for power supply analysis is available from Venable Inc. The Venable meter can be used with an injection transformer from Venable, or an ordinary transformer can be used as long as it keeps a low ac and dc impedance.

Good results have also been achieved with a Bode 100 phase gain meter from Omicron Labs and using Coilcraft BU15-7521ROBL common mode choke hooked up as a transformer (input on 1,2 output on 3,4). When terminated with a 50 Ω resistor on the input side, this transformer gives <100 Ω impedance on the output side from dc to well over 10 MHz insuring that the transformer itself does not impact the feedback loop.

Other phase gain meters can be used as long as they are capable of operating in the 100 Hz to 40 kHz range of interest and have a provision for high impedance (1 MΩ) probes.

The phase-gain meter is used to measure the output voltage response to the input voltage that is stimulated by the transformer (see Figure 3). The magnitude and phase of the voltage (V_{STIM}) that the transformer produces is not critical. It should be large enough that the signals can be measured but not so large that there is distortion. In practice, a signal level of –20 to –30 dBm (50 Ω reference) has been found to be satisfactory.

The magnitude and phase of the ratio of the output voltage the input voltage is what needs to be measured to examine loop stability. In general it is good practice to have at least 50 degrees of phase margin when the gain is unity (zero dB) and 10 dB of gain margin when the phase reaches zero degrees.

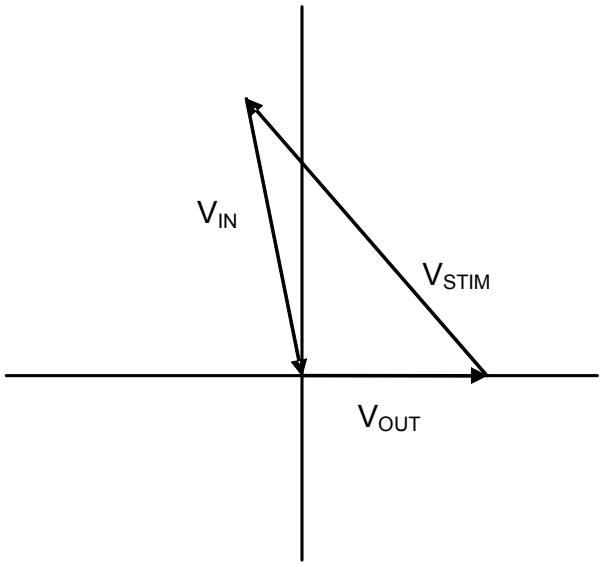

Figure 3. Phase and Gain of VOUT with Respect to VIN

Experimental results for the standard isolated and non-isolated reference designs are shown in Figures 4 and 5 (see also AN296).

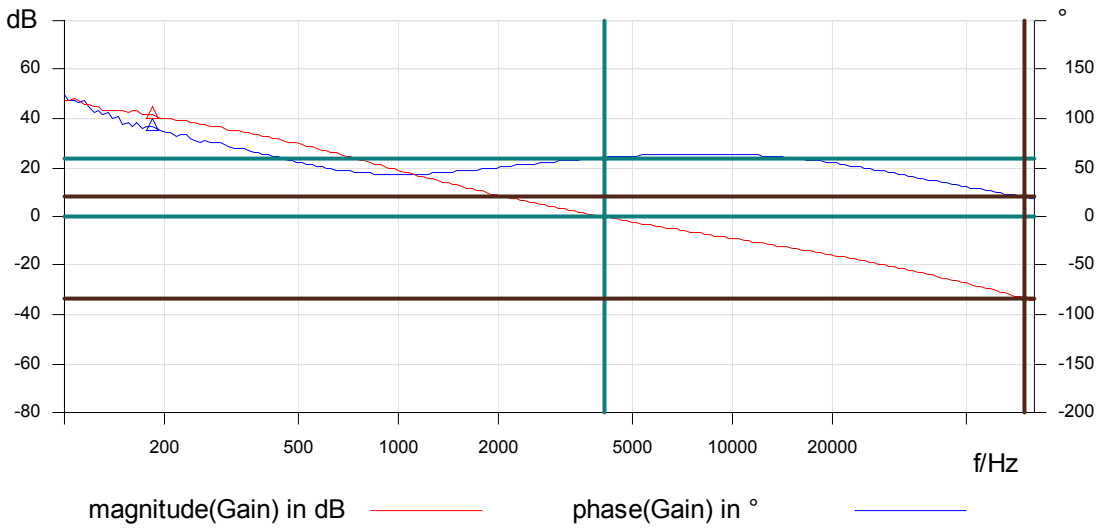

Figure 4. Gain and Phase for Non-Isolated Design

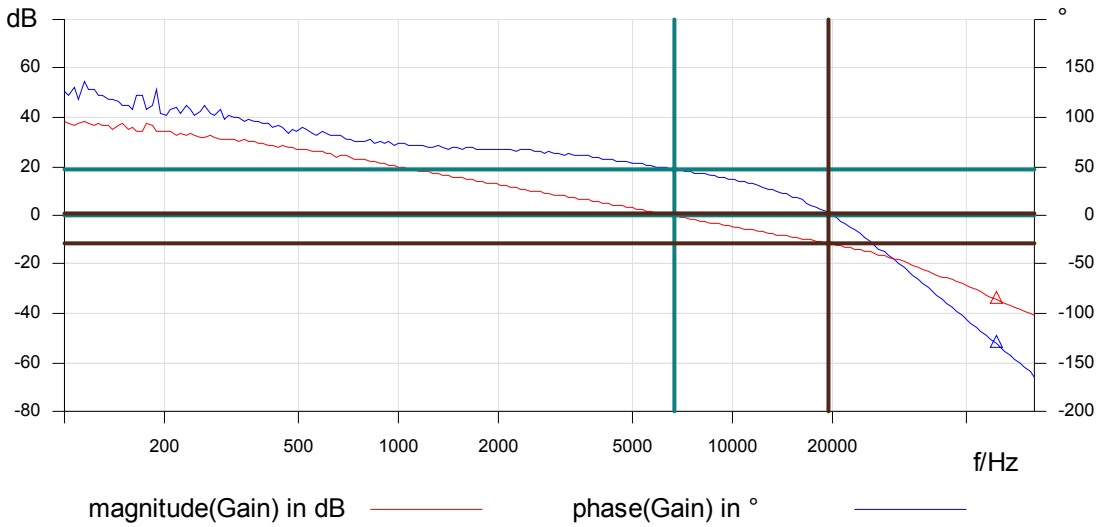

Figure 5. Gain and Phase of Isolated Design

1.2. Optimizing the feedback loop

Generally, the feedback loop should be checked over the entire input voltage and load range. In practice, the maximum input voltage and maximum load is generally the worst case corner. Building in some margin for gain and phase allows for variation in components and temperature. In the case of the isolated design, a gain sorted opto-coupler should be used to avoid a lot of gain variation from the opto-coupler. Also, for designs that operate at very low (–40 °C) temperature and use electrolytic capacitors in the filter path, it is desirable to check at low temperature because electrolytic capacitors have substantial variation in ESR at low temperature.

A low or negative gain and phase margin can give power supply output oscillation and the feedback loop crossover frequency should be reduced. An excessively large gain and phase margin means that better transient response could be obtained by increasing the crossover frequency.

For the non-isolated design, the dominant pole is set by C7. A zero is introduced by R7-C7, and an optional second zero is introduced by C20-R6. The zeros in the transfer function are used to compensate for the poles introduced by the output filter and extend the frequency response of the feedback loop. The R7-C7 zero should be placed at somewhat less than the desired loop bandwidth in order to contribute the most phase boost. For example, in the

non-isolated reference design the R7-C7 zero is at 1.6 kHz and the loop bandwidth is about 4 kHz. C19 introduces a final pole which is required to filter noise that can be coupled to the ERout node. If used, the C20-R6 zero is placed at about the loop bandwidth (not below) so as to maximize the phase boost prior to the pole from C20-R5// R6.

The optimization process for the non-isolated design is as follows:

1. R5 and R6 are fixed to set the desired output voltage (see http://www.silabs.com/public/documents/tpub_doc/othertpubs/Wireline/High_Voltage/en/Si3400SwitcherCalcs.xls
2. Vary C7 to move the crossover frequency up and down.
3. R7 is increased to reduce the C7-R7 zero to 1/2 to 1/3 of the loop bandwidth.
4. If used, C20 is set so that C20-R6 is equal to the loop bandwidth.
5. If the phase margin and gain margin are too big or too small go back to step 2 and change C7 up (not enough margin) or down (too much margin and not enough bandwidth).

For the isolated design, the C21-R11 pole compensates the zero introduced by C9 and R8+R6//R5. Therefore, the zeros of concern for loop stability are C21-R12 and C8-R5. As in the non-isolated design these zeros (in this case 7.8 kHz and 7.2 kHz) are placed at around the desired loop bandwidth (7 kHz) so as to maximize the phase boost. In this case both zeros are placed near the loop bandwidth because it is desirable to minimize R12 to reduce noise at ERout.

The optimization process for the isolated design is as follows:

1. R5 and R6 are fixed to set the desired output voltage (see http://www.silabs.com/public/documents/tpub_doc/othertpubs/Wireline/High_Voltage/ R8 is set to 10 kΩ, R11 is set to 4.99 kΩ and R7 is set according to the output voltage (1 kΩ at 3.3 V 2.05 kΩ at 5 V and 4.99 kΩ at 9 or 12 V for example). R9 is generally set to approximately 3.01 kΩ.
2. Vary C9 and C21 to move the crossover frequency up and down. Generally, C9 and C11 are kept as a ratio and C9 is < 1/4 of C21.
3. R12 is increased so that R12 x C21 is less than or equal to the loop bandwidth subject to the constraint that R12 <1K to filter any noise at ERout.
4. C8 is increased so that C8 x R5 is approximately equal to the loop bandwidth.
5. If the phase margin and gain margin are too big or too small, go back to step 2 and change C9 and C21 (in the same ratio) up (not enough margin) or down (too much margin and not enough bandwidth).

2. Conclusions

To ensure robust performance in cases where a predefined compensation and output filter are not used, the application note outlines the general process required for experimentally compensating the Si3400/01 feedback loop.

Refer to the Si3400/01 Evaluation Board User's Guides and reference designs for complete schematics for common output voltages and output filter configurations.

NOTES:

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