



Technical Reference Note (APC08)

Centauri (APC08) Non-Isolated DC/DC Power Module

The Centauri (APC08) DC-DC Power Module is a high efficiency non-isolated buck converter designed for use in a wide variety of applications. It works from a wide input voltage range of 1.8V to 6V or 5V to 13V and offers an extensive array of output voltages starting from 0.9V to 3.6V (up to 6V in some flavors). Through careful layout and component selection it achieves the highest efficiency/load in the smallest footprint available in the market today. It is ideal for Point of Load applications and provides the most flexibility for the ever-changing DSP and ASIC power requirements.



Industry Standard
0.53 X 1.3 X 0.29H SMT Package

Special Features

- Point of load (POL) applications
- High efficiency, 3.3V@93% Typ
- -40°C to +85°C Ambient Operating Temperature
- Open Frame SMT
- Positive enable function
- Low output ripple and noise
- Regulation to zero load
- Programmable Output from 0.9V to 3.6V (External Trim Resistor)
- Fixed frequency switching (400 KHz)
- Power Good Signal (Optional)
- Active Current share (Optional)

Environmental Specifications

- Operating temperature: -40°C to +85°C
- Storage temperature: -40°C to +125°C
- MTBF: >3.3 million hours

Electrical Parameters

Input

Input range 1.8-6.0VDC and 5.0-13.0VDC
Efficiency 3.3V @ 93% Typ

Control

Enable TTL compatible (Positive Logic)

Output

Regulation (Line, Load, Temp) <3%

Ripple and noise 75mV - (³2.5V Output)
50mV - (<2.5V Output)

Output voltage adjust range 0.9V to 3.6V (J Version)
Transient Response 5% max deviation with
50% to 75% full load
500 μS (max) recovery

Safety

Designed to meet:
UL, cUL 60950 Recognized
TUV EN60950 Licensed





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APC08 SERIES

THIS SPECIFICATION COVERS THE REQUIREMENTS

For A New 1.3" X 0.53" X 0.33"(H) Maximum 28W Single Output High efficiency Non-Isolated SMT DC-DC Converter

MODEL NAME	Vin nominal/ Vin range	Vout/Iout
APC08J03	3.3V / 1.8-6.0V	0.9V, 8A
APC08K03	3.3V / 1.8-6.0V	1.2V, 8A
APC08M03	3.3V / 1.8-6.0V	1.5V, 8A
APC08Y03	3.3V / 2.2-6.0V	1.8V, 8A
APC08G03	3.3V / 3.0-6.0V	2.5V, 8A
APC08F03	5.0V / 4.0-6.0V	3.3V, 8A
APC08J08	8V / 5.0-12.0V	0.9V, 8A
APC08K08	8V / 5.0-12.0V	1.2V, 8A
APC08M08	8V / 5.0-12.0V	1.5V, 8A
APC08Y08	8V / 5.0-12.0V	1.8V, 8A
APC08G08	8V / 5.0-12.0V	2.5V, 8A
APC08F08	8V / 5.0-12.0V	3.3V, 8A
APC05A08	8V / 5.0-12.0V	5V, 5A
APC04S08	8V / 5.0-12.0V	6V, 4A

Options (suffix):

"-9" = Trim

"-9MA" = Trim with Power Good and Active Current Share

"-J" = Jedec tray-type packaging

"W" = Improved Loop Bandwidth / Transient Response (only for APC08x03 series)



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Electrical Specifications

STANDARD TEST CONDITION on a single unit, unless otherwise specified.

T _A :	25°C (Ambient Air)	
V _{in} (P1):	APC08x03	+1.8V to +6.0V
	APC08x08	+5.0V to +13V
Enable (P5):	Open	
V _o (P2):	Connect to load	
Gnd (P3):	Return for V _{in} and V _o	
Trim (P4):	Open	
PGood (P6):	Open	
P (P7):	Open	

ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or in any other conditions in excess of those given in the operational sections of the specs. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Device	Symbol	Min	Typ	Max	Unit
Input Voltage						
Continuous	03	V _{IN}	1.8	-	6.0	Vdc
Transient (100ms)	03	V _{IN,trans}	-	-	7.0	Vdc
Continuous	08	V _{IN}	5.0	-	13.0	Vdc
Transient (100ms)	08	V _{IN,trans}	-	-	14.0	Vdc
Operating Temperature	All	T _A	-40	-	85	°C
Storage Temperature	All	T _{STG}	-40	-	125	°C
Operating Humidity	All	-	-	-	85	%

INPUT SPECIFICATIONS

Parameter	Device	Symbol	Min	Typ	Max	Unit
Operating Input Voltage ¹	03	V _{IN}	1.8	3.3	6.0	Vdc
	08		5.0	8.0	12.0	Vdc
Maximum Input Current ² (V _{IN} = 0 to V _{IN,max} ; I _O = I _{O,max})	All	I _{IN,max}	-	-	9.0	A
	APC05				6.0	
	APC04				5.0	
Input Ripple Current 5Hz to 20MHz	All	I _{IN-1}	-	200	250	mAp-p

Note: 1. Minimum V_{IN} (03 device) for 1V8, 2V5 and 3V3 versions are 2V2, 3V and 4V respectively. For 08 device, min V_{IN} for 5V and 6V versions are 7.5V_{in} and 8.5V_{in}

2. This power module is not internally fused. The use of an input line fuse (03 Version: GMA-10A; 08 version: GMA-6A Bussman fuses or equivalent) is recommended.



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Electrical Specifications (continued)

OUTPUT SPECIFICATIONS

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Voltage Setpoint ($V_{IN}=V_{IN,min}$ to $V_{IN,max}$ at $I_O=I_{O,max}$) ¹	APC08J03 APC08K03 APC08M03 APC08Y03 APC08G03 APC08F03 APC08J08 APC08K08 APC08M08 APC08Y08 APC08G08 APC08F08 APC05A08 APC04S08	$V_{O,SET}$	0.873 1.164 1.455 1.746 2.425 3.200 0.873 1.164 1.455 1.746 2.425 3.200 4.850 5.820	0.9 1.2 1.5 1.8 2.5 3.3 0.9 1.2 1.5 1.8 2.5 3.3 5.0 6.0	0.927 1.236 1.545 1.854 2.575 3.400 0.927 1.236 1.545 1.854 2.575 3.400 5.150 6.180	Vdc
Output Regulation: Line: $V_{IN}=V_{IN,min}$ to $V_{IN,max}$ Load: $I_O=I_{O,min}$ to $I_{O,max}$ Temp: $T_A=-40$ °C to 85 °C	All All All	- - -	- - -	- - -	0.5 0.5 ±1.5	% % %
Output Ripple and Noise ¹¹ Peak to Peak: 5Hz to 20MHz	≥ 2.5V < 2.5V	- -	- -	- -	75 50	mV _{PK-PK} mV _{PK-PK}
Output Current Range	All 5V 6V	I_O	0 0 0	- - -	8 5 4	A
External Load Capacitance ⁹	Suffix "W" All	- -	- -	- -	5000 500	μF μF
Capacitor ESR	Suffix "W" All	- -	10 100	- -	100 -	mΩ mΩ
Output Current Limit Inception ³	All	I_O	-	11.5	-	A
Output Short Circuit Current ⁴	All	-	-	-	-	
Efficiency $V_{IN}=1.8V$ to 6V ¹ $I_O=8A$ Resistive Load	APC08J03 APC08K03 APC08M03 APC08Y03 APC08G03 APC08F03	η	74 80 83 85 89 90	76 81 86 88 91 93	- - - - - -	%
Switching Frequency	All	-	-	400	-	KHz
Turn-On time (Input to Output) ⁵ $I_O=8A$; $V_{IN}=V_{IN,nom}$	All	-	-	-	50	ms



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Electrical Specifications (continued)

OUTPUT SPECIFICATIONS

Parameter	Device	Symbol	Min	Typ	Max	Unit
Efficiency V _{IN} = 6V to 12V I _O = 8A Resistive Load (5A for 5V _O ; 4A for 6V _O)	APC08J08 APC08K08 APC08M08 APC08Y08 APC08G08 APC08F08 APC05A08 APC04S08		71 75 77 81 85 87 90 91	76 81 84 86 90 92 94 95	- - - - - - - -	
Dynamic Response: Slew Rate	All Suffix "W"	$\Delta I_O / \Delta t$	- -	0.1 1.0	- -	A/ μ s
Load Change: 50%-75% I _{O,max} Peak Deviation Settling time to V _{O,nom}	All All	- -	- -	5 500	10 -	%V _O μ s
Load Change: 50% to 25% I _{O,max} Peak Deviation Settling time to V _{O,nom}	All All	- -	- -	5 500	10 -	%V _O μ s
Output Voltage Overshoot Passive Resistive Full Load	All	-	-	5	-	%V _O

FEATURE SPECIFICATION

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Voltage Adjustment Range ⁶	-9 opt		V _O	-	3.6	V
Module Parallel Capability ¹⁰	-9MA		40	-	60	%I _O
Power Good ⁷ Open Collector max sink current max pull-up voltage	All		- -	- -	5 6	mA V
Condition PG _{LOW} 90% V _{O,SET-MIN} > V _O > 110% V _{O,SET-MAX}	All	PG _{LOW}	0	-	250	m Ω
90% V _{O,SET-MIN} ≤ V _O ≤ 100% V _{O,SET-MAX}	All	PG _{HIGH}	100	-	-	K Ω
Output Enable ⁸ Module ON: Logic High Module OFF: Logic Low Enable source current at Logic Low	All All All		> 4.1 0 -	- - -	14 0.8 60	Vdc Vdc μ A



Electrical Specifications *(continued)*

- Note:
3. This feature is only for module protection and is not intended for customer application. The value is specified at 25C ambient air temperature. For other ambient air temperature, please refer to thermal derating curve to determine corresponding current-limit inception values.
 4. Pulse train with 90 ms period and 1ms pulse width. Average I_{out} equals about zero.
 5. Input to Output Turn-On time is defined as the difference between t_1 and t_2 : where t_1 is the time when the input voltage reaches the minimum V_{IN} ($V_{IN} = V_{IN,MIN}$) and t_2 is the time when the output voltage reaches it's specified range ($V_O = V_{O,SET-Min}$).
 6. There are two methods applicable to be able to trim the output voltage. Please refer to related sections under Feature Specification.
 7. See Figure 6 for PGood configuration
 8. Refer to further notes under Feature Specification for the Enable Pin function.
 9. Check with factory for higher output capacitance loading.
 10. Please refer to "Basic Operation and Features" section on page 11 for additional information on Current sharing.
 11. Output ripple is measured with 470 μ F cap termination on the output.

ISOLATION SPECIFICATION

- The APC08 series are Non Isolated units.

SAFETY APPROVAL

- UL / cUL 60950, and TUV EN60950 - Flammability and temp rise only.



Basic Operation and Features

The APC08 family was designed specifically to address applications where on board distributed power with Point-of-Load Converters (Conversion needed as close to the IC, usually DSP's and ASIC's) is employed. With its wide range input and flexible programmable output, any change in the load becomes very manageable with little to no impact on time to market. All of the converters in this family are buck converters. The APC08x03 versions allow 1.8V to 6V input voltage and the APC08x08 versions allow a 5V to 12V input with 14V max surge.

MODULE PIN ASSIGNMENT

There are 4 to 7 surface mount pins on a Centauri module. The availability of pins from individual modules is relevant to its version / selected option.

PIN #	DESIGNATION	
P1	V _{IN}	Input Voltage
P2	V _O	Output Voltage
P3	GND	Common Ground
P4	TRIM	Output Voltage Adjustment [OPTION]
P5	ENABLE	Output Voltage Enable
P6	PGood	Power Good [OPTION]
P7	P	Load Current Active Sharing [OPTION]

INDUSTRY STANDARD PINOUT

When ordered with no options, the module comes with only 4 pins – Vin, Gnd, Vout and Enable – and is compatible with other leading manufacturer's footprint. The PGood, Active Current Share, and Trim pins are options that can be ordered with any model number. For the optional trim function add a (-9) to the end of the standard part number. For the optional current share and PGood signal in addition to the trim function, add (-9MA) to the end of the part number. Please refer to the Part Number Ordering Scheme section.

Note: When using the trim function, this module offers much more trim flexibility than the competitive footprint and also requires a jumper between the two footprints to be source compatible. Contact Factory for applications note.

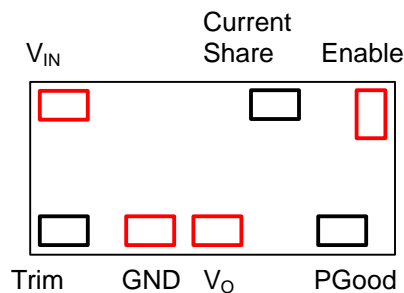


Figure 1. Pin Assignment Viewed from Top of Board.

Typical Application Circuit (Standard Pinout)

Recommended C1 is a low ESR (<100 mohms) 100 μ F tantalum and C2 is a 1 μ F ceramic or equivalent. Recommended output decoupling capacitor C3 for -W models is 22 μ F low ESR ceramic capacitor (at a min). For all other models, C3 can go as low as 1 μ F ceramic capacitor.

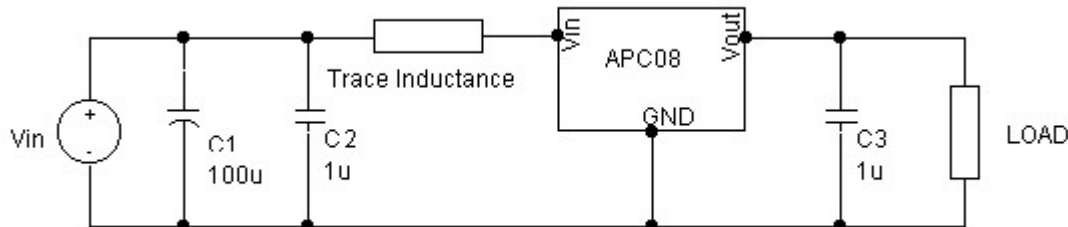


Figure 2. Typical Application Circuit.

Enable Pin (Standard configuration)

Pin P5 is functioned to enable the output voltage of a module. If this pin is left open or connected to > 4.1Vdc up to 14Vdc, the module is turned on. On the other hand, if this pin is connected to ground or to a voltage potential from 0 to 0.8Vdc, the module is turned off. The enable pin can source current up to 60 μ A max - suited for typical open-collector transistors readily available in the market.

For TTL compatibility, Figure 3 shows a 7405 open collector inverter IC utilized to function the Enable feature. Other common chips that can do the function are 74S05; 74HCT05; non-inverting - 7407; 74S07; 74HC07. If SMT packaging is preferred, Fairchild's Tiny Logic NC7SZ05 or TI's Little Logic SN7SLVC1G06 comes in SOT23 or SC70 packages.

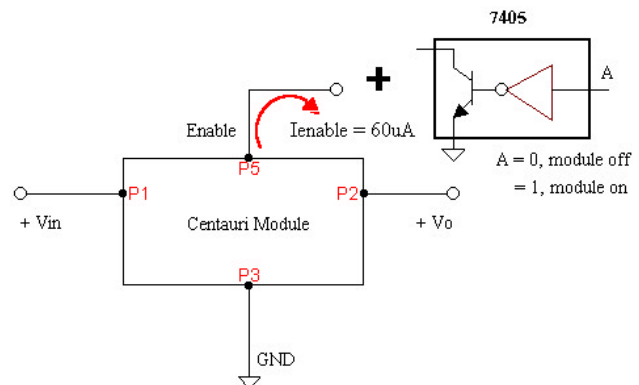


Figure 3. Output Voltage Enable function diagram.

Special Feature Pins (Options):

Trim Function (-9):

Pin P4 is used for output voltage adjustment. The output voltage can be trimmed through an external resistor or through an external DC supply as described in the succeeding sections.

Method 1: External Trim Resistor.

By connecting an external resistor across P4 and P3 (Gnd), the voltage appearing on pin P2 (V_o) is adjusted to a higher value. The output voltage of a module can be adjusted up to a maximum value of 3.3V (nominal) or 83% of the input voltage,

Method 1: External Trim Resistor (*continued*)

whichever is lower. By connecting an external resistor across P4 and P2, V_o is adjusted to a lower value. Only small reductions, 2%, in voltage are recommended, as adjustment to lower voltages tends to affect the loop compensation of the module.

Full range adjustment (from 0.9V to 3.6V) can be obtained from a module with the lowest V_o setpoint (0.9V).

To adjust V_o to a higher value, please refer to Figure 4. The required resistor value (R_t) can be determined through Equation (1) where V_o is the voltage on P2 before the adjustment and V_{ot} is the voltage of P2 after R_t is connected.

$$R_t = \frac{V_{ref}}{V_{ot} - V_o} R_1 \quad \text{Equation (1)}$$

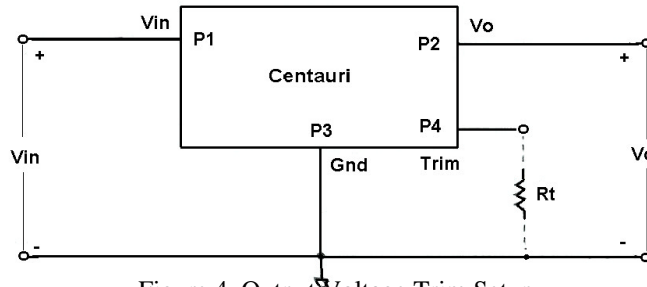


Figure 4. Output Voltage Trim Setup.

Please refer to related constants given in TABLE 1 to calculate the Equation.

TABLE 1. CONSTANTS

	Version	0.9V	1.2V	1.5V	1.8V	2.5V	3.3V	R1
APC08X03	R2	97.6k	8.45k	4.32k	2.94k	1.69k	1.13k	3.09k
APC08X08	R2	210k	17.4k	9.09k	6.04k	3.48k	2.32k	6.49k
V_r / V_{ref}	0.87V							

Be aware that the maximum V_o allowed is 3.6V (for APC08x08 series). Please refer to Centauri datasheet.

Example:

Module version: APC08J03-9 (1.8 to 6.0V_{in}, 0.9V_o).

Requiring to adjust output voltage from $V_o = 0.9V$ to $V_{ot} = 1.8V$. $V_{ref} = 0.875V$ and $R_1 = 3.09k\Omega$ (from TABLE 1).

Based on Equation (1), R_t can be determined as $3.0k\Omega$.

To adjust V_o to a lower value, R_t should be connected between P4 and P2. Equation (2) provides the calculation for R_t .

$$R_t = \frac{(V_o - V_{ref})(V_{ot} - V_{ref})}{V_{ref}(V_o - V_{ot})} R_2 \quad \text{Equation (2)}$$

Note: minimum $V_o = 0.9V$



Method 1: External Trim Resistor (*continued*)

Example

Module version: APC08F03-9 (4.0 to 6.V_{in}, 3.3V_o).

Requiring to adjust the output voltage from V_o = 3.3V to V_{ot} = 3.3 (1-0.02) = 3.234V.

V_o = 3.3V, V_{ot} = 3.234V, V_{ref} = 0.875V, R₂ = 1.13kΩ (from TABLE 1).

Based on Equation (1), R_t can be determined as 111.9kΩ.

Trim Function (*continued*)

Method 2: External DC Source

By connecting an external DC supply across P4 (Enable) and P3 (GND) through a limiting resistor R_t, (see Figure 5), output voltage adjustment can also be achieved. Equation 3 provides the relationship between the External DC supply, V_t, and V_o (where V_o is the desired output voltage).

$$V_t = \left(1 + \frac{R_t}{R_1} + \frac{R_t}{R_2}\right) V_r - \frac{R_t}{R_1} V_o \quad \text{Equation (3)}$$

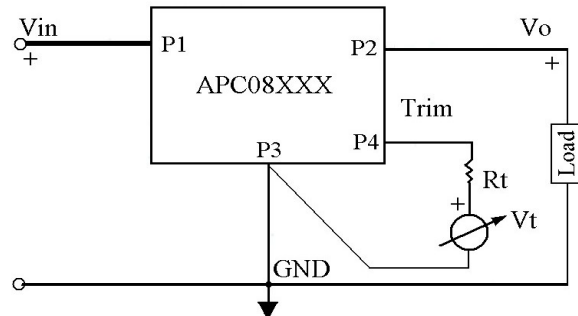


Figure 5. External DC source for output trim adjust.

Given: R_t = 10kΩ

V_o Adjustment to Lower Voltages. This method does not limit the recommended lower V_o adjustment to 2% as mentioned on previous sections re: V_o adjustment through external trim resistor.

Example:

Module version: APC08G03-9 (3V to 6V_{in}, 2.5V_o).

Requiring to adjust the output voltage from V_o = 2.5V to 1.8V

V_o = 1.8V, V_r = 0.87V, R₁ = 3.09kΩ, R₂ = 1.69kΩ (from Table 1). Based on Equation (3), V_t = 3.0V.

Example:

Module version: APC08G03-9 (3V to 6V_{in}, 2.5V_o).

Requiring to adjust the output voltage from V_o = 2.5V to 0.9V

V_o = 0.9V, V_r = 0.87V, R₁ = 3.09kΩ, R₂ = 1.69kΩ (from Table 1). Based on Equation (3), V_t = 5.9V.

Method 2: External DC Source (continued)

Vo Adjustment to Higher Voltages

Example:

Module version: APC08G03-9 (3V to 6Vin, 2.5Vo).

Requiring to adjust the output voltage from $V_o = 2.5V$ to $3.3V$

$V_o = 3.3V$, $V_r = 0.87V$, $R_1 = 3.09k\Omega$, $R_2 = 1.69k\Omega$ (from Table 1). Based on Equation (3), $V_t = -1.84V$.

If application of negative voltage is not desired, the limiting resistor **Rt** can either be changed to a lower value (**Rt = 1k Ω** , such that $V_t = 0.60V$ per Equation 3), or use Method 1.

Power Good Signal Operation (Option (-9MA)):

PG pin provides an output signal indicating the V_{out} is operational (TTL logic signal). It can sink current up to a max of 5mA and can have a maximum external pull-up voltage of 6V. Please see recommended setup shown on Figure 6.

For multiple module configurations, the PG pin/signal can be used to drive the Enable signal of the other module for simple sequencing scheme.

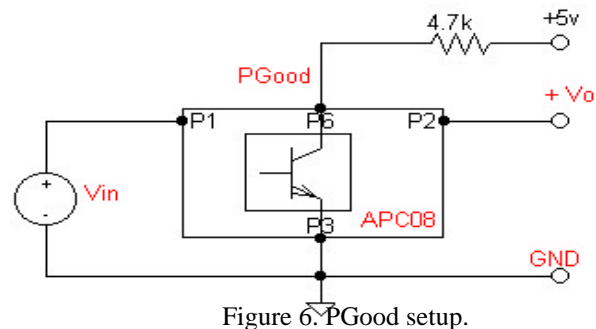


Figure 6. PGGood setup.

Active Current Share Operation (Option (-9MA)):

Active Current share pin is compatible with APC08 modules only. Connecting this pin directly with the same Pin from another module guarantees current sharing to within 40% to 60% I_{out} . Note that this pin is not compatible with competitive modules that employ active current sharing.

To attain efficient current sharing between like modules, the following points are recommended:

- The modules to be shared should be located as close as possible into the host card.
- The copper tracks that connect V_o and GND should at least be 0.60" in width with at least 2 oz. Cu.
- Due to tolerances of turn-on time characteristics, the initial load current of two APC08 units connected in current sharing configuration should be less than the OCP point of one module. This is to ensure that the first unit that reaches V_o set-point is capable of supplying the load current. This also eliminates the possibility of false triggering the OCP protection. The load current can then be ramped up to the desired loading condition (typical 13A max combined for 2 modules in parallel) after both outputs have stabilized.
- Due to mismatches on the output voltage setpoints of the two converters in parallel, it is recommended to maintain a minimum load current (typical 1.5A) on the output.



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Performance Curves - Efficiency

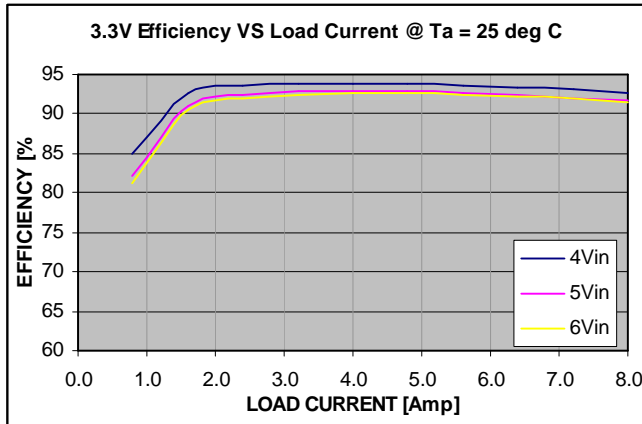


Figure 7. APC08F03 Efficiency Curve.

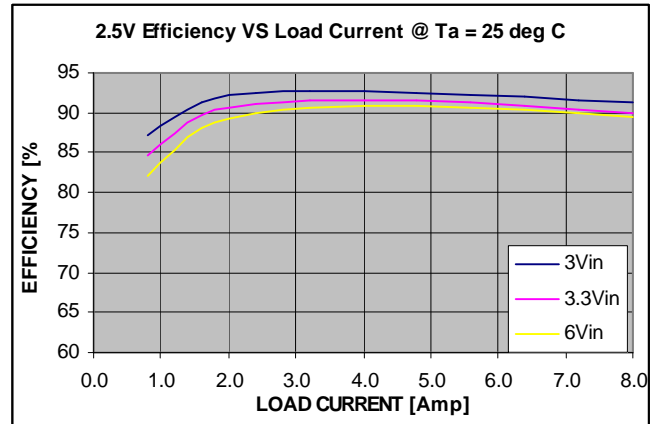


Figure 8. APC08G03 Efficiency Curve.

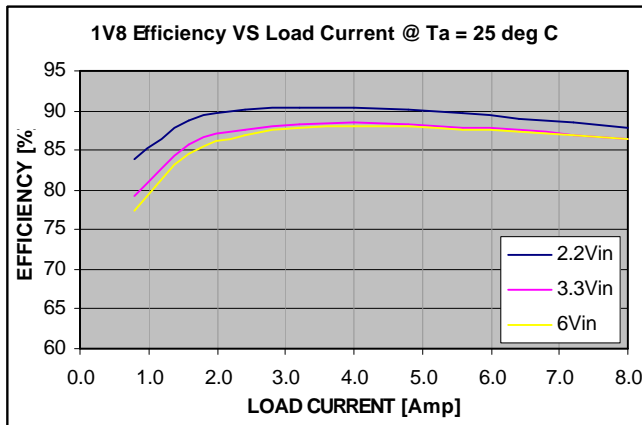


Figure 9. APC08Y03 Efficiency Curve.

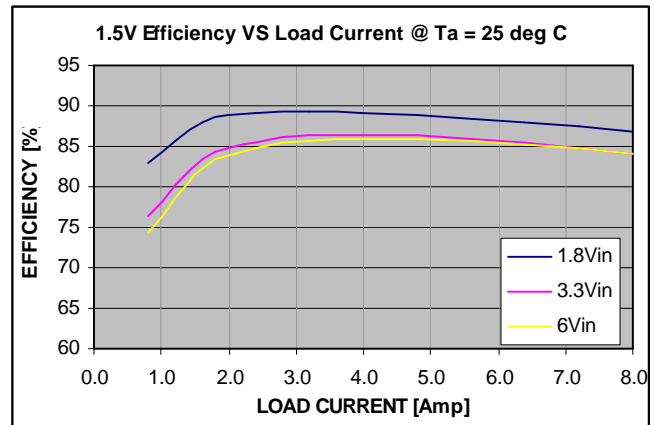


Figure 10. APC08M03 Efficiency Curve.

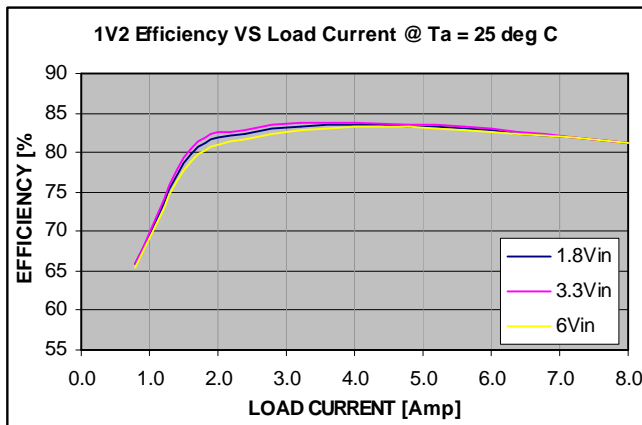


Figure 11. APC08K03 Efficiency Curve.

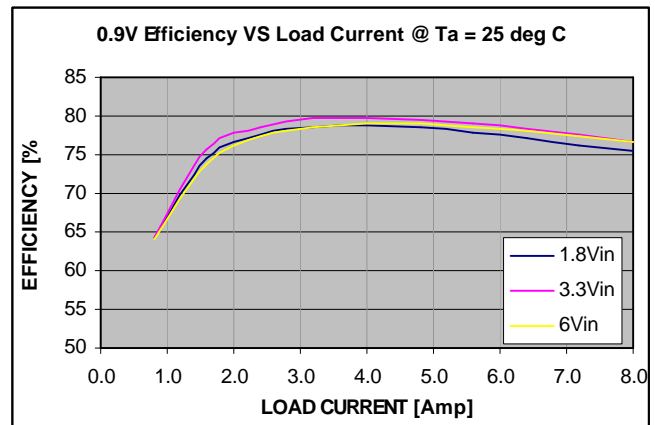


Figure 12. APC08J03 Efficiency Curve.



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Performance Curves - Efficiency (*continued*)

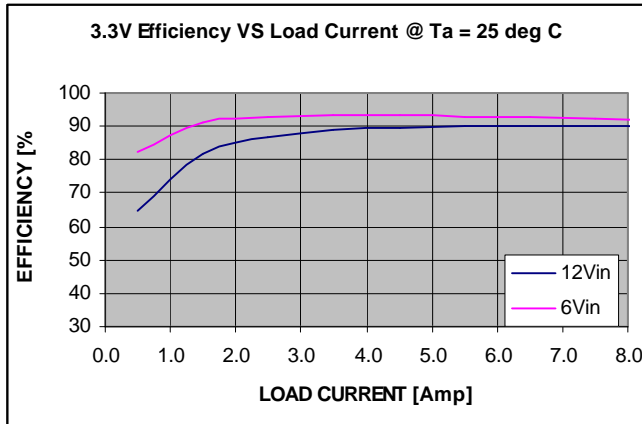


Figure 13. APC08F08 Efficiency Curve.

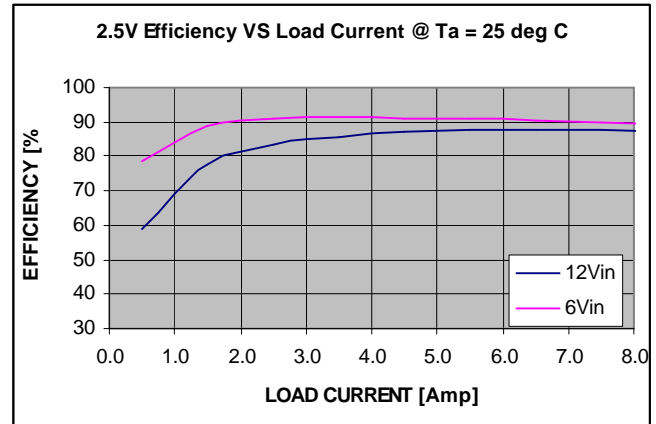


Figure 14. APC08G08 Efficiency Curve.

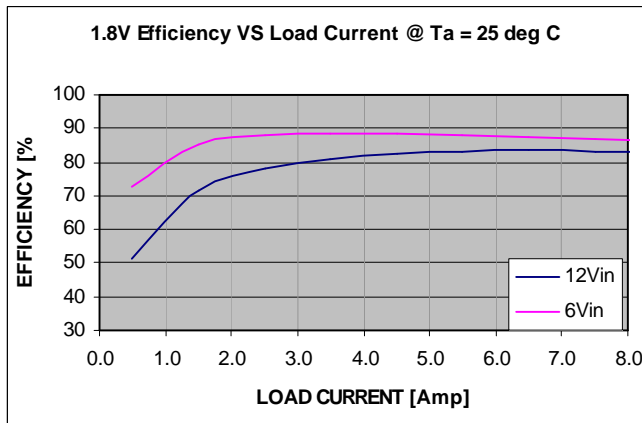


Figure 15. APC08Y08 Efficiency Curve.

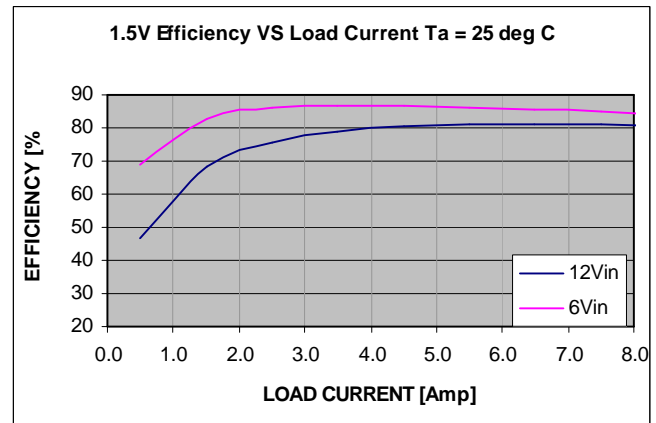


Figure 16. APC08M08 Efficiency Curve.

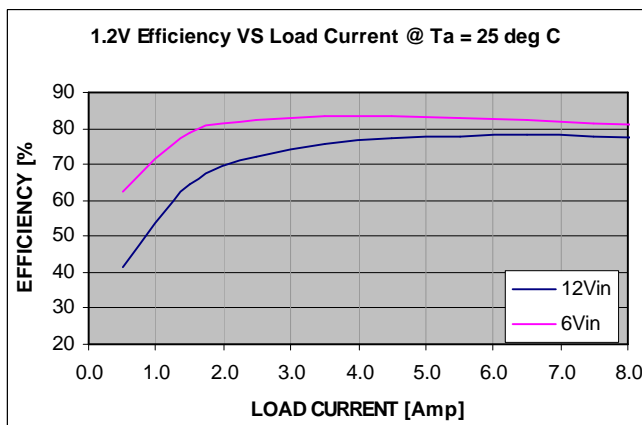


Figure 17. APC08K08 Efficiency Curve.

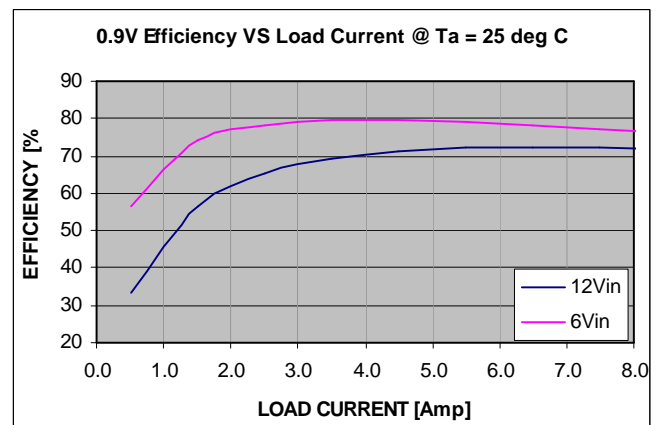


Figure 18. APC08J08 Efficiency Curve.



Performance Curves - Thermal Derating Curve

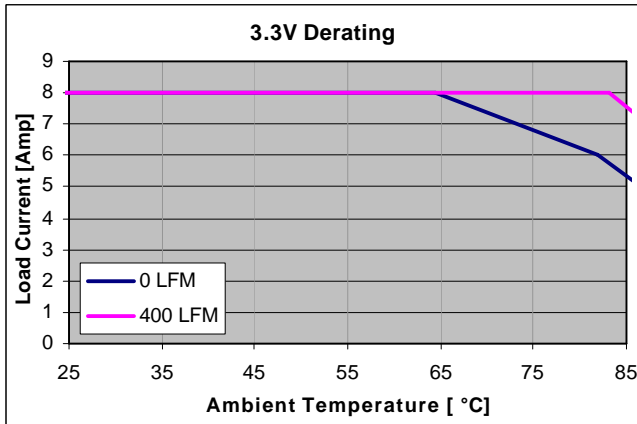


Figure 19. APC08F03 Thermal Derating Curve.

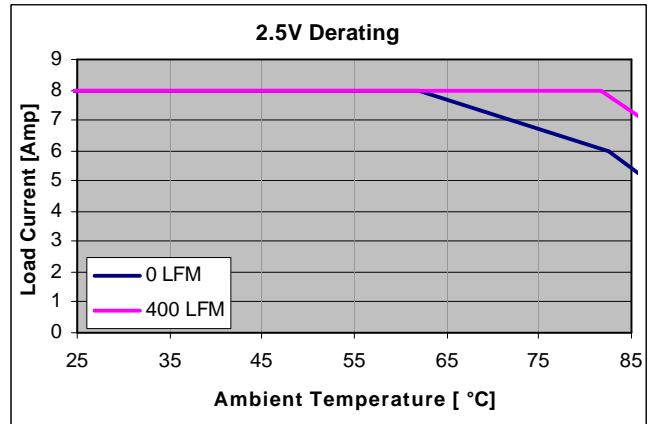


Figure 20. APC08G03 Thermal Derating Curve.

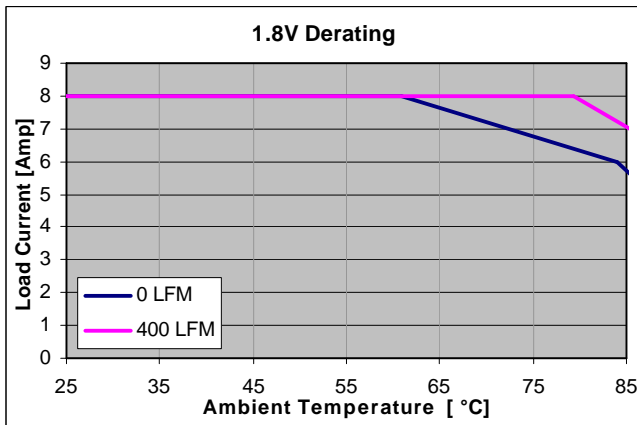


Figure 21. APC08Y03 Thermal Derating Curve.

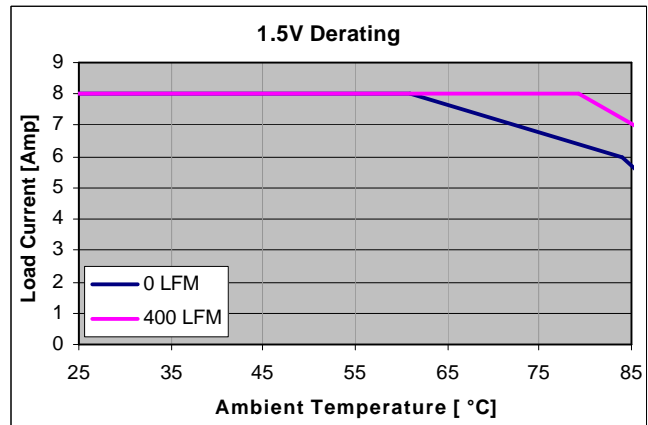


Figure 22. APC08M03 Thermal Derating Curve.

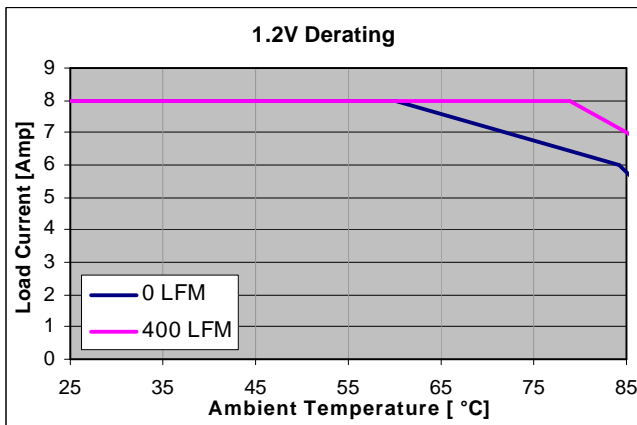


Figure 23. APC08K03 Thermal Derating Curve.

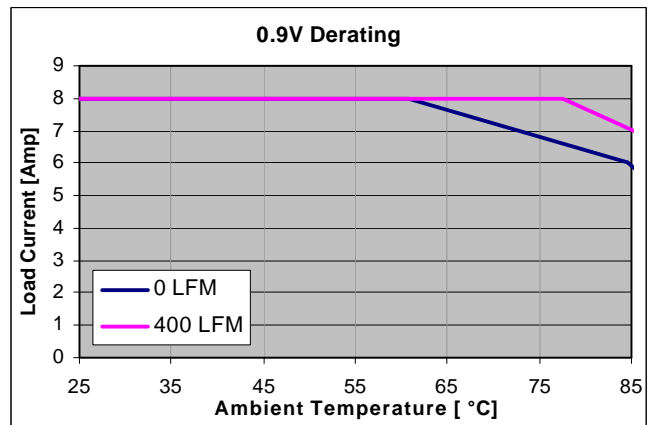


Figure 24. APC08J03 Thermal Derating Curve.



Technical Reference Note (APC08)

Performance Curve - Thermal Derating (continued)

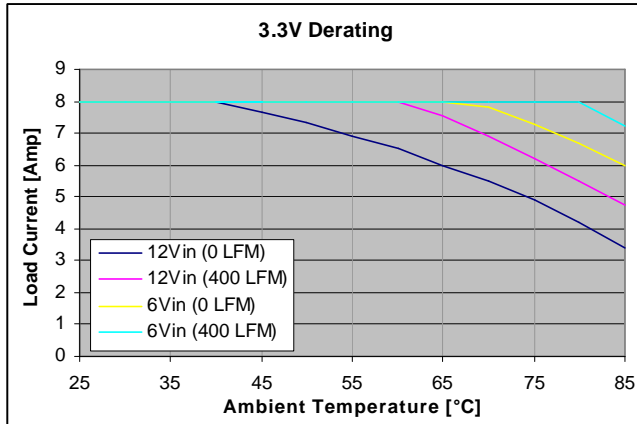


Figure 25. APC08F08 Thermal Derating Curve.

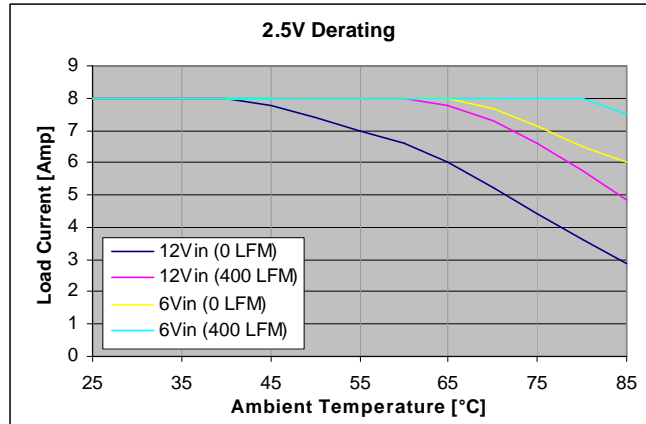


Figure 26. APC08G08 Thermal Derating Curve.

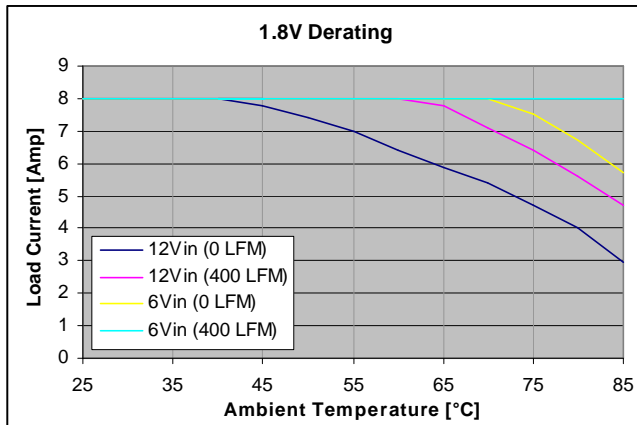


Figure 27. APC08Y08 Thermal Derating Curve.

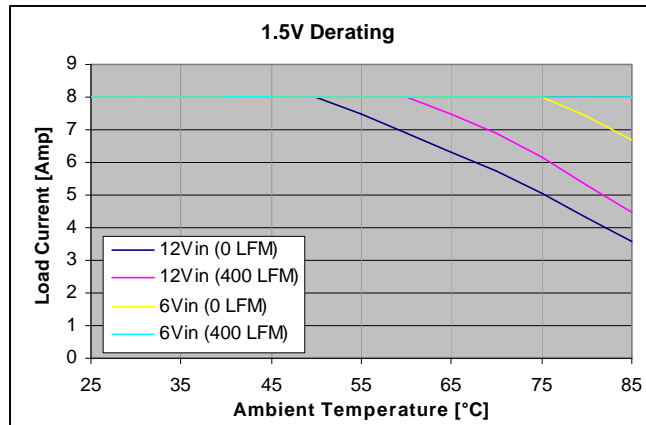


Figure 28. APC08M08 Thermal Derating Curve.

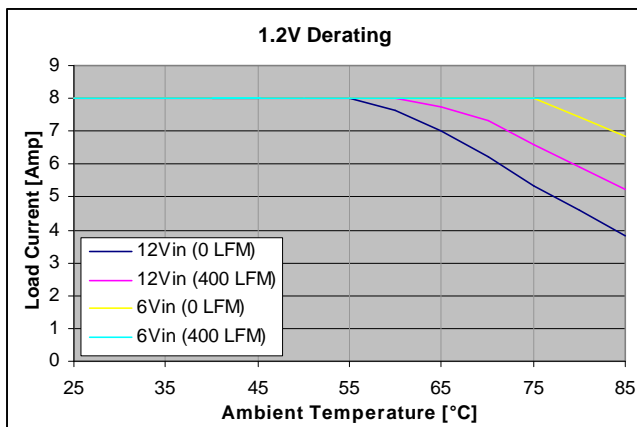


Figure 29. APC08K08 Thermal Derating Curve.

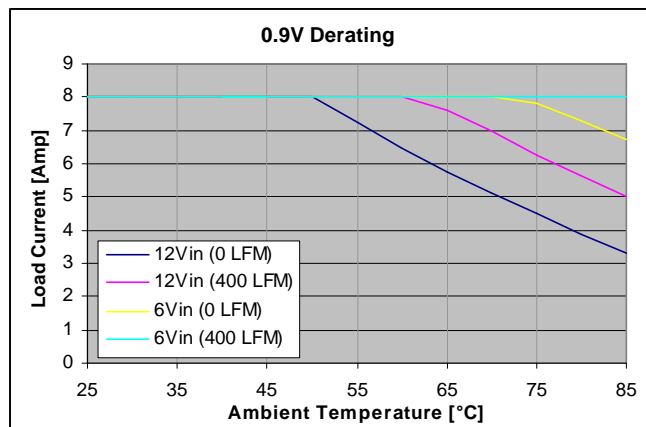


Figure 30. APC08J08 Thermal Derating Curve.



Technical Reference Note (APC08)

Performance Curves

Typical performance curves, T_{ON} delay, at 25°C ambient temperature; $I_O = I_{O,max}$, $V_{IN} = V_{IN,max}$. For reference CH1 is connected to + V_{IN} pin, CH2 is connected to the output of the module.

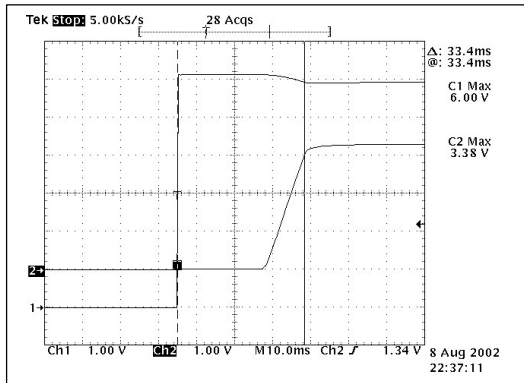


Figure 31. APC08F03 T_{ON} delay at $V_{IN,max} = 6V$.

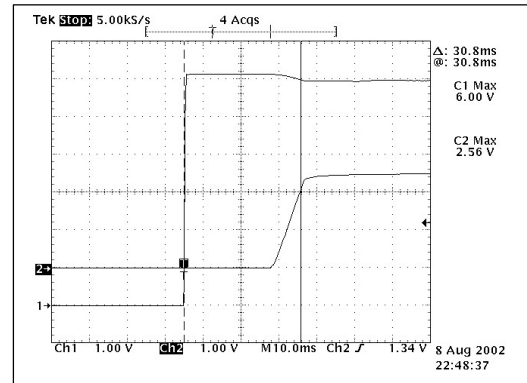


Figure 32. APC08G03 T_{ON} delay at $V_{IN,max} = 6V$.

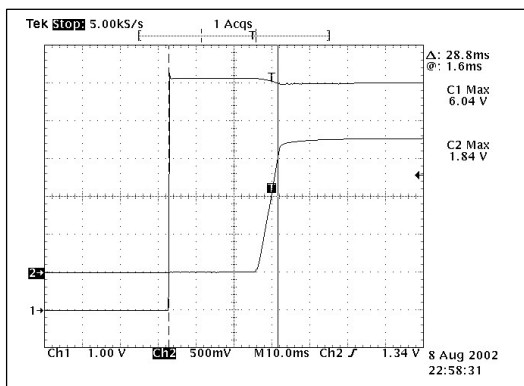


Figure 33. APC08Y03 T_{ON} delay at $V_{IN,max} = 6V$.

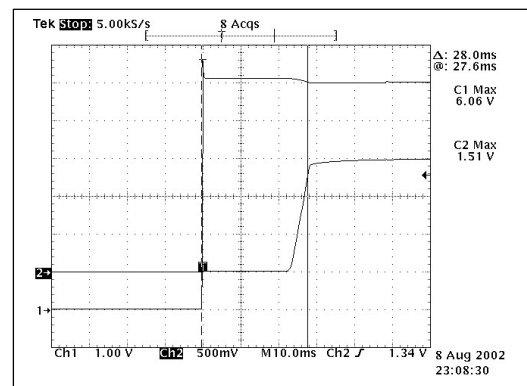


Figure 34. APC08M03 T_{ON} delay at $V_{IN,max} = 6V$.

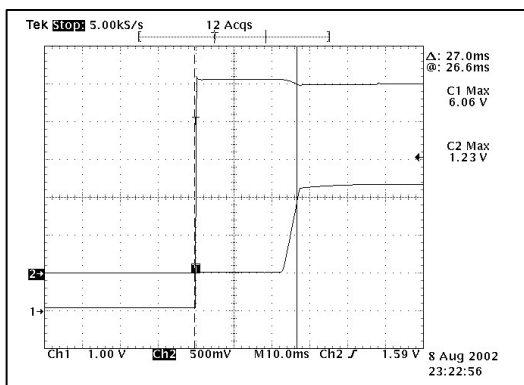


Figure 35. APC08K03 T_{ON} delay at $V_{IN,max} = 6V$.

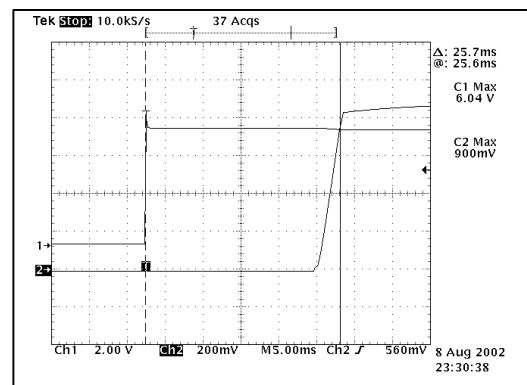


Figure 36. APC08J03 T_{ON} delay at $V_{IN,max} = 6V$.



Technical Reference Note (APC08)

Performance Curves (continued)

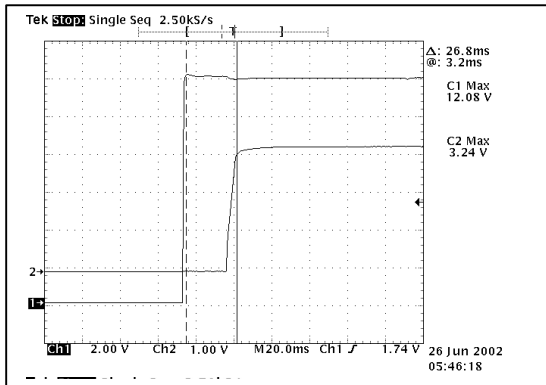


Figure 37. APC08F08 T_{ON} delay at $V_{IN,max} = 12V$.

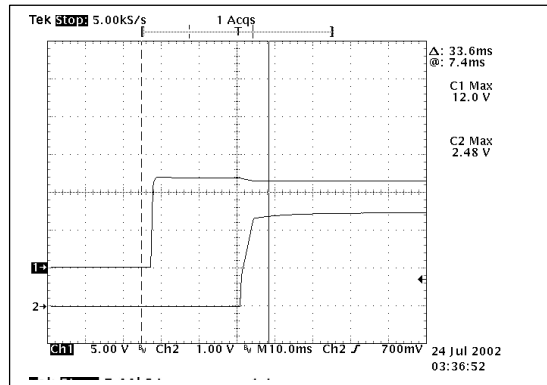


Figure 38. APC08G08 T_{ON} delay at $V_{IN,max} = 12V$.

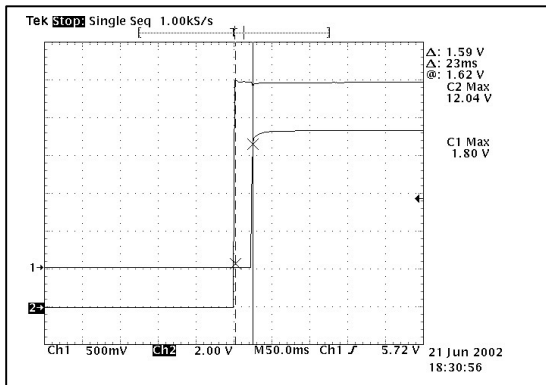


Figure 39. APC08Y08 T_{ON} delay at $V_{IN,max} = 12V$ (Ch1)

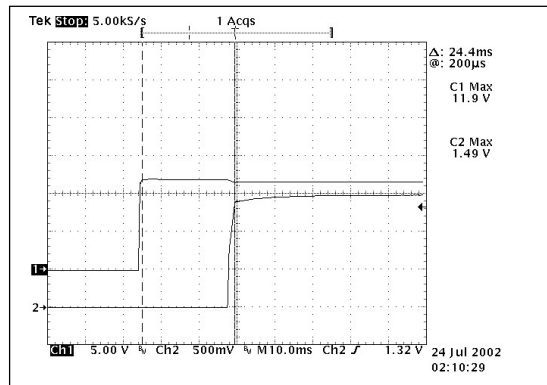


Figure 40. APC08M08 T_{ON} delay at $V_{IN,max} = 12V$.

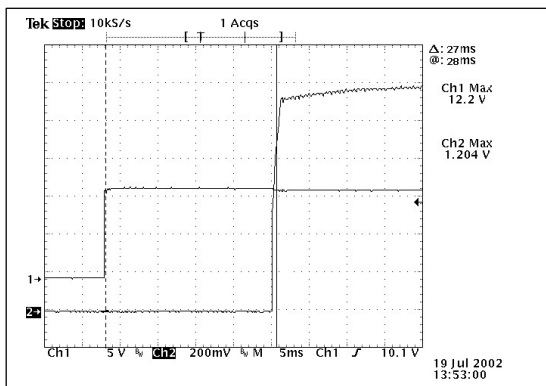


Figure 41. APC08K08 T_{ON} delay at $V_{IN,max} = 12V$.

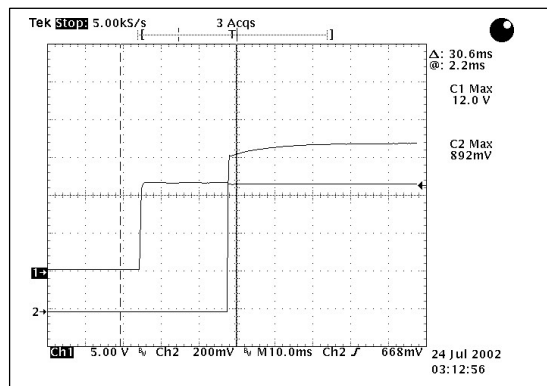


Figure 42. APC08J08 T_{ON} delay at $V_{IN,max} = 12V$.

Young's Stability Curves

GAIN MARGIN

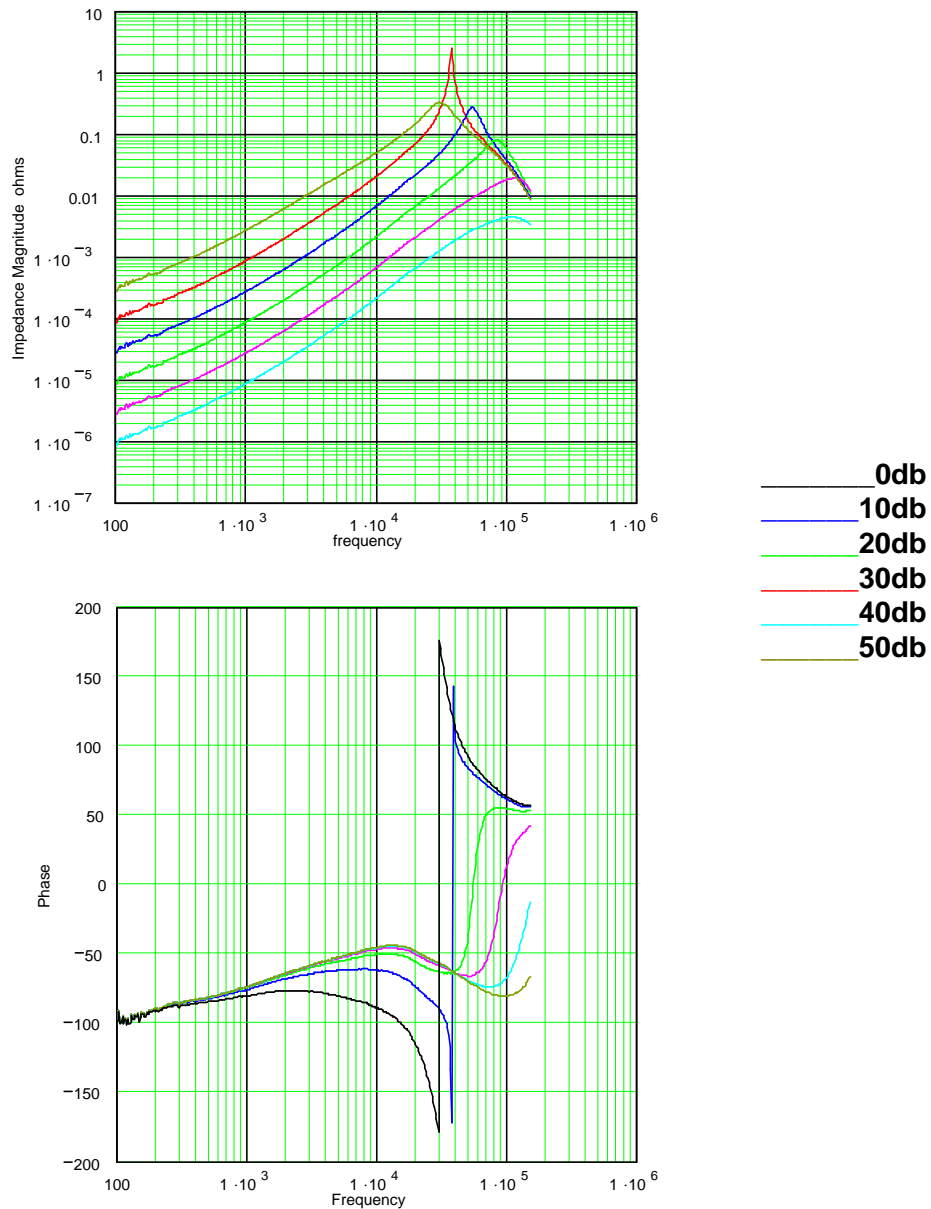


Figure 43. YSC- Gain Margin response to determine system stability at other load condition.

Young's Stability Curves

PHASE MARGIN

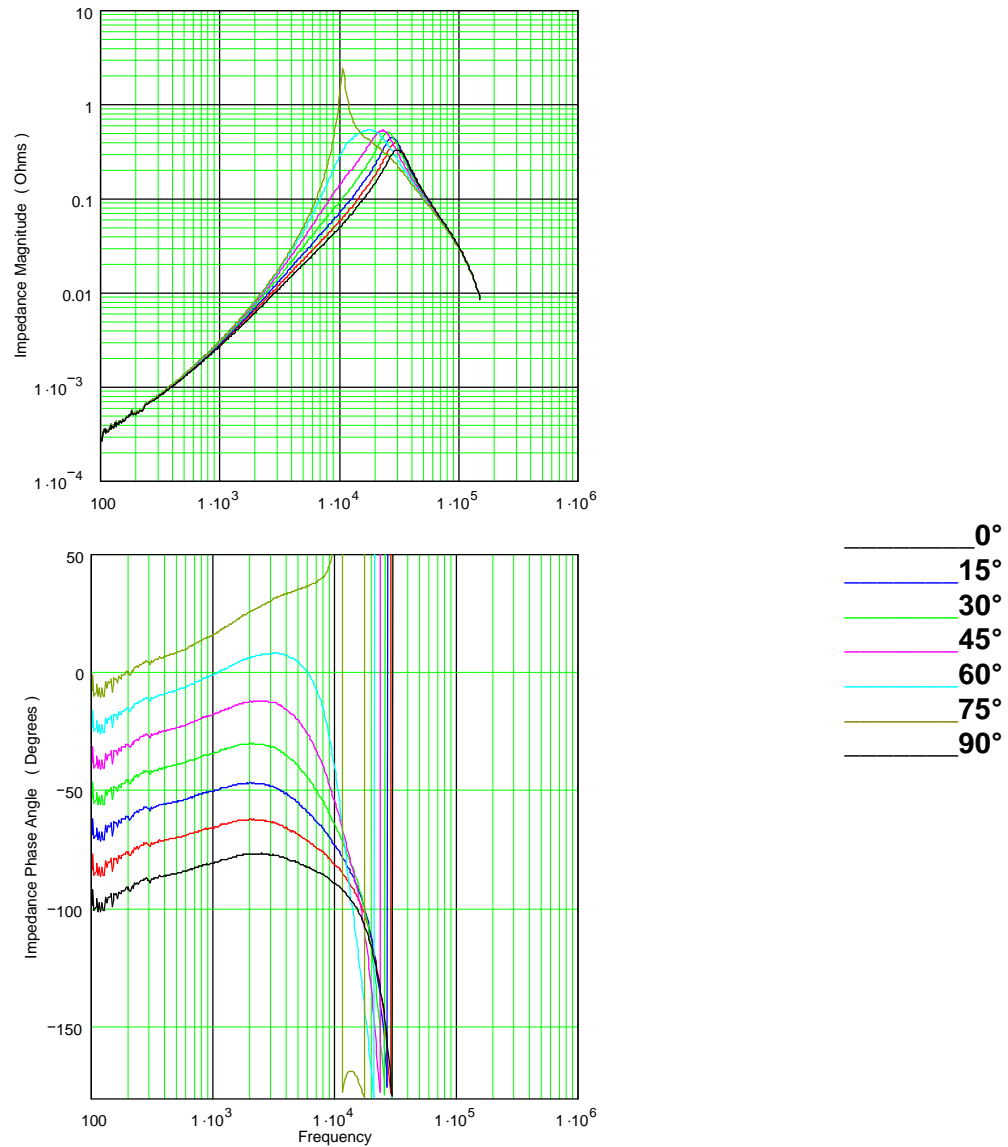
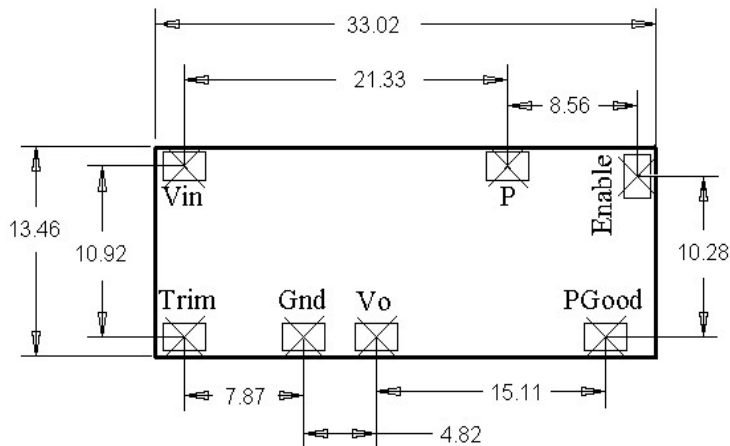


Figure 44. YSC - Phase Margin response to determine system stability at other load conditions.

Mechanical Specifications

OUTLINE DRAWING



PIND / PIN DIMENSION	
Nominal Pin Dimension	0.055 X 0.102 [in]
Suggested Pad Dimensions	0.070 X 0.110 [in]

Figure 45. Pad Layout outline (in mm).

Parameter	Device	Symbol	Min	Typ	Max	Unit
Dimension	All	L	-	-	1.300 (33.02)	in (mm)
		W	-	-	0.530 (13.46)	in (mm)
		H	-	-	0.290 (7.36)	in (mm)
Weight	All	-	-	5 (0.16)	10 (0.32)	g (oz)

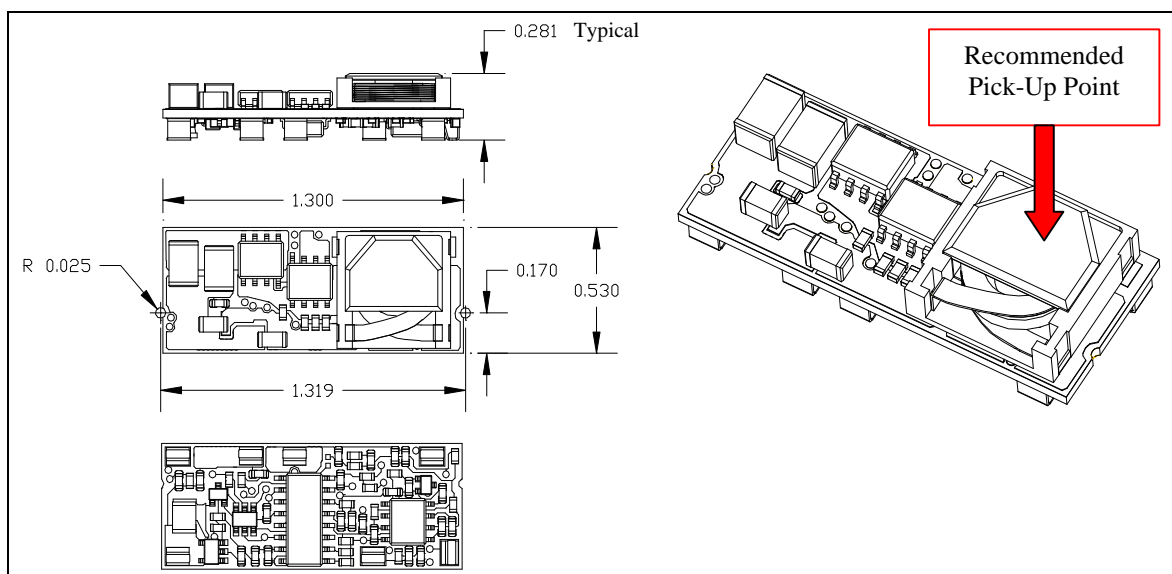


Figure 46. Mechanical Outline (in inches).



Technical Reference Note (APC08)

RECOMMENDED LOCATION FOR PICK AND PLACE

The flat top surface of the large inductor (topside of the board) provides a versatile and convenient way of picking up the module (see Figure 46). A 6-7mm outside diameter nozzle from a conventional SMD machine is recommended to attain maximum vacuum pick-up. Nozzle travel and rotation speed should be controlled to prevent this off-centered picked-up module from falling off the nozzle. The use of vision recognition systems for placement accuracy will be very helpful.

REFLOW NOTES / RECOMMENDATIONS

1. Refer to the recommended Reflow Profile per Figure 47. Profile parameters exceeding the recommended maximums may result to permanent damage to the module.
2. The module is recommended for topside reflow process to the host card. For other orientations, contact factory.
3. In the event that the module needs to be desoldered from the host card, some pins may be detached from the module.

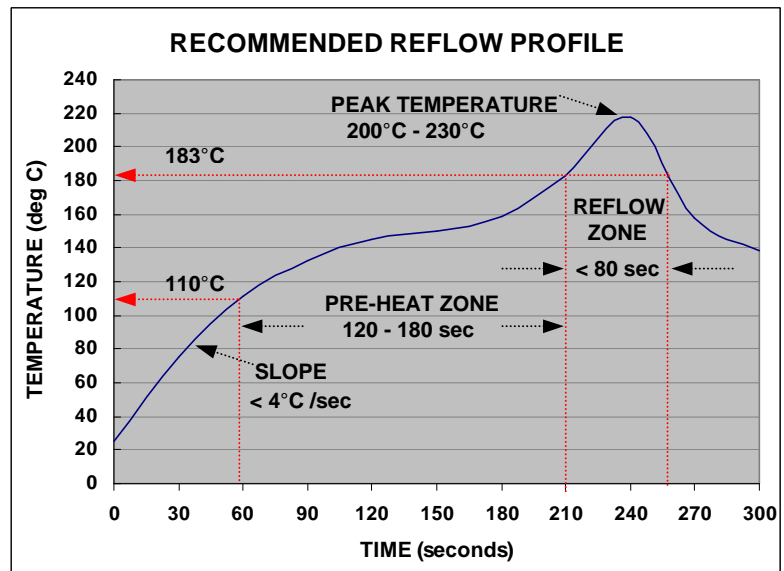


Figure 47. Recommended Reflow Profile.

MODULE MARKINGS / LABELS

Marking shall be permanent and legible. Please refer to Figure 48 for the module marking/ label detail.

Note 1	
MMM	Model No
FFF	Option
Note 2	
YYWW	Year / Work Week
D	Day of Week
PP	nth Panel of the day
LL	Location in the panel
Note 3: Barcode	
	6 & 7 characters / line Code 128, 32CPI 0.070" Height

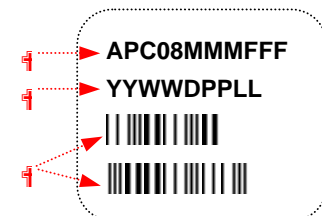


Figure 48. Module Label



Technical Reference Note (APC08)

PACKING AND SHIPPING

Standard packaging for the modules will be in tape and reel. Jedec-style tray packaging is also available (add suffix "J" in pn). Please refer to the ordering information. Maximum number of modules in a reel is 300pcs. The tray can hold 33 modules max. Please refer to Figure 49 for the carrier dimensions.

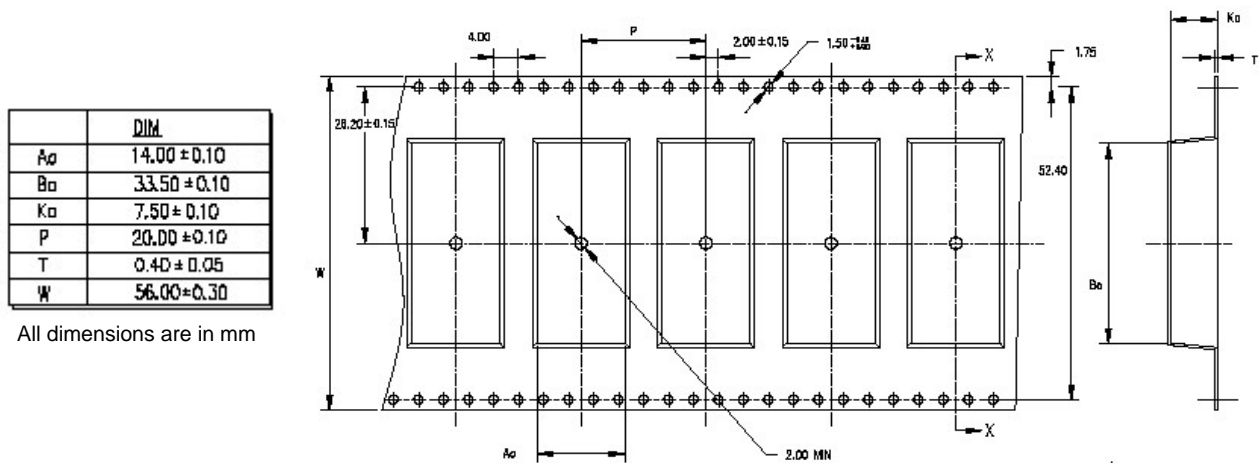


Figure 49. Tape/ pocket dimensions

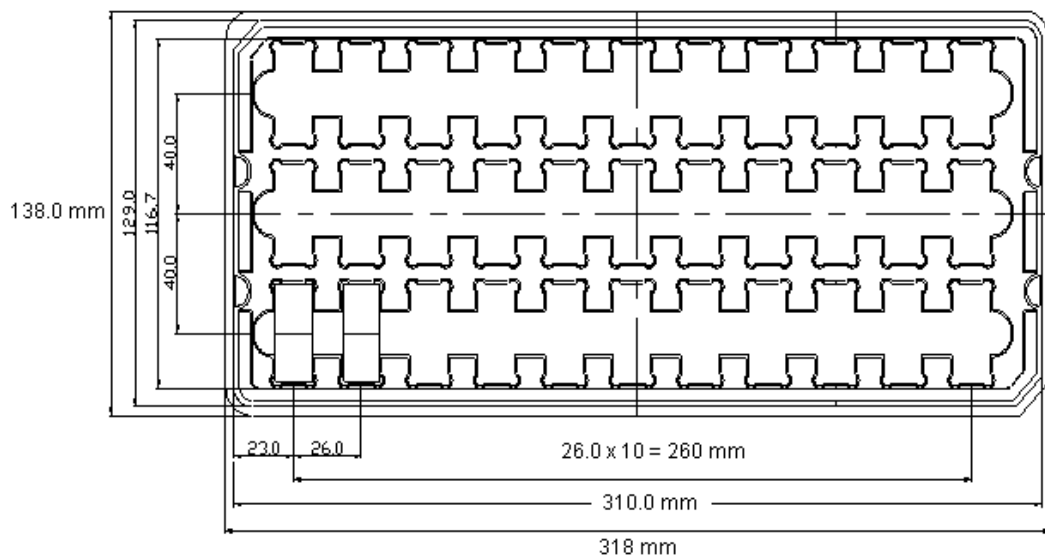


Figure 50. Jedec-style tray dimensions in mm.



PART NUMBER CODING SCHEME FOR ORDERING

A	P	C	0	8	x	0	y	-	z
---	---	---	---	---	---	---	---	---	---

x	Output Voltage
	F = 3.3V G = 2.5V Y = 1.8V
	M = 1.5V K = 1.2V J = 0.9V
y	Input Voltage Range
	3: 1.8V to 6V 8: 5V to 12V
z	Options
	9: Trim function 9MA: Trim function plus PGood and Current Sharing J: Adding a J suffix indicates Jedec style tray packaging W: Improved Loop Bandwidth (for APC08x03 version only)

Please call 1-888-41-ASTEC for further inquiries or
visit us at www.astecpower.com