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FAIRCHILD SEMICONDUCTOR®

January 2008

FSA3157B
Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

Features

- Useful in Both Analog and Digital Applications
- Ultra-small, MicroPak™ Leadless Package
- Low On Resistance: <10Ω Typical at 3.3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Rail-to-rail Signal Handling
- Power-down, High-impedance Control Input
- Over-voltage Tolerance of Control Input to 7.0V
- Break-before-make Enable Circuitry
- 250MHz, 3dB Bandwidth

Description

The FSA3157B is a high-performance, single-pole / double-throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The control input tolerates voltages up to 5.5V, independent of the V_{CC} operating range.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSA3157BL6X	-40 to +85°C	7G	6-Lead, MicroPak 1.0mm Wide Package	5000 Units on Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

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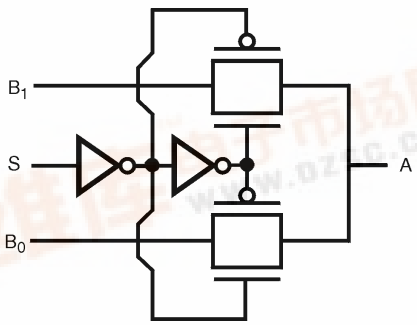

Figure 1. Logic Symbol

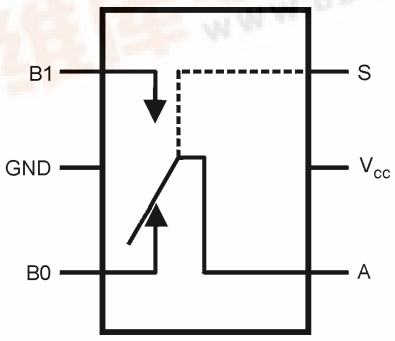

Figure 2. Analog Symbol

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Pin Configuration

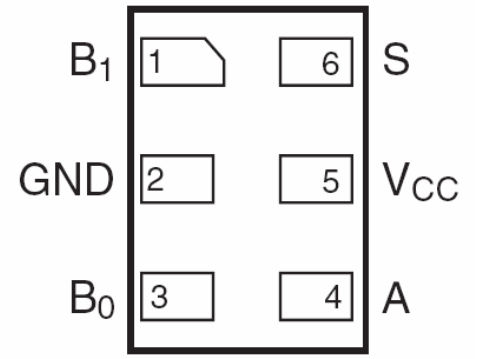

Figure 3. Pad Assignments

Function Table

Input (S)	Function
Logic Level LOW	B_0 Connected to A
Logic Level HIGH	B_1 Connected to A

Pin Descriptions

Pin	Description
A, B_0, B_1	Data Ports
S	Control Input

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	7.0	V
V_S	DC Switch Voltage(1)	-0.5	V_{CC}+0.5	V
V_{IN}	DC Input Voltage(1)	-0.5	7.0	V
I_{IK}	DC Input Diode Current at V_{IN} < 0V	-50		mA
I_{OUT}	DC Output Current		128	mA
$I_{CC/IGND}$	DC V_{CC} or Ground Current		±100	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Junction Temperature Under Bias		+150	°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)		+260	°C
P_D	Power Dissipation at +85°C		180	mW
ESD	Human Body Model, JESD22-A114		4	kV

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
V_{IN}	Control Input Voltage(2)		0	V_{CC}	V
V_{IN}	Switch Input Voltage(2)		0	V_{CC}	v
V_{OUT}	Output Voltage(2)		0	V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
t_r, t_f	Input Rise and Fall Time	Control Input V_{CC}=2.3V–3.6V	0	10	ns/V
		Control Input V_{CC}=4.5V–5.5V	0	5	

Note:

2. Control input must be held HIGH or LOW; it must not float.

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Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			T_A=-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage		1.65 to 1.95	$0.75V_{CC}$			$0.75V_{CC}$		V
			2.3 to 5.5	$0.7V_{CC}$			$0.7V_{CC}$		
V_{IL}	Low Level Input Voltage		1.65 to 1.95			$0.25V_{CC}$		$0.25V_{CC}$	V
			2.3 to 5.5			$0.3V_{CC}$		$0.3V_{CC}$	
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le 5.5V$	0 to 5.5		±0.05	±0.1		±1	µA
I_{OFF}	Off State Leakage Current	$0 \le A, B \le V_{CC}$	1.65 to 5.5		±0.05	±0.1		±1	µA
R_{ON}	Switch On Resistance(3)	V_{IN}=0V, I_O=30mA	4.5		3.0	7.0		7.0	Ω
		V_{IN}=2.4V, I_O=–30mA			5.0	12.0		12.0	
		V_{IN}=4.5V, I_O=–30mA			7.0	15.0		15.0	
		V_{IN}=0V, I_O=24mA	3.0		4.0	9.0		9.0	
		V_{IN}=3V, I_O=–24mA			10.0	20.0		20.0	
		V_{IN}=0V, I_O=8mA	2.3		5.0	12.0		12.0	
		V_{IN}=2.3V,I_O=–8mA			13.0	30.0		30.0	
		V_{IN}=0V, I_O=4mA	1.65		6.5	20.0		20.0	
		V_{IN}=1.65V, I_O=–4mA			17.0	50.0		50.0	
I_{CC}	Quiescent Supply Current: All Channels On or Off	V_{IN}=V_{CC} or GND I_{OUT}=0	5.5			1.0		10.0	µA
	Analog Signal Range		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{RANGE}	On Resistance Over Signal Range(3,7)	I_A=–30mA, $0 \le V_{Bn} \le V_{CC}$	4.5					25.0	Ω
		I_A=–24mA, $0 \le V_{Bn} \le V_{CC}$	3.0					50.0	
		I_A=–8mA, $0 \le VBn \le V_{CC}$	2.3					100.0	
		I_A=–4mA, $0 \le V_{Bn} \le V_{CC}$	1.65					300	
ΔR_{ON}	On Resistance Match Between Channels(3,4)	I_A=–30mA, V_{Bn}=3.15	4.5		0.15				Ω
		I_A=–24mA, V_{Bn} 2.1	3.0		0.2				
		I_A=–8mA, V_{Bn}=1.6	2.3		0.5				
		I_A=–4mA, V_{Bn}=1.15	1.65		0.50				
Rflat	On Resistance Flatness(3,4,6)	I_A=–30mA, $0 \le V_{Bn} \le V_{CC}$	5.0		6.0				Ω
		I_A=–24mA, $0 \le V_{Bn} \le V_{CC}$	3.0		12.0				
		I_A=–8mA, $0 \le V_{Bn} \le V_{CC}$	2.5		28.0				
		I_A=–4mA, $0 \le V_{Bn} \le V_{CC}$	1.8		125				

Notes:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports)
4. Parameter is characterized, but not tested in production.
5. $\Delta R_{ON} = R_{ON}$ maximum– R_{ON} minimum measured at identical V_{CC}, temperature, and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
7. Guaranteed by design.

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AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PLH}	Propagation Delay Bus-to-bus[8]	V_I=OPEN	1.65 to 1.95			3.5		3.5	ns	Figure 10 Figure 11
			2.3 to 2.7			1.2		1.2		
			3.0 to 3.6			0.8		0.8		
			4.5 to 5.5			0.3		0.3		
t_{PZL}, t_{PZH}	Output Enable Time Turn on Time (A to B_n)	V_I=2x V_{CC} for t_{PZL} V_I=0V for t_{PZH}	1.65 to 1.95	7.0		23.0		24.0	ns	Figure 10 Figure 11
			2.3 to 2.7	3.5		13.0		14.0		
			3.0 to 3.6	2.5		6.9		7.6		
			4.5 to 5.5	1.7		5.2		5.7		
t_{PLZ}, t_{PHZ}	Output Disable Time Turn off Time (A Port to B Port)	V_I=2x V_{CC} for t_{PLZ} V_I=0V for $t_{PHZ1.}$	1.65 to 1.95	3.0		12.5		13.0	ns	Figure 10 Figure 11
			2.3 to 2.7	2.0		7.0		7.5		
			3.0 to 3.6	1.5		5.0		5.3		
			4.5 to 5.5	0.8		3.5		3.8		
t_{BBM}	Break-before-Make Time[9]		1.65 to 1.95	0.5			0.5		ns	Figure 12
			2.3 to 2.7	0.5			0.5			
			3.0 to 3.6	0.5			0.5			
			4.5 to 5.5	0.5			0.5			
Q	Charge Injection[9]	C_L=0.1nF, V_{GEN}=0V	5.0		7.0				pC	Figure 13
		R_{GEN}=0Ω	3.3		3.0					
OIRR	Off Isolation[10]	R_L=50Ω, f=10MHz	1.65 to 5.5		-57.0				dB	Figure 14
Xtalk	Crosstalk	R_L=50Ω, f=10MHz	1.65 to 5.5		-54.0					Figure 15
BW	-3dB Bandwidth	R_L=50Ω	1.65 to 5.5		250				dB	Figure 18
THD	Total Harmonic Distortion[9]	R_L=600Ω, 0.5V_{PP}, f=600Hz to 20KHz	5.000		.011				%	

Notes:

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).
9. Guaranteed by design.
10. Off Isolation = 20 $\log_{10}$ [V_A / V_{Bn}].

Capacitance

T_A = +25°C, f=1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typ.	Max.	Units	Figure
C_{IN}	Control Pin Input Capacitance	V_{CC}=0V	2.3		pF	
C_{IO-B}	B Port Off Capacitance	V_{CC}=5.0V	6.5		pF	Figure 16
C_{IOA-ON}	A Port Capacitance when Switch is Enabled	V_{CC}=5.0V	18.5		pF	Figure 17

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Typical Performance Characteristics

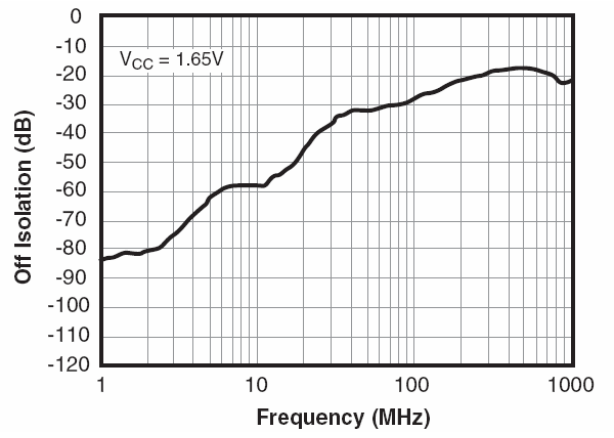

Figure 4. Off Isolation, V_{CC}-1.65V

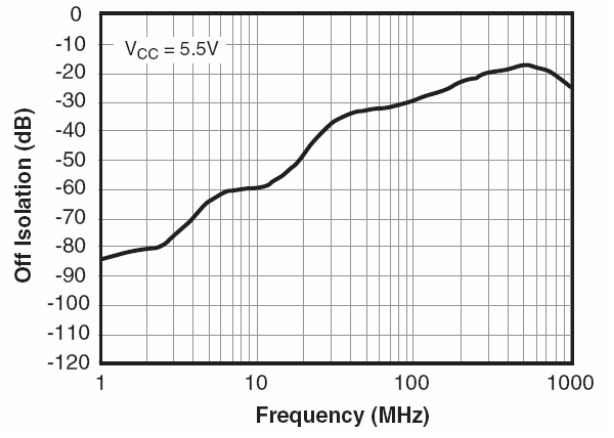

Figure 5. Off Isolation, V_{CC}-5. 5V

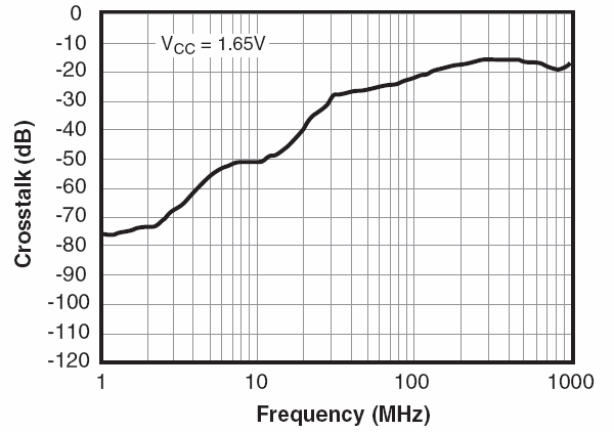

Figure 6. Crosstalk, V_{CC}=1.65V

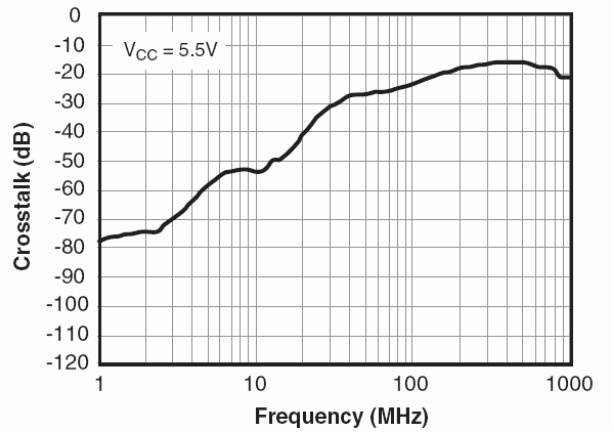

Figure 7. Crosstalk, V_{CC}=5.5V

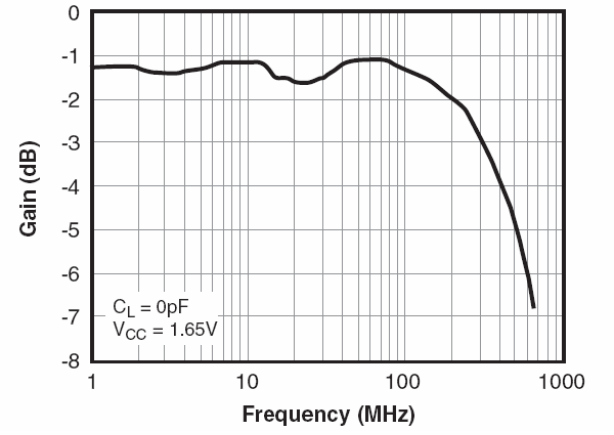

Figure 8. Bandwidth, V_{CC}=1.65V

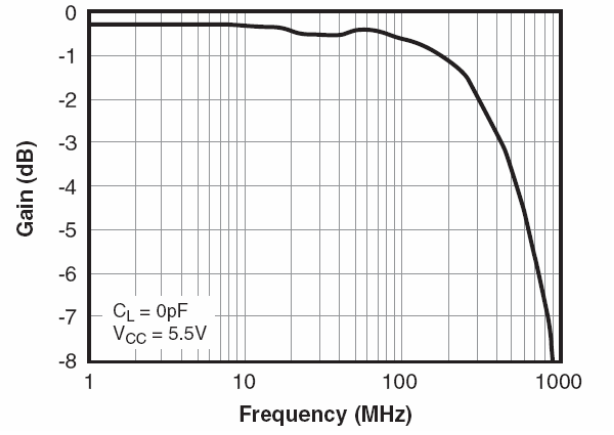

Figure 9. Bandwidth, V_{CC}=5.5V

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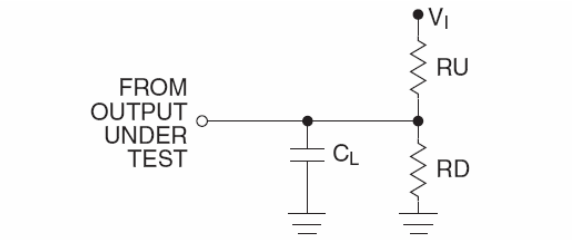
AC Loading and Waveforms



Notes:
Input driven by 50Ω source terminated in 50Ω
C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_W = 500 ns

Figure 10. AC Test Circuit

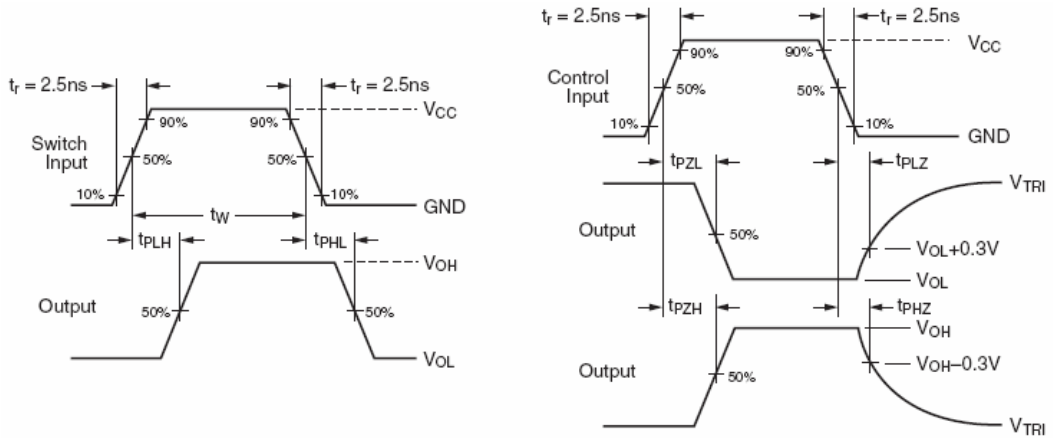


Figure 11. AC Waveforms

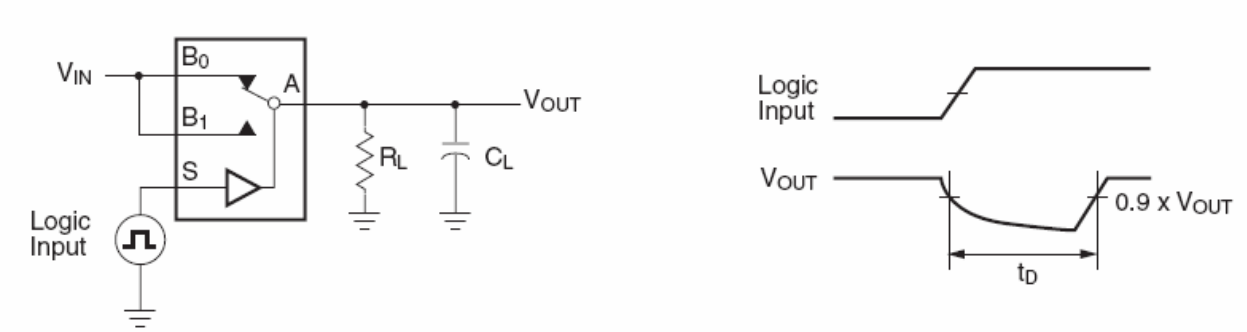


Figure 12. Break-before-make Interval Timing

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AC Loading and Waveforms (Continued)

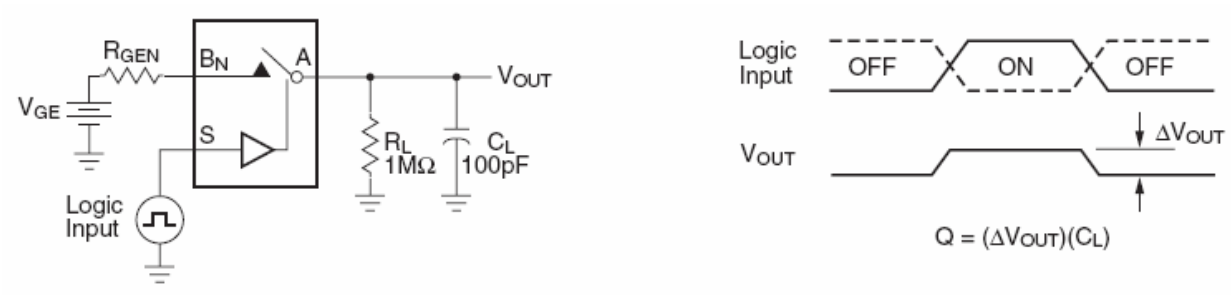

Figure 13. Charge Injection Test

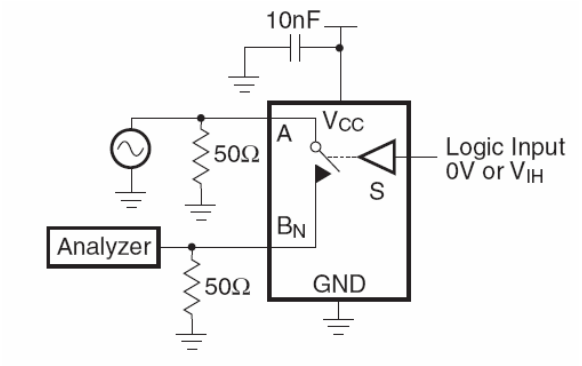

Figure 14. Off Isolation

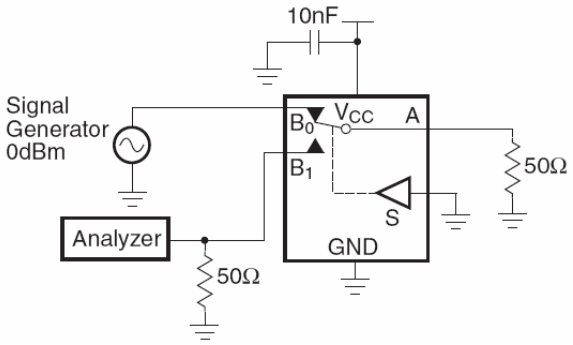

Figure 15. Crosstalk

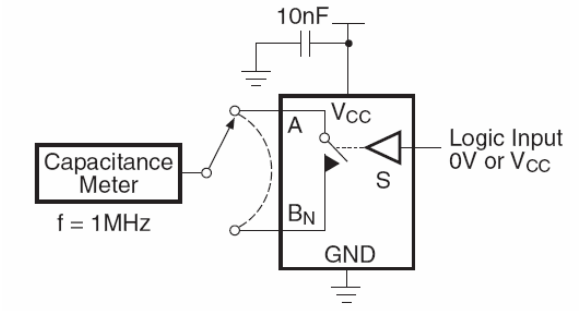

Figure 16. Channel Off Capacitance

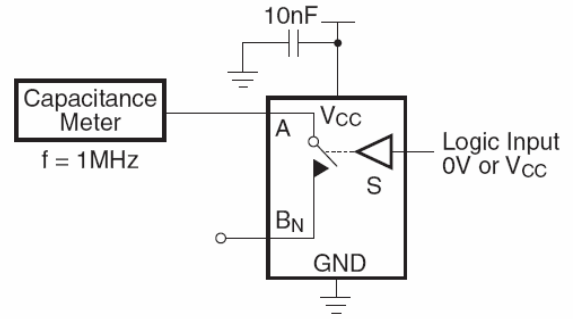

Figure 17. Channel On Capacitance

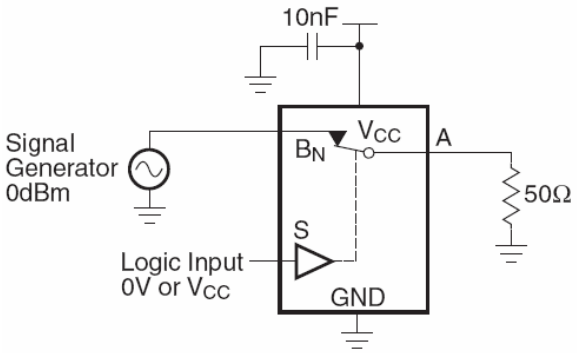

Figure 18. Bandwidth

Physical Dimensions

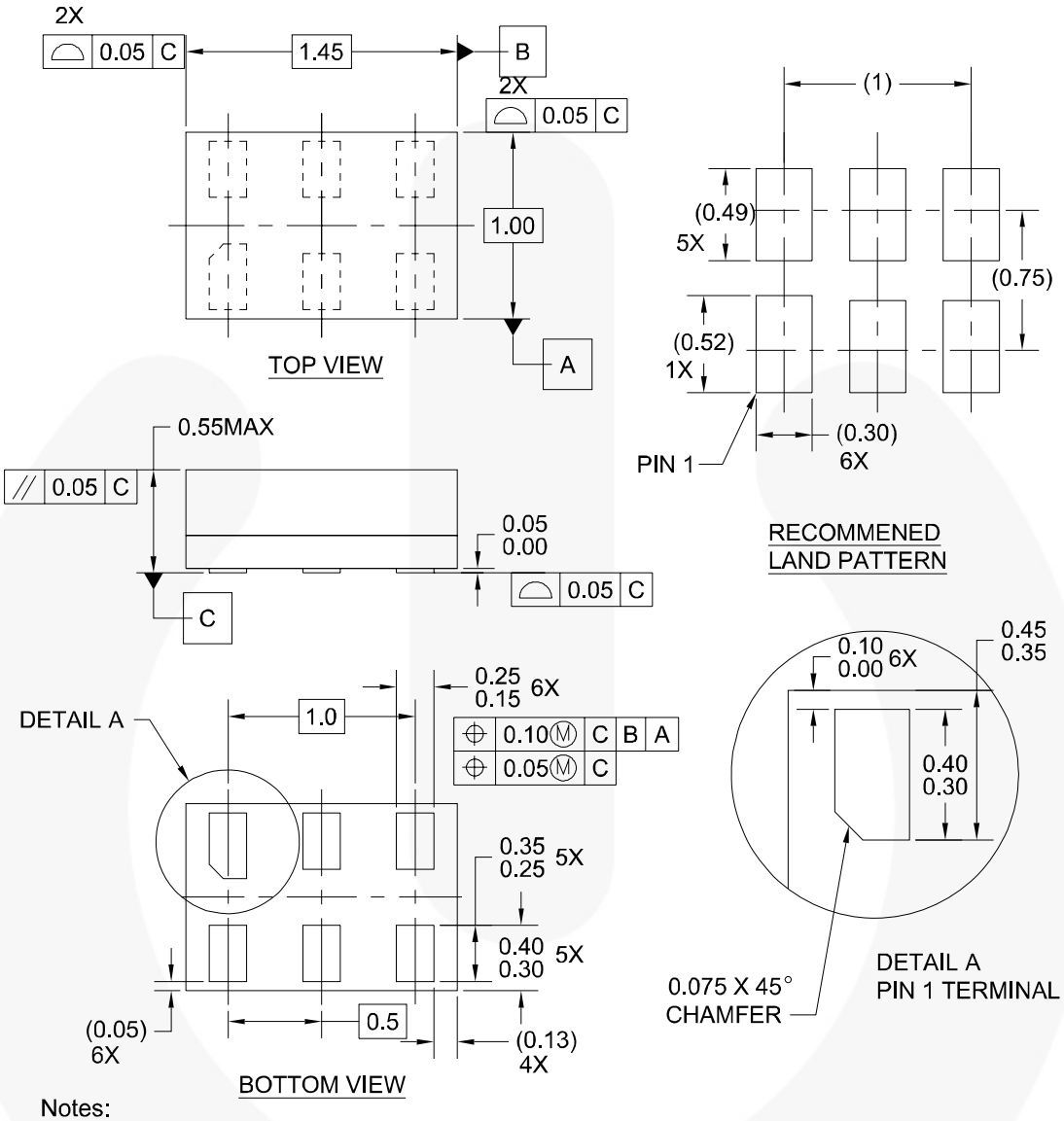

Figure 19. 6-Lead, MircoPak™ 1.0mm Wide Package

Note: click here for tape and reel specifcations, available at:

http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

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Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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