eala
Stereo Expander

Digital Signal Processor for 2ch Speaker System

■ General Description

The NJU26040-16A is a high performance 24-bit digital signal processor.

The NJU26040-16A provides 3D Surround function, Stereo Enhancement function, Equalizer function, Dynamic Bass Boost function, AGC/Limiter function. These kinds of sound functions are suitable for docking speaker, boom box, mini/micro-component, TV, and other speaker system.

■ Package

NJU26040V-16A

■ FEATURES

- Software

- 3D Surround: eala (NJRC Original)
  - Stable center image and natural sound field
- Stereo Enhancement: eala Stereo Expander (NJRC Original)
  - Reproduce the amazing stereo image even narrow distance between two speakers
- Equalizer
  - 5band biquad filter
  - Band1, 2, 3 : HPF/Parametric Equalizer/is selectable.
  - Band4,5 : HPF/Parametric Equalizer/Bass/Treble is selectable.
- Master Volume
- Dynamic Bass Boost (NJRC Original)
  - Two-independent-channel processing for high channel separation
- AGC/Limiter
- Clock for Watch Dog Timer

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz Max
- Digital Audio Interface : 3 Input port / 2 Output ports
- Digital Audio Format : I^2S 24bit, Left-justified, Right-justified, BCK : 32fs/64fs
- Master / Slave Mode : Master Mode MCK : 1/2 fclk, 1/3 fclk
  ex. MCK = 384Fs(1/2) or MCK = 256Fs(1/3) at fclk=768Fs
- Power Supply : 3.3V
- Input terminal : 5V Input tolerant
- Package : SSOP32 (Pb-Free)
- Micro computer interface : I^2C bus (standard-mode/100kbps, Fast-mode/400kbps)
  : Serial interface (4 lines: clock, enable, input data, output data)

The detail hardware specification is described in the " NJU26040 Series Data Sheet (NJU26040_E_REL.pdf)".

■ Function Block Diagram

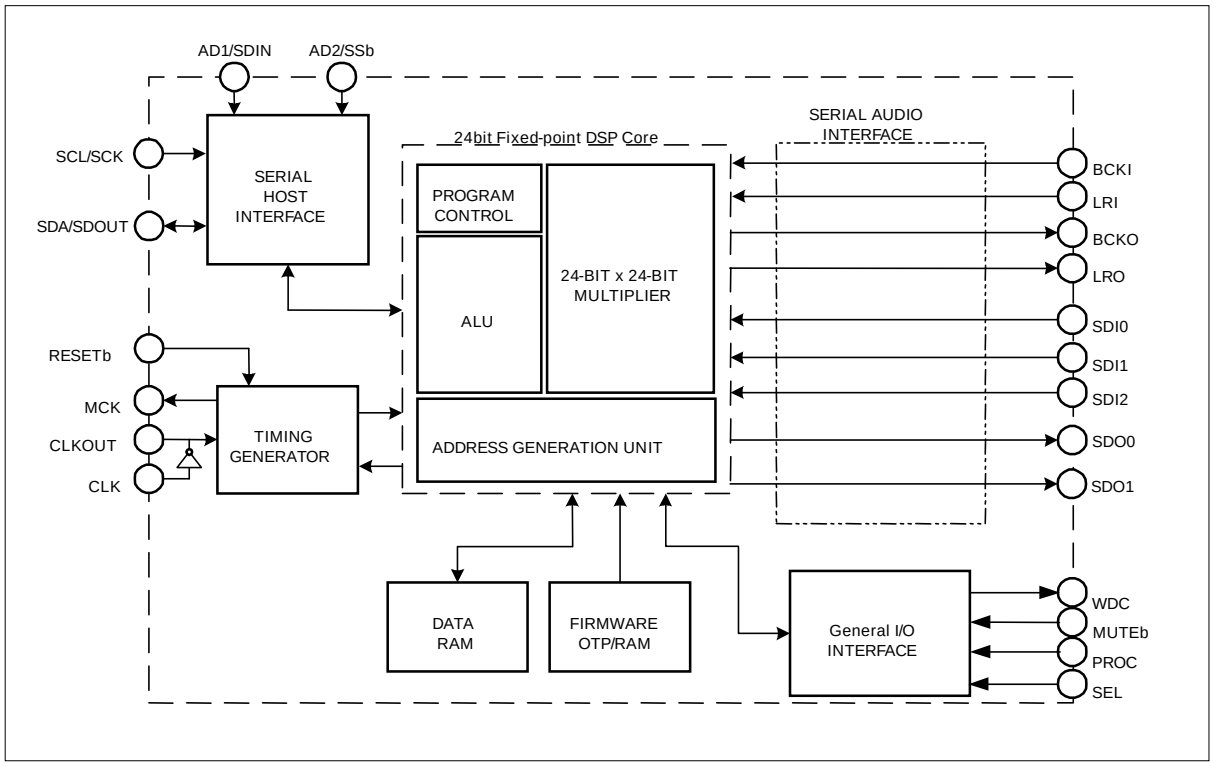


Fig. 1 NJU26040-16A Block Diagram

■ DSP Block Diagram

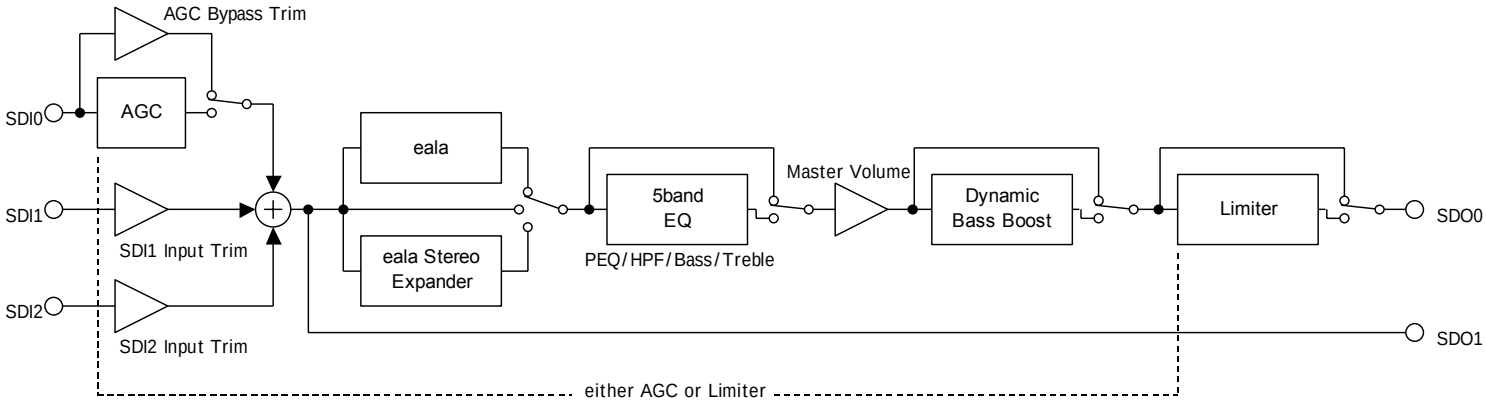


Fig. 2 NJU26040-16A Function Diagram

■ Pin Configuration

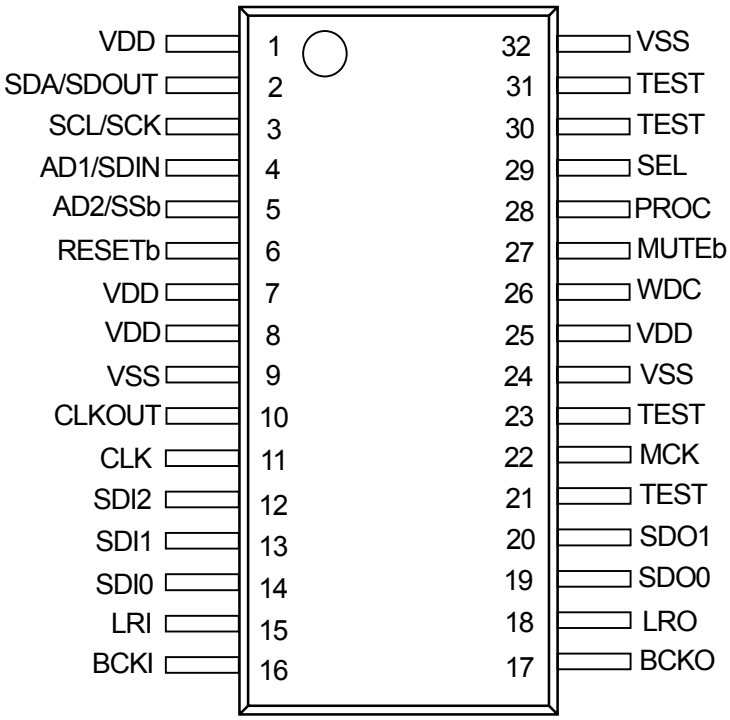


Fig. 3 NJU26040-16A Pin Configuration

■ Pin Description

Table 1 Pin Description

Pin No.	Symbol	I/O	Description
1, 7, 8, 25	VDD	-	Power Supply +3.3V
2	SDA / SDOUT	OD	I^2C I/O / 4-wire Serial Output This pin requires a pull-up.
3	SCL / SCK	I	I^2C Clock / Serial Clock
4	AD1 / SDIN	I	I^2C Address / Serial Input
5	AD2 / SSb	I	I^2C Address / Serial Enable
6	RESETb	I	Reset (RESETb='Low': DSP Reset)
9, 24, 32	VSS	-	GND
10	CLKOUT	O	OSC Output
11	CLK	I	OSC Clock Input
12	SDI2	I	Audio Data Input 2
13	SDI1	I	Audio Data Input 1
14	SDI0	I	Audio Data Input 0
15	LRI	I	LR Clock Input
16	BCKI	I	Bit Clock Input
17	BCKO	O	Bit Clock Output
18	LRO	O	LR Clock Output
19	SDO0	O	Audio Data Output 0
20	SDO1	O	Audio Data Output 1
21	TEST	O	for Test (Do not connect)
22	MCK	O	Master Clock Output for A/D, D/A
23, 30, 31	TEST	I -	for Test (connect to VSS)
26	WDC	I/O +	Watch Dog Clock Output (Open drain output)
27	MUTEb	I/O -	Master Volume level, After Reset DSP ,"1":0dB, "0": Mute
28	PROC	I/O -	After Reset DSP, "1": Normal, "0": Wait for start command
29	SEL	I/O -	Select I^2C or Serial bus ("1": Serial / "0": I^2C-bus)

Note : I : Input
I - : Input (Pull-down)
O : Output
O + : Output (with Pull-up resistance)
OD : Bi-directional (Open Drain) This pin requires a pull-up resistance.

■ Digital Audio Interface

The NJU26040-16A audio interface provides industry standard serial data format of I^2S. The NJU26040-16A audio interface provides three audio data inputs, two audio data outputs as shown in table 2, table 3.

Table 2 Serial Audio Input Pin

Pin No.	Symbol	Description
14	SDI0	Audio Data Input 0 L / R
13	SDI1	Audio Data Input 1 L / R
12	SDI2	Audio Data Input 2 L / R

Table 3 Serial Audio Output Pin

Pin No.	Symbol	Description
19	SDO0	Audio Data Output 0 L / R
20	SDO1	Audio Data Output 1 L / R

■ Host Interface

The NJU26040-14A can be controlled via Serial Host Interface (SHI) using either of two serial bus formats:I^2C bus or 4-Wire serial bus.(Table 4) Data transfers are in 8-bit packets (1 byte) when using either format.

Table 4 Serial Host Interface Pin Description

Pin No.	Symbol	Setting	Host Interface
29	SEL	"Low"	I^2C bus
		"High"	4-Wire serial bus

Table 5 Serial Host Interface Pin Description

Pin No.	Symbol (I^2C bus / Serial)	I^2C bus Format	4-Wire Serial bus Format
2	SDA / SDOUT *	Serial Data Input/Output (Open Drain Input/Output)	Serial Data Output (Open-Drain Output)
3	SCL / SCK *	Serial Clock	Serial Clock
4	AD1 / SDIN *	I^2C bus address Bit1	Serial Data Input
5	AD2 / SSb *	I^2C bus address Bit2	Serial enable

Note : SDA pin is a bi-directional open drain.
This pin requires a pull-up resistance in both I^2C bus and 4-Wire serial mode.
When the power supply (V_{DD}= +3.3V) is supplied to NJU26040-16A, these pins become +5.0V Input tolerant.

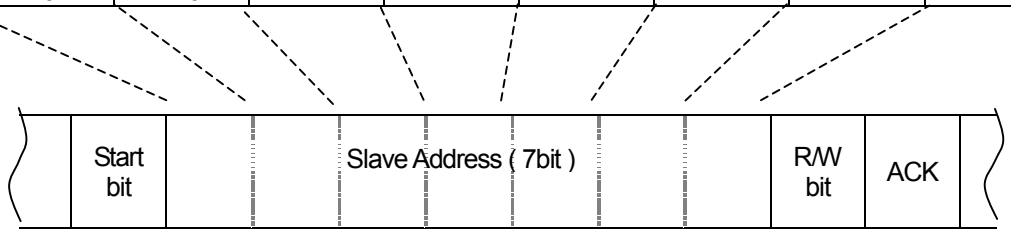
■ I²C bus

I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 6) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26040-16A. An address can be arbitrarily set up by the AD1 and AD2 pins. The I²C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

Table 6 I²C bus SLAVE Address

bit7	bit6	bit5	bit4	bit3	AD2 bit2	AD1 bit1	R/W bit0
0	0	1	1	1	0	0	R/W
0	0	1	1	1	0	1	
0	0	1	1	1	1	0	
0	0	1	1	1	1	1	



* SLAVE address is 0 when AD1/2 is "Low". SLAVE address is 1 when AD1/2 is "High".

Note : The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I²C bus data transfer.

■ 4-Wire Serial Interface

SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin Low (SSb=0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSb.

SDOUT is Hi-Z in case of SSb = "High". SDOUT is Open-drain output in case of SSb = "Low". SDOUT needs a pull-up resistor when SDOUT is Hi-Z.

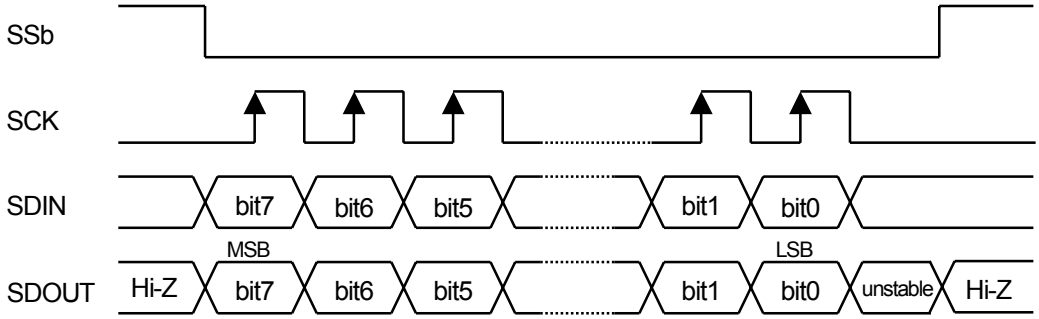


Fig.4 4-Wire Serial Interface Timing

Note: When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSb="High". When the data-clock is more than 8 clocks, the last 8 bit data becomes valid. After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSb becomes "High".

■ Pin setting

The NJU26040-16A operates default command setting after resetting the NJU26040-16A. In addition, the NJU26040-16A restricts operation at power on by setting PROC pin and MUTEb pin (Table 8). These pins are input pin. However, these pins operate as bi-directional pins. Connect with V_{DDIO} or V_{SSIO} through 3.3kΩ resistance.

Table 7 Pin setting

Pin No.	Symbol	Setting	Function
28	PROC	"High"	The NJU26040-16A operates default setting after reset.
		"Low"	The NJU26040-16A does not operate after reset. Sending start command is required for starting operation.
27	MUTEb	"High"	Master volume is set 0dB after reset.
		"Low"	Master volume is set mute after reset.

■ Watch Dog Clock

The NJU26040-16A outputs clock pulse through WDC (No.26) pin during normal operation. (Table 9)

Table 8 Watch Dog Clock Output Cycle

WDC Output Cycle (Low/High) Time
100ms

The NJU26040-16A generates a clock pulse through the WDC terminal after resetting the NJU26040-16A. The WDC clock is useful to check the status of the NJU26040-16A operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26040-16A. When the WDC clock pulse is lost or not normal clock cycle, the NJU26040-16A does not operate correctly. Then reset the NJU26040-16A and set up the NJU26040-16A again.

Note: If input and output of an audio signal stop and an audio interface stops, WDC can't output.
That is because it has controlled based on the signal of an audio interface.

■ NJU2604016A Command Table

Table 9 NJU26040-16A Command

No.	Command
1	System State Command
2	Sample Rate Select Command
3	Set Task Command
4	Smooth Control Config Command
5	Master Volume Control Command
6	Master Volume Balance Setup Command
7	AGC/Limiter Threshold Level Command
8	AGC/Limiter Noise Compressor Level Command
9	AGC/Limiter Ratio Command
10	AGC/Limiter Attack Time / Release Time Command
11	AGC/Limiter Output Boost Command
12	AGC Bypass Trim Command
13	SDI1 Input Trim Command
14	SDI2 Input Trim Command
15	eala Surround Gain Command

No.	Command
16	eala Stereo Expander Effect mode Command
17	EQ Mode Setup Command
18	EQ f0 Command
19	EQ Q Command
20	EQ Gain Command
21	DBB Start Level Command
22	DBB Limit Level Command
23	DBB Effect Command
24	DBB Control Command
25	DBB Attack Time / Release Time Command
26	DBB LPF fc Command
27	DBB Treble Boost Level Command
28	Version No. Request Command
29	Revision No. Request Command
30	Start Command
31	No Operation Command

Notes : In respect to detail command information, request New Japan Radio Co., Ltd.

Ver. 1.00