LM34914 Evaluation Board

National Semiconductor
Application Note 1549
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Introduction

The LM34914EVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 5V output over an input range of 8V to 40V. The circuit delivers load currents to 1A, with current limit set at ≅1.2A. The board is populated with all components except R3, C2, C11 and C12. These components provide options for managing the output ripple as described later in this document.

The board's specification are:

- Input Voltage: 8V to 40V
- Output Voltage: 5V
- Maximum load current: 1.0A
- Minimum load current: 0A
- Current Limit: ≅1.2A (Vin = 8V)
- Measured Efficiency: 94.5% (V_{IN} = 8V, I_{OUT} = 200 mA)
- Nominal Switching Frequency: 275 kHz
- Size: 2.0 in. x 1.0 in. x 0.53 in

Example Circuit

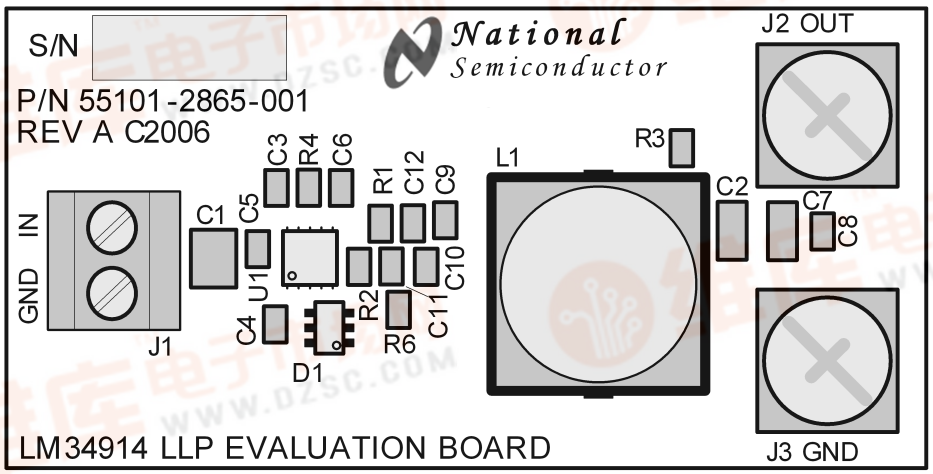


FIGURE 1. Evaluation Board - Top Side

Theory of Operation

Refer to the evaluation board schematic in Figure 5, which contains a simplified block diagram of the LM34914. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R4 and VIN according to the equation:

$$t_{ON} = \frac{1.15 \times 10^{-10} \times (R4 + 1.4k)}{(V_{IN} - 1.5V)} + 50\ ns$$

The on-time of this evaluation board ranges from ≅2700 ns at VIN = 8V, to ≅500 ns at VIN = 40V. The on-time varies inversely with VIN to maintain a nearly constant switching frequency. At the end of each on-time the Minimum Off-Timer ensures the buck switch is off for at least 265 ns. In normal operation, the off-time is much longer. During the off-time, the load current is supplied by the output capacitor (C7). When the output voltage falls sufficiently that the voltage at FB is below 2.5V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at FB to switch the regulation comparator. The current limit threshold, which varies with Vin, is ≅1.2A at Vin = 8V, and ≅1.05A at Vin = 40V. Refer to the LM34914 data sheet for a more detailed block diagram, and a complete description of the various functional blocks.

Board Layout and Probing

The pictorial in Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

1) When operating at high input voltage and high load current, forced air flow may be necessary.

2) The LM34914, and diode D1 may be hot to the touch when operating at high input voltage and high load current.

3) Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.

4) At maximum load current (1A), the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

Board Connection/Start-up

The input connections are made to the J1 connector. The load is connected to the J2 (OUT) and J3 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 8V, at which time the output voltage should be 5V. If the output voltage is correct with 8V at VIN, then increase the input voltage as desired and proceed with evaluating the circuit. DO NOT EXCEED 40V AT VIN.

Output Ripple Control

The LM34914 requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW pin, for proper operation. The required ripple can be supplied from ripple at V_{OUT}, through the feedback resistors, as described in options B and C below, or the ripple can be generated separately (using R6, C9, C10) keeping the ripple at V_{OUT} to a minimum as described in option A below.

A) **Minimum Output Ripple:** This evaluation board is supplied configured for minimum ripple at V_{OUT} by using components R6, C9 and C10. The output ripple, which ranges from ≅3mVp-p at V_{IN} = 8V to ≅8 mVp-p at V_{IN} = 40V, is determined primarily by the ESR of output capacitor (C7), and the inductor's ripple current, which ranges from 85 mAp-p to 190 mAp-p over the input voltage range. The ripple voltage required by the FB pin is generated by R6, C9 and C10 since the SW pin switches from -1V to V_{IN}, and the right end of C9 is a virtual ground. The values for R6 and C9 are chosen to generate a 30-40 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through C10. The following procedure is used to calculate values for R6, C9 and C10:

1) Calculate the voltage V_A:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN})))$$

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1V), and V_{IN} is the minimum input voltage. For this circuit V_A calculates to 4.63V. This is the approximate DC voltage at the R6/C9 junction, and is used in the next equation.

2) Calculate the R6 x C9 product:

$$R6 \times C9 = \frac{(V_{IN} - V_A) \times t_{ON}}{\Delta V}$$

where t_{ON} is the maximum on-time (≅2700 ns), V_{IN} is the minimum input voltage, and ΔV is the desired ripple amplitude at the R6/C9 junction, 30 mVp-p for this example.

$$R6 \times C9 = \frac{(8V - 4.63V) \times 2700\ ns}{0.03V} = 3.03 \times 10^{-4}$$

R6 and C9 are then chosen from standard value components to satisfy the above product. For example, C9 can be 3300 pF requiring R6 to be ≤91.8 kΩ. C10 is chosen to be 0.01 µF, large compared to C9. The circuit as supplied on this EVB is shown in Figure 2.

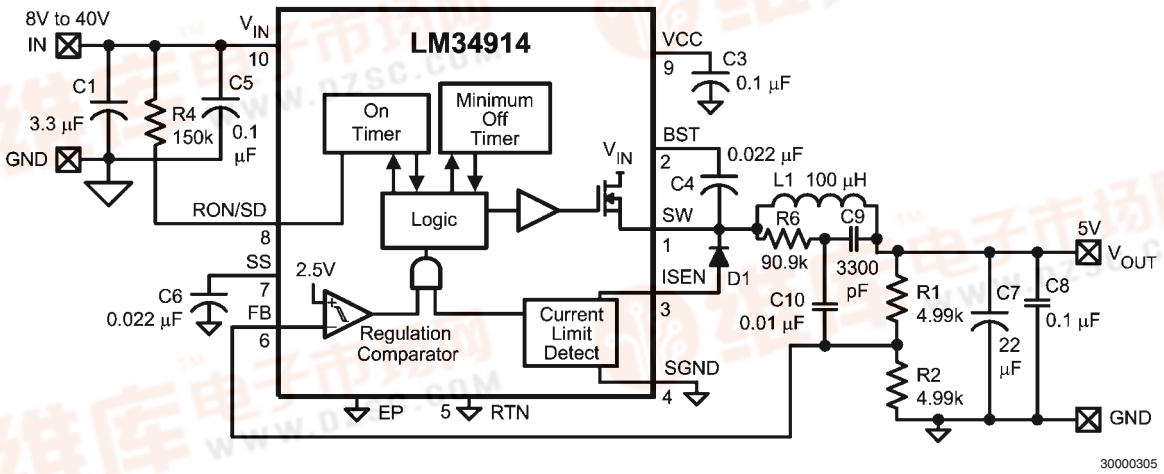


FIGURE 2. Minimum Output Ripple Configuration Using R6,C9,C10

B) **Intermediate Ripple Level Configuration:** This configuration generates more ripple at V_{OUT} than the above configuration, but uses two less capacitors. If some ripple can be tolerated in the application, this configuration is slightly more economical, and simpler. R3, C2 and C12 are used instead of R6 and C7-C10, as shown in Figure 3.

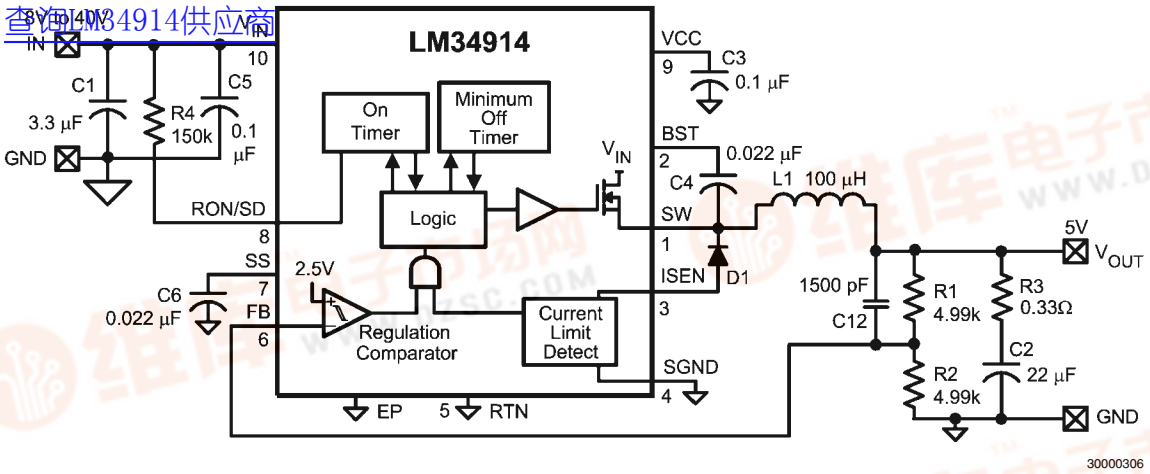


FIGURE 3. Intermediate Ripple Configuration Using C12 and R3

R3 is chosen to generate 25-30 mVp-p at V_{OUT} knowing that the minimum ripple current is 85 mAp-p at minimum V_{IN}. C12 couples that ripple to the FB pin without the attenuation of the feedback resistors. C12's minimum value is calculated from:

$$C12 \geq \frac{t_{ON(max)}}{(R1//R2)}$$

where $t_{ON(max)}$ is the maximum on-time (at minimum V_{IN}), and R1//R2 is the equivalent parallel value of the feedback resistors. For this evaluation board $t_{ON(max)}$ is approximately 2700 ns, and R1//R2 = 2.5 kΩ, and C12 calculates to a minimum of 1080 pF. In the circuit of Figure 3 the ripple at V_{OUT} ranges from ≅30 mVp-p to ≅63 mVp-p over the input voltage range.

C) **Lowest Cost Configuration:** This configuration is the same as option B above, but without C12. Since ≥25 mVp-p are required at the FB pin, R3 is chosen to generate ≥50 mV at V_{OUT}, knowing that the minimum ripple current in this circuit is 85 mAp-p at minimum V_{IN}. Using 0.68Ω for R3, the ripple at V_{OUT} ranges from ≅60 mVp-p to ≅120 mVp-p over the input voltage range. If the application can tolerate this ripple level, this is the most economical solution. The circuit is shown in Figure 4.

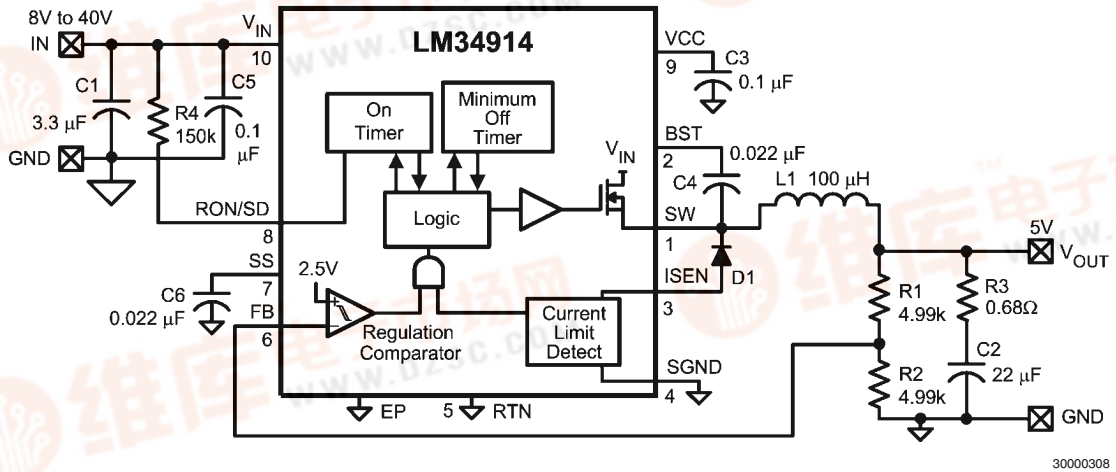


FIGURE 4. Lowest Cost Configuration

Minimum Load Current

The LM34914 requires a minimum load current of ≅500 µA to ensure the boost capacitor (C4) is recharged sufficiently during each off-time. In this evaluation board, the minimum load current is provided by the feedback resistor (R1, R2), allowing the board's minimum load current V_{OUT} to be specified at zero.

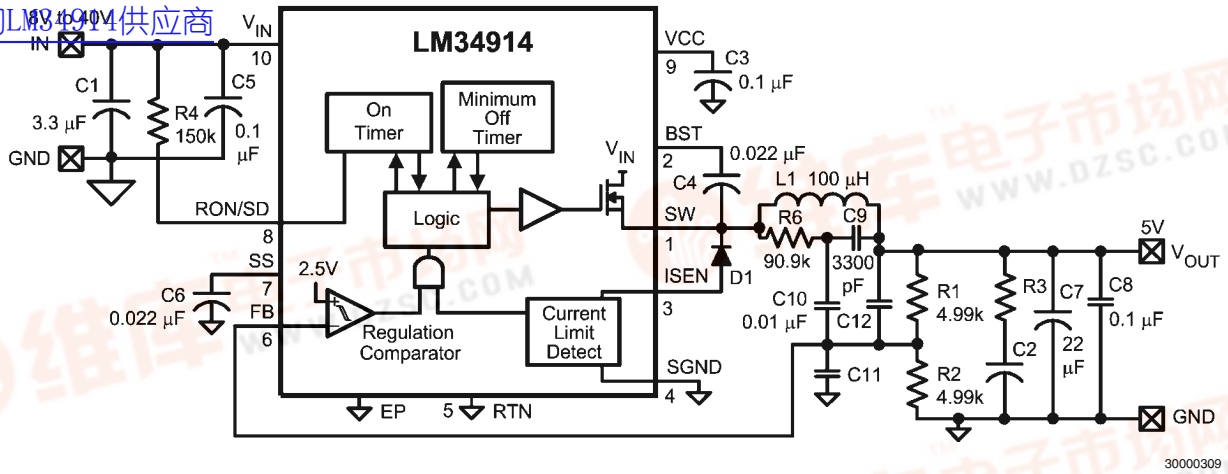


FIGURE 5. Complete Evaluation Board Schematic

Item	Description	Mfg., Part Number	Package	Value
C1	Ceramic Capacitor	TDK C3225X7R1H475M	1210	4.7 µF, 50V
C2	Ceramic Capacitor	Unpopulated	1206	
C3	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 16V
C4	Ceramic Capacitor	TDK C2012X7R1C104M	0805	0.022 µF, 16V
C5	Ceramic Capacitor	TDK C2012X7R1C223M	0805	0.1 µF, 100V
C6	Ceramic Capacitor	TDK C2012X7R1C223M	0805	0.022 µF, 16V
C7	Ceramic Capacitor	TDK C3225X7R1C226M	1206	22 µF, 16V
C8	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 16V
C9	Ceramic Capacitor	TDK C2012X7R2A332M	0805	3300 pF
C10	Ceramic Capacitor	TDK C2012X7R2A103M	0805	0.01 µF
C11	Ceramic Capacitor	Unpopulated	0805	
C12	Ceramic Capacitor	Unpopulated	0805	
D1	Schottky Diode	Zetex ZLLS2000	SOT23-6	40V, 2.2A
L1	Power Inductor	TDK SLF12575T-101M1R9, or Cooper Bussmann DR125-101	12.5 mm x 12.5 mm	100 µH, 1.9A
R1	Resistor	CRCW08054991F	0805	4.99 kΩ
R2	Resistor	CRCW08054991F	0805	4.99 kΩ
R3	Resistor	Unpopulated	0805	
R4	Resistor	CRCW08051503F	0805	150 kΩ
R6	Resistor	CRCW08059092F	0805	90.9 kΩ
U1	Switching Regulator	National Semiconductor LM34914SD	LLP 3x3	

Circuit Performance

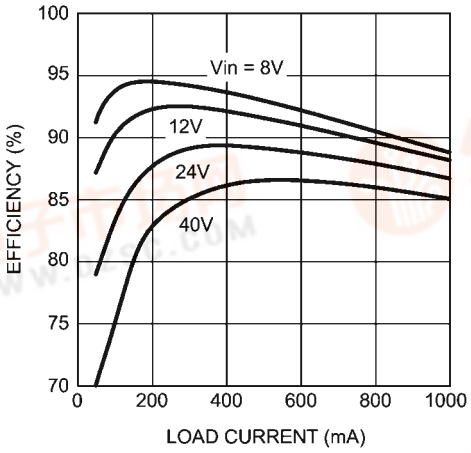


FIGURE 6. Efficiency vs Load Current

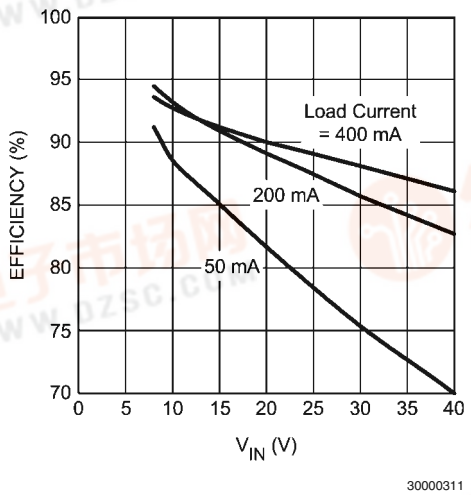


FIGURE 7. Efficiency vs Input Voltage

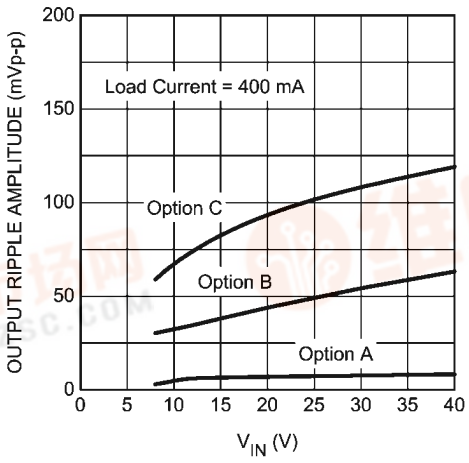


FIGURE 8. Output Voltage Ripple

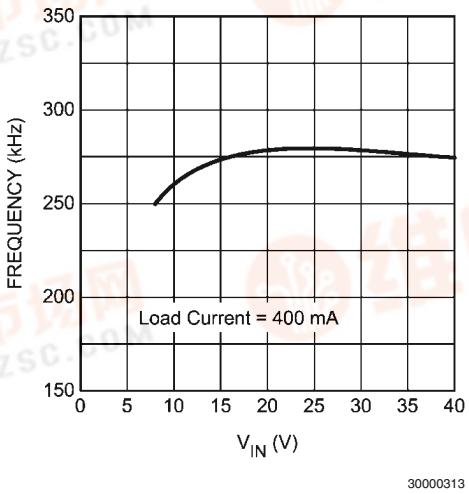


FIGURE 9. Switching Frequency vs. Load Current

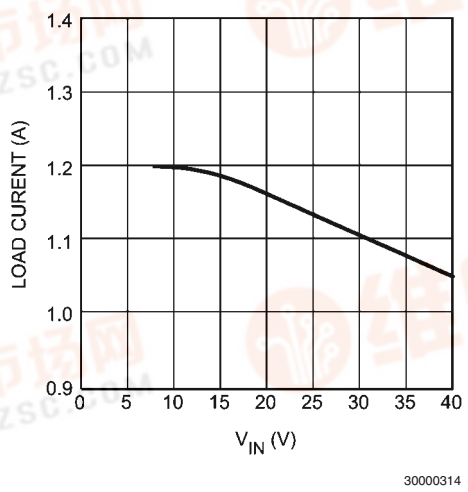
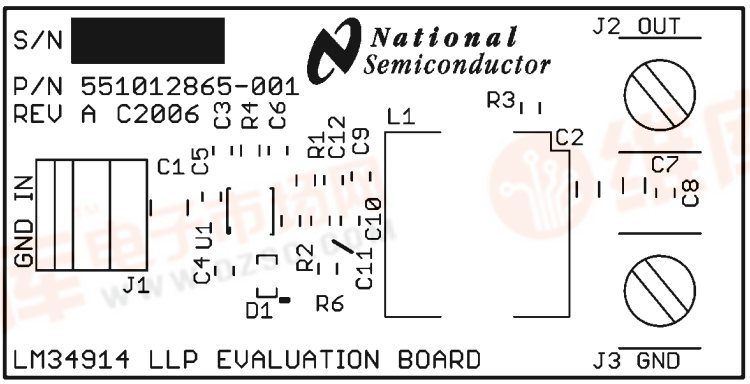


FIGURE 10. Current Limit vs Input Voltage

PC Board Layout



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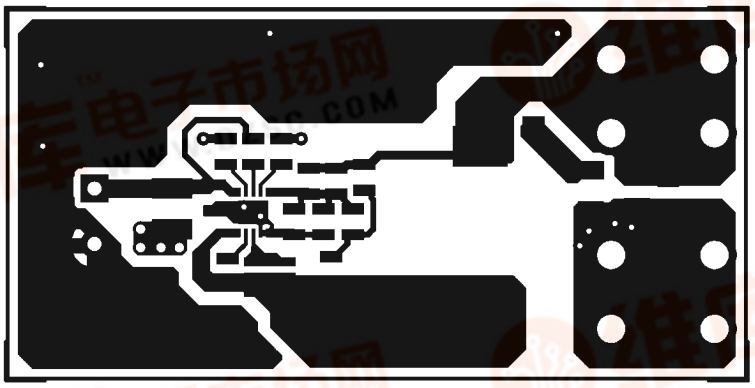
Board Silkscreen



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Board Top Layer

30000328

Board Bottom Layer (Viewed from Top)

Notes

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