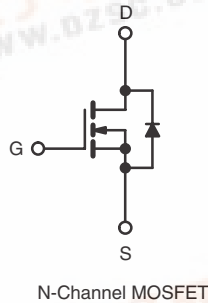
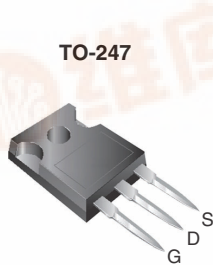


## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	1.2
$Q_g$ (Max.) (nC)	60	
$Q_{gs}$ (nC)	8.3	
$Q_{gd}$ (nC)	30	
Configuration	Single	



### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available



RoHS\*  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

### ORDERING INFORMATION

Package	TO-247
Lead (Pb)-free	IRFPC40PbF
	SiHFPC40-E3
SnPb	IRFPC40
	SiHFPC40

### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	27	
Linear Derating Factor		1.2	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	410	mJ
Maximum Power Dissipation	$P_D$	150	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	3.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 16\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 6.8\text{ A}$  (see fig. 12).
- $I_{SD} \leq 6.8\text{ A}$ ,  $dI/dt \leq 80\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.83	

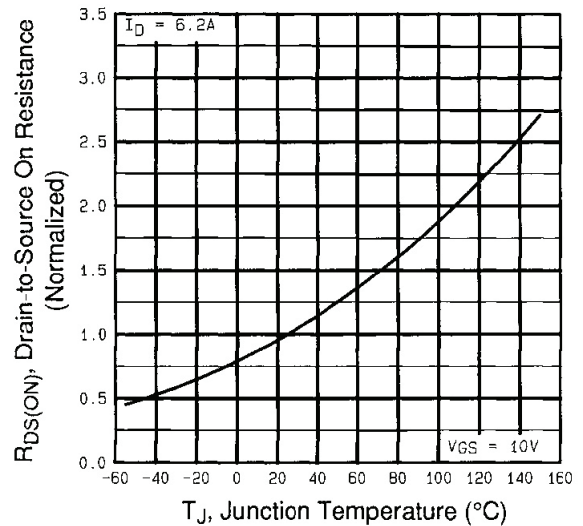
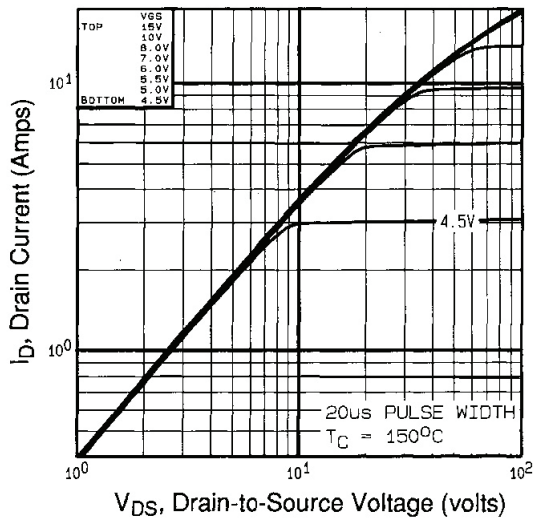
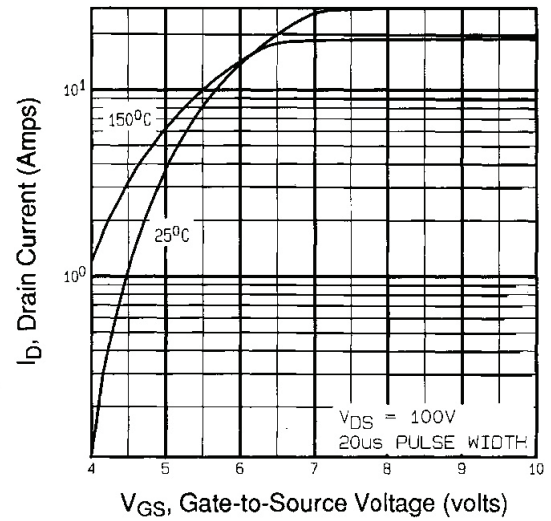
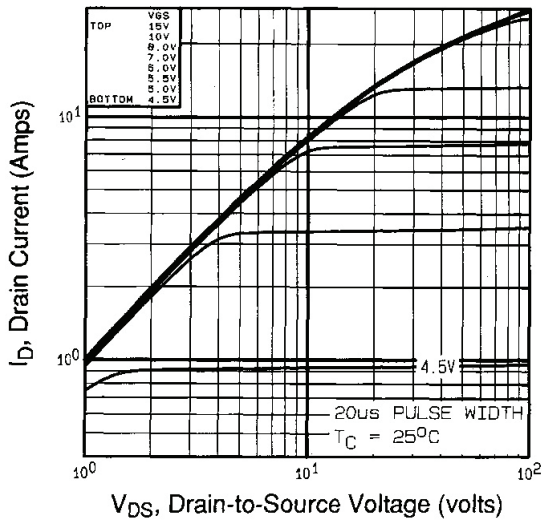
**SPECIFICATIONS**  $T_J = 25\text{ °C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	100	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.1 A <sup>b</sup>	-	-	1.2	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 4.1 A <sup>b</sup>		4.9	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1300	-	pF
Output Capacitance	C <sub>oss</sub>			-	160	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	30	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 6.2 A, V <sub>DS</sub> = 360 V, see fig. 6 and 13 <sup>b</sup>	-	-	60	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	8.3	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	30	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 6.2 A , R <sub>G</sub> = 9.1 Ω, R <sub>D</sub> = 47 Ω, see fig. 10 <sup>b</sup>		-	13	-	ns
Rise Time	t <sub>r</sub>			-	18	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	55	-	
Fall Time	t <sub>f</sub>			-	20	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.8	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	27	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 6.8 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 6.2 A, dI/dt = 100 A/μs <sup>b</sup>		-	450	940	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	3.8	7.9	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



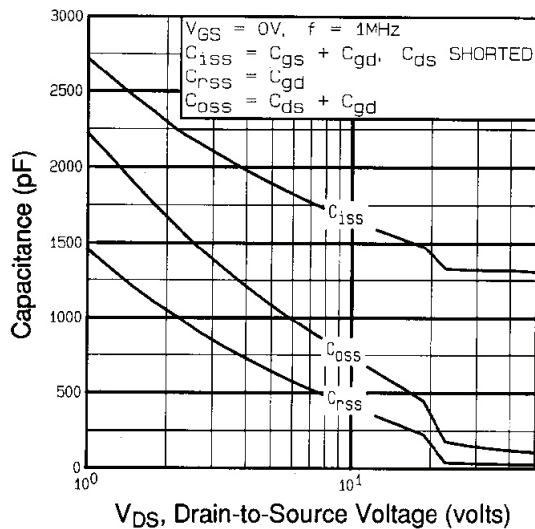


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

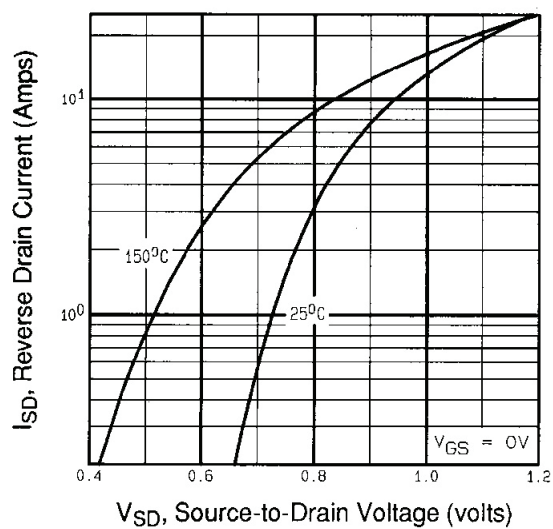


Fig. 7 - Typical Source-Drain Diode Forward Voltage

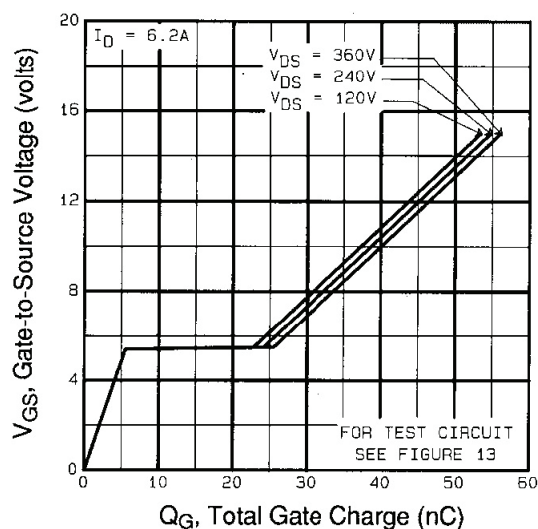


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

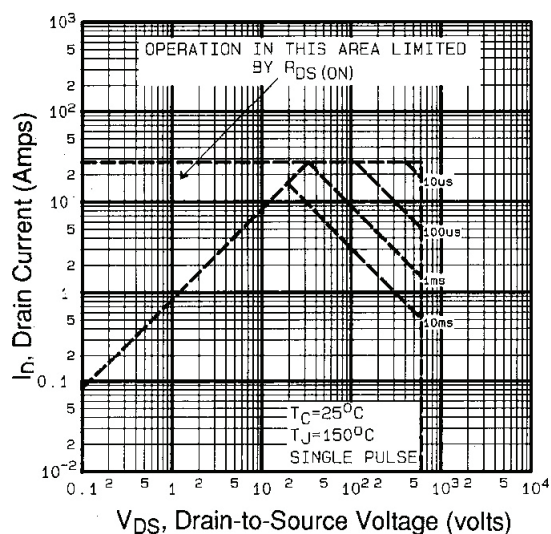
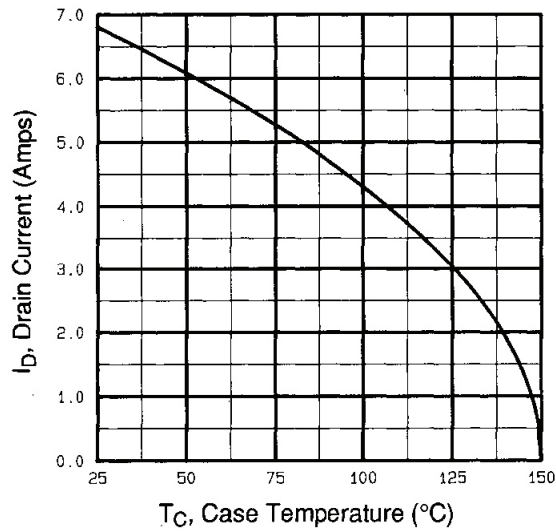


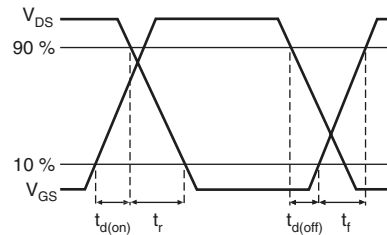
Fig. 8 - Maximum Safe Operating Area



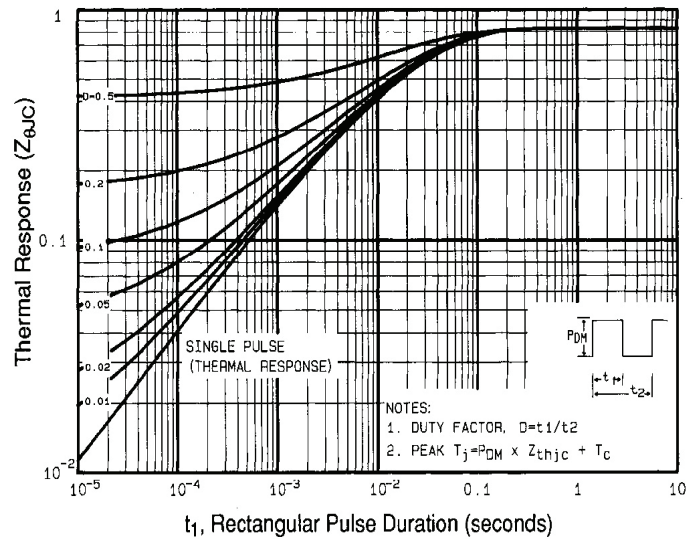
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

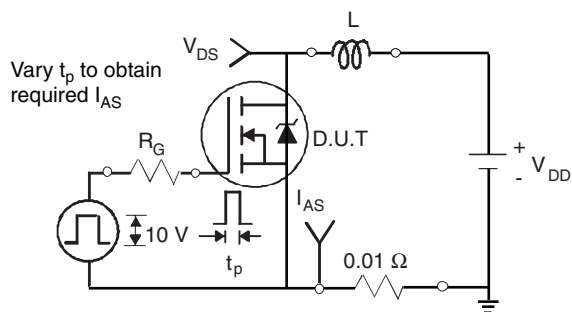


Fig. 12a - Unclamped Inductive Test Circuit

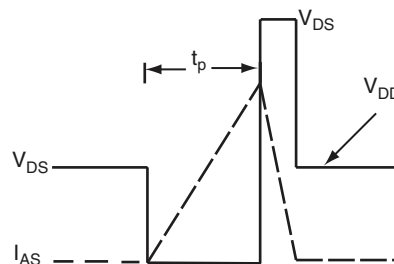


Fig. 12b - Unclamped Inductive Waveforms

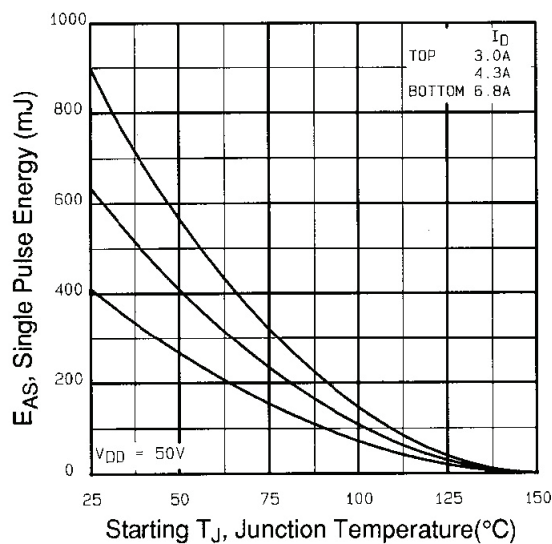


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

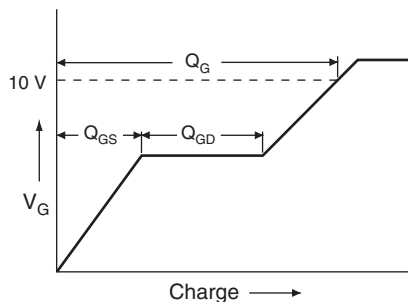


Fig. 13a - Basic Gate Charge Waveform

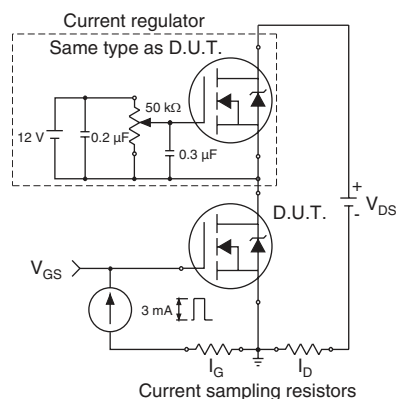
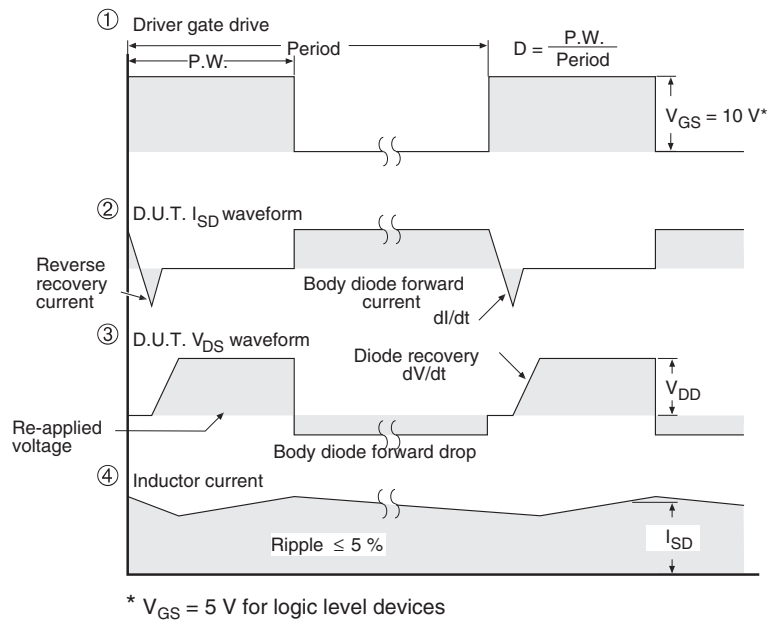
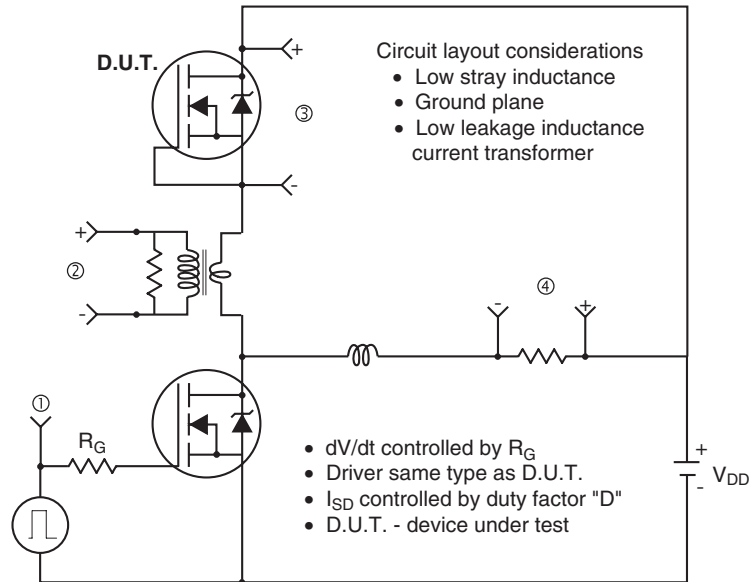


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery $dV/dt$ Test Circuit



**Fig.14 - For N-Channel**

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