

INTEGRATED CIRCUITS

DATA SHEET

PCA8521

Infrared remote control transmitter RC5

Product specification

1999 Jun 15

Supersedes data of 1997 Jul 03

File under Integrated Circuits, IC02

Infrared remote control transmitter RC5**PCA8521****FEATURES**

- RC5 protocol
- Maximum of:
 - 56 keys (20-pin version)
 - 30 keys (16-pin version).
- Option of multi-system or single system transmitter
 - Multi-system: maximum 8 systems, selection by key
 - Single system: maximum 8 different systems per IC, selection by jumper wire or switch.
- Power-down and key wake-up
- High output current (≤ 45 mA)
- Oscillator frequency of 432 kHz or 4 MHz
- Multiple key protection
- Option of 25% or 33% duty factor
- Contained in DIP16, SO16, DIP20 or SO20 packages.

GENERAL DESCRIPTION

The PCA8521 can be used in infrared remote control transmitters. It generates output pulses, in accordance with the RC5 protocol, when a key is pressed. The IC does not contain a software programmable processor. However, it does contain a ROM in which the codes that have to be transmitted are stored. An example of an application diagram using a 20-pin IC is illustrated in Fig.7. The oscillator frequency may be optionally chosen as 432 kHz or 4 MHz. For 432 kHz additional external capacitors must be connected. The capacitors for a 4 MHz oscillator is integrated. When a key in the key-matrix is pressed a drive line will be connected to a sense line. This causes the oscillator to start and a corresponding code will be generated conforming to the RC5 protocol.

Seven drive lines ($\overline{DR0}$ to $\overline{DR6}$) and eight sense lines (SN0 to SN7) may be connected via the key matrix to scan the keys (see Fig.1).

When two or more keys are activated simultaneously no transmission will take place.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8521FP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
PCA8521FT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA8521BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCA8521BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

Infrared remote control transmitter RC5

PCA8521

BLOCK DIAGRAM

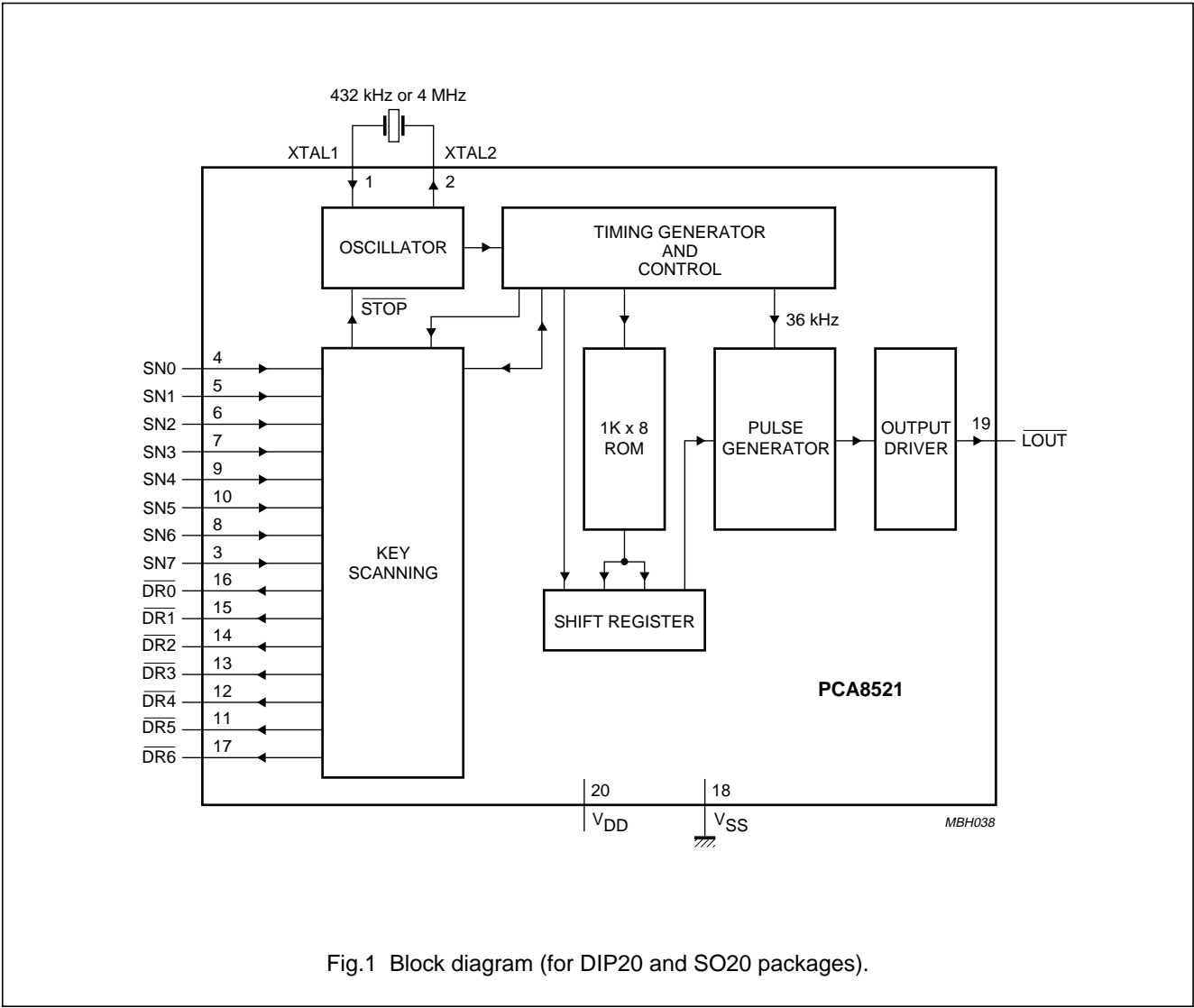


Fig.1 Block diagram (for DIP20 and SO20 packages).

Infrared remote control transmitter RC5

PCA8521

PINNING

16-pin dual in-line and small outline package

SYMBOL	PIN	DESCRIPTION
XTAL1	1	oscillator input
XTAL2	2	oscillator output
SN0	3	sense line 0 for key matrix
SN1	4	sense line 1 for key matrix
SN2	5	sense line 2 for key matrix
SN3	6	sense line 3 for key matrix
SN4	7	sense line 4 for key matrix
SN5	8	sense line 5 for key matrix
$\overline{\text{DR4}}$	9	drive line 4 for key matrix (active LOW)
$\overline{\text{DR3}}$	10	drive line 3 for key matrix (active LOW)
$\overline{\text{DR2}}$	11	drive line 2 for key matrix (active LOW)
$\overline{\text{DR1}}$	12	drive line 1 for key matrix (active LOW)
$\overline{\text{DR0}}$	13	drive line 0 for key matrix (active LOW)
V_{SS}	14	ground
$\overline{\text{LOUT}}$	15	output signal (active LOW)
V_{DD}	16	power supply

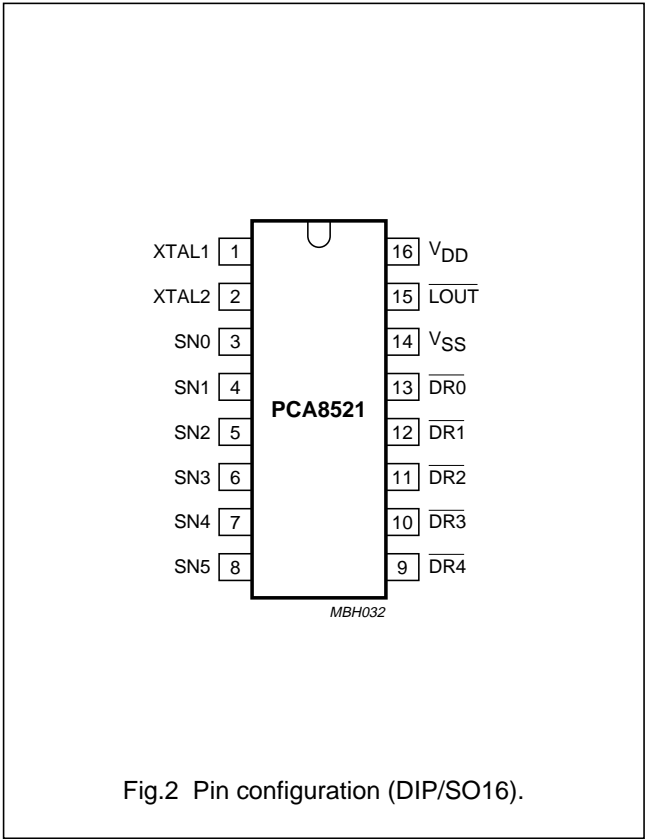


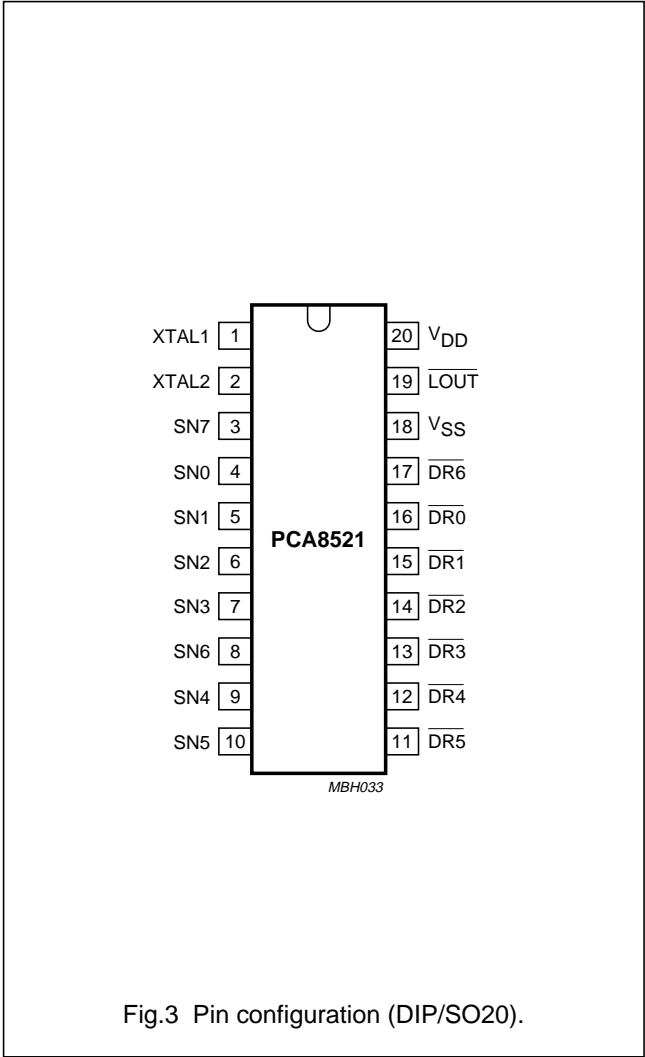
Fig.2 Pin configuration (DIP/SO16).

Infrared remote control transmitter RC5

PCA8521

20-pin dual in-line and small outline package

SYMBOL	PIN	DESCRIPTION
XTAL1	1	oscillator input
XTAL2	2	oscillator output
SN7	3	sense line 7 for key matrix
SN0	4	sense line 0 for key matrix
SN1	5	sense line 1 for key matrix
SN2	6	sense line 2 for key matrix
SN3	7	sense line 3 for key matrix
SN6	8	sense line 6 for key matrix
SN4	9	sense line 4 for key matrix
SN5	10	sense line 5 for key matrix
$\overline{\text{DR5}}$	11	drive line 5 for key matrix (active LOW)
$\overline{\text{DR4}}$	12	drive line 4 for key matrix (active LOW)
$\overline{\text{DR3}}$	13	drive line 3 for key matrix (active LOW)
$\overline{\text{DR2}}$	14	drive line 2 for key matrix (active LOW)
$\overline{\text{DR1}}$	15	drive line 1 for key matrix (active LOW)
$\overline{\text{DR0}}$	16	drive line 0 for key matrix (active LOW)
$\overline{\text{DR6}}$	17	drive line 6 for key matrix (active LOW)
V_{SS}	18	ground
$\overline{\text{LOUT}}$	19	output signal (active LOW)
V_{DD}	20	power supply



Infrared remote control transmitter RC5

PCA8521

FUNCTIONAL DESCRIPTION

Key numbering for the matrix is given in Tables 1 and 2.

Table 1 Key numbering for 16-pin package

DRIVER LINES	SENSE LINES					
	SN0	SN1	SN2	SN3	SN4	SN5
DR0	0	1	2	3	4	5
DR1	8	9	10	11	12	13
DR2	16	17	18	19	20	21
DR3	24	25	26	27	28	29
DR4	32	33	34	35	36	37

Table 2 Key numbering for 20-pin package

DRIVER LINES	SENSE LINES							
	SN0	SN1	SN2	SN3	SN4	SN5	SN6	SN7
DR0	0	1	2	3	4	5	6	7
DR1	8	9	10	11	12	13	14	15
DR2	16	17	18	19	20	21	22	23
DR3	24	25	26	27	28	29	30	31
DR4	32	33	34	35	36	37	38	39
DR5	40	41	42	43	44	45	46	47
DR6	48	49	50	51	52	53	54	55

When the keys have been scanned the key-number of the activated key serves as the address of the ROM to obtain the required code-word. When a 16-pin IC is used the following sense lines and driver lines will not be connected; SN6, SN7, DR5 and DR6. Consequently, key numbers 6, 7, 14, 15, 22, 23, 30, 31, 38, 39 and 40 to 55 will not be addressed.

The ROM contains 8 banks of 64 code-words. Thus for each key a maximum of 8 different code-words may be generated. With multi-system use, 8 different systems (e.g. TV, VCR, tuner, CD etc.) may be selected. Apart from the system bits the command bits may also be different in different banks (true multi-function keys). Selection can be performed using the keys. For each key three bank select bits are present that determine which bank will be selected for the next key.

For each key an 'inhibit' bit is also present. When this bit is at logic 1 at an address in a given bank, and when the corresponding key is pressed (when this bank has been selected) no transmission will take place.

A single system option is available however, whereby instead of keys a jumper wire and/or a switch may be used for bank selection. Using this option it is possible to program different transmitter models in one IC and select the required bank by means of a jumper wire. Instead of a jumper wire a side-switch may also be used to change the generated code temporarily (select different bank) to obtain multi-function keys. With this option the jumper wires or switch must be connected between sense line SN0 and one of the drive lines DR0 to DR6 or ground. This means that SN0 cannot be used to connect keys and the maximum number of keys will be 25 keys for a 16-pin package and 49 keys for a 20-pin package.

It is not possible to use a combination of jumper wires and selection keys for bank selection in one unit.

The output of the ROM is loaded into a shift register that provides the input bits for the pulse generator. This pulse generator drives the output pin.

Infrared remote control transmitter RC5

PCA8521

Timing generator

A schematic diagram of the timing generator is illustrated in Fig.4. The oscillator frequency is 432 kHz or 4 MHz. The timing generator is stopped when no key is activated and started again when a key is pressed.

The output of the oscillator (CLK1) is divided by 111 for 4 MHz or by 12 for 432 kHz. Selection is achieved using a mask option. The output of the divider is CLK2 which is used for clocking of the control timer. The frequency of CLK2 is 36 kHz and the inverse is used to generate the output pulses in the subcarrier frequency. By mask option the duty factor can be chosen to be 25% or 33%.

The control timer has a length of 4096 subcarrier (pulse) periods. This is equal to the transmission repetition time. A bit time is equal to 64 pulses and the repetition time is 64 bit times. The control timer provides the timing of the key scanning, the ROM access and the code transmission. When the control timer has arrived at a certain state, and no key has been pressed for at least 28 ms, a stop signal will be generated which will stop the oscillator. All drive lines will then be set to logic 0. As soon as a key is pressed one of the sense lines will become logic 0. This will generate a start signal which will restart the oscillator.

Key scanning

Six bits of the control timer are used to control the key scanning, subsequently 64 time slots are available. Each time slot corresponds to a key number. The 3 most significant bits (MSBs) control the drive lines and the 3 least significant bits (LSBs) control the sense lines. The scan timing is illustrated in Fig.5. In the first 8 time slots drive line $\overline{DR0}$ is LOW. During this time the 8 sense lines SN0 to SN7 are sequentially tested. The same occurs for the next 8 time slots when $\overline{DR1}$ is at logic 0 and so on until $\overline{DR6}$ is at logic 0. After testing there are 8 time slots when no drive line is at logic 0 (all drive lines HIGH).

When, during time slots 0 to 63, one of the sense lines is at logic 0 the contents of the 6 bits is stored in the key register. This register is used to address the ROM.

No transmission will take place when two or more keys are activated. This situation is considered to be the same as 'no key' and the control bit in the command word for the next transmission will be toggled.

When no key is pressed the oscillator will stop at the end of the control timer (see Section "Timing generator"). In this situation all drive lines will be set to logic 0. When one of the keys is pressed again a wake-up will occur by starting the oscillator.

An option is available to select 'single' or 'multi' system.

Single system

SN0 should be connected to one of the drive lines or ground.

The bank that will be selected is equal to drive line number to which SN0 is connected. When connected to ground the number will be 7. This is achieved by loading the bank select flip-flops BS0 to BS2 with the contents of C5 to C7 of the control timer (see Fig.4) when sense line SN0 is at logic 0. In this way it is possible to use two different systems in one transmitter by using a side switch. With this option SN0 cannot be used to connect keys, so the maximum number of keys will be lower. (49 keys with 20-pin IC and 25 keys with 16-pin IC).

Multi system

The bank is selected by key for maximum 8 different systems (e.g. TV, VCR, CD, etc.), any key is flexible for bank selection. When a user inserts a new battery, the default bank is always in bank 7. If only bank 7 is used, then maximum number of keys can be:

- 56 keys for a 20-pin IC
- 30 keys for 16-pin IC.

ROM

A schematic diagram of the ROM is illustrated in Fig.6. The ROM is divided into 8 banks of 2×64 bytes. Bank selection is performed using flip-flops BS0 to BS2 that are the 3 highest bits of the address. With the 'single system' these bits are loaded from the 3 MSBs of the scan control when SN0 = 0. At power-on the bank select flip-flops will be in an arbitrary state.

When a key was activated, the key number is stored in the 6-bit key register. This register forms the lower bits of the ROM address. For each command the ROM will be accessed twice. This gives 16 bits in total (M0L to M7L and M0H to M7H). The bits are described in Table 3.

Infrared remote control transmitter RC5

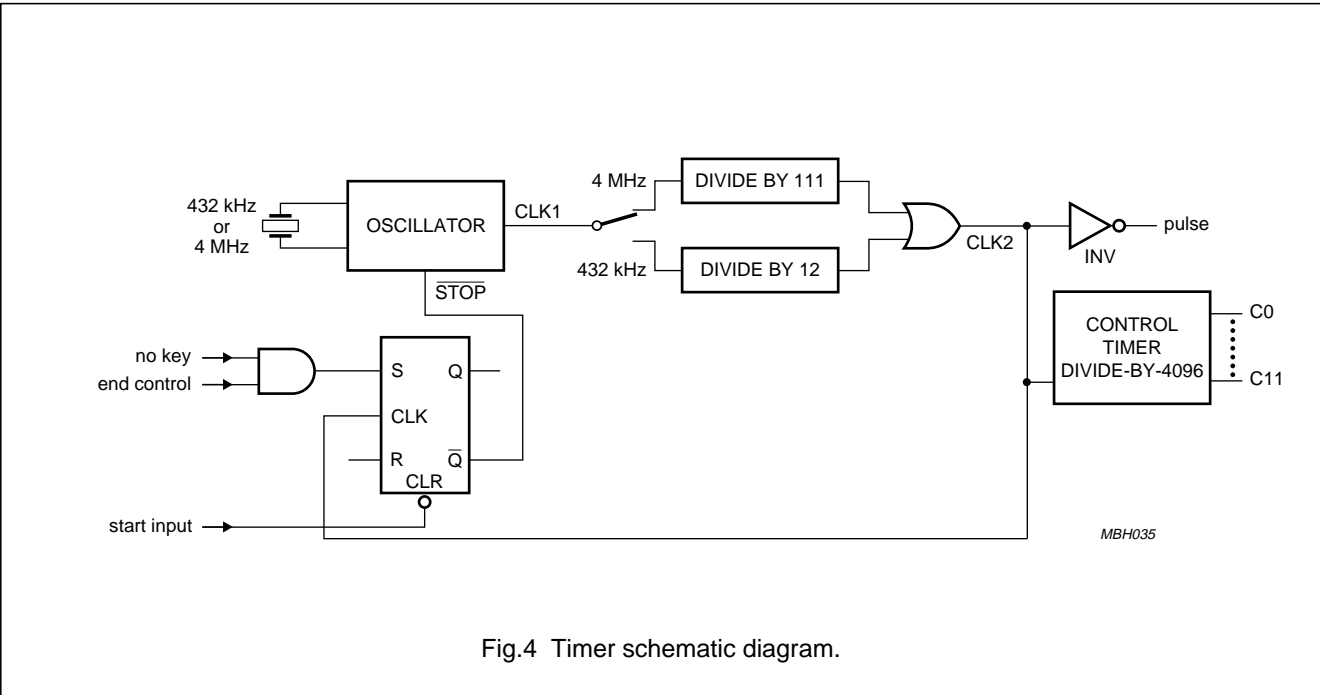
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Table 3 ROM bit description

BITS	FUNCTION
M0L to M5L	Command bits 0 to 5.
M6L	Field bit. This bit indicates whether command codes 0 to 63 are used (field bit is at logic 1) or command codes 64 to 127 are used (field bit is at logic 0).
M7L	Inhibit bit. When this bit is at logic 1 no transmission will take place. When this bit is at logic 0 the appropriate code-word will be transmitted.
M0H to M4H	System bits 0 to 4.
M5H to M7H	Bank select. Will be stored in BS0 to BS2 when the 'multi-system' option is selected. With single system bits M5H to M7H are don't care.

Pulse output

The bits of the remote control word, as indicated by the addressed ROM locations, are loaded into a shift register every bit-time this register is shifted. The output is used to generate a logic 0 or a logic 1 in the biphase (Manchester) coding, modulated with a frequency of 36 kHz. The duty factor of the modulation pulses may be selected (optionally) to be 25% or 33.3%. The output of the pulse generator controls the output driver that can provide a maximum current of 45 mA.



Infrared remote control transmitter RC5

PCA8521

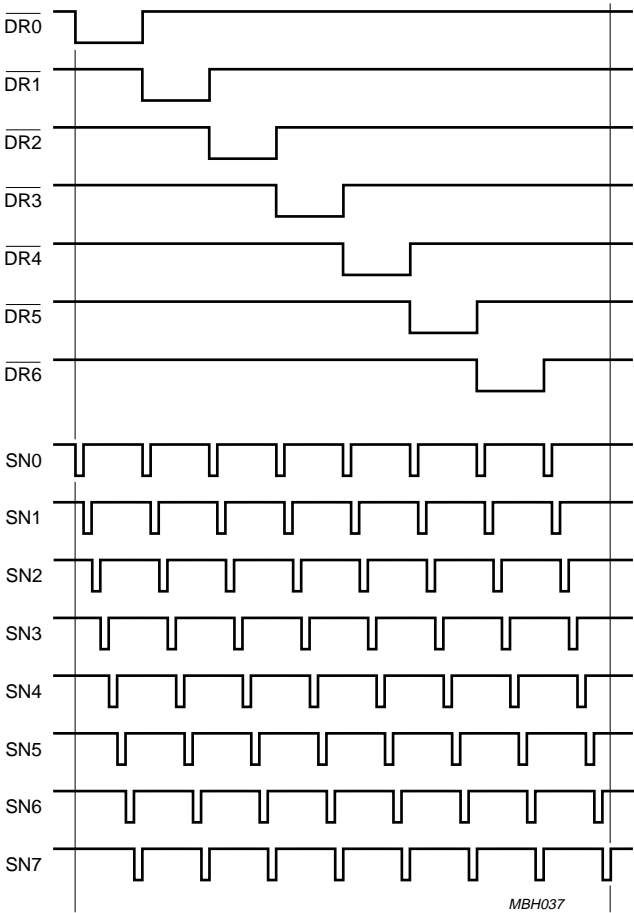


Fig.5 Scan timing.

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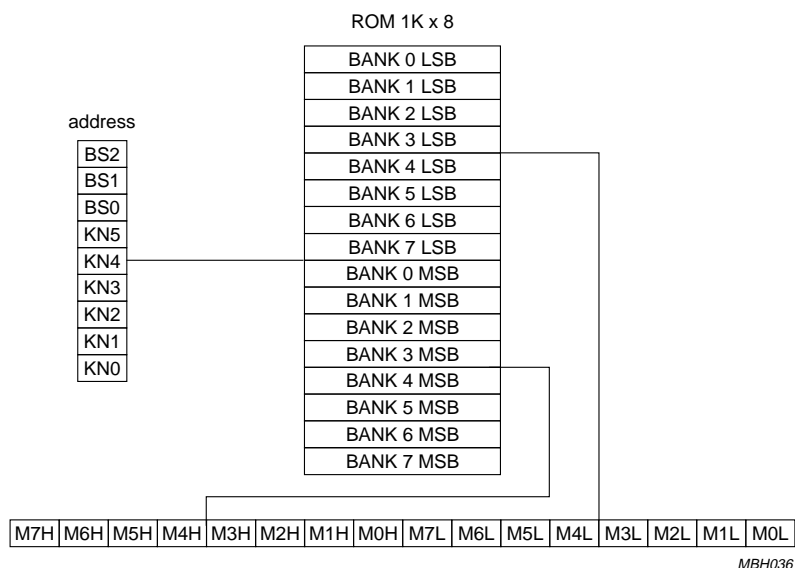


Fig.6 ROM schematic diagram.

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		2.0	–	5.5	V
I_{DD}	supply current	$V_{DD} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$	–	–	2	mA
$I_{DD(q)}$	quiescent current	$V_{DD} = 3\text{ V}$; $T_{amb} = 25\text{ °C}$	–	–	1	μA
T_{amb}	operating ambient temperature		–10	–	+50	°C
Sense lines (input only and will have a weak internal pull-up resistance)						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
R_{pu}	pull-up resistance	$V_{DD} = 2\text{ V}$	50	–	100	kΩ
Driver lines (output only; open drain; maximum on-resistance when LOW)						
R_{on}	maximum on-resistance	$V_{DD} = 2\text{ V}$	–	–	2	kΩ
Output driver (has a weak pull-up resistance)						
I_{sink}	sink current	$V_{DD} = 2\text{ V}$; $V_o = 1\text{ V}$	–	–	45	mA
R_{pu}	pull-up resistance	$V_{DD} = 2\text{ V}$	–	–	5	kΩ

Infrared remote control transmitter RC5

PCA8521

SYSTEM DEVELOPMENT

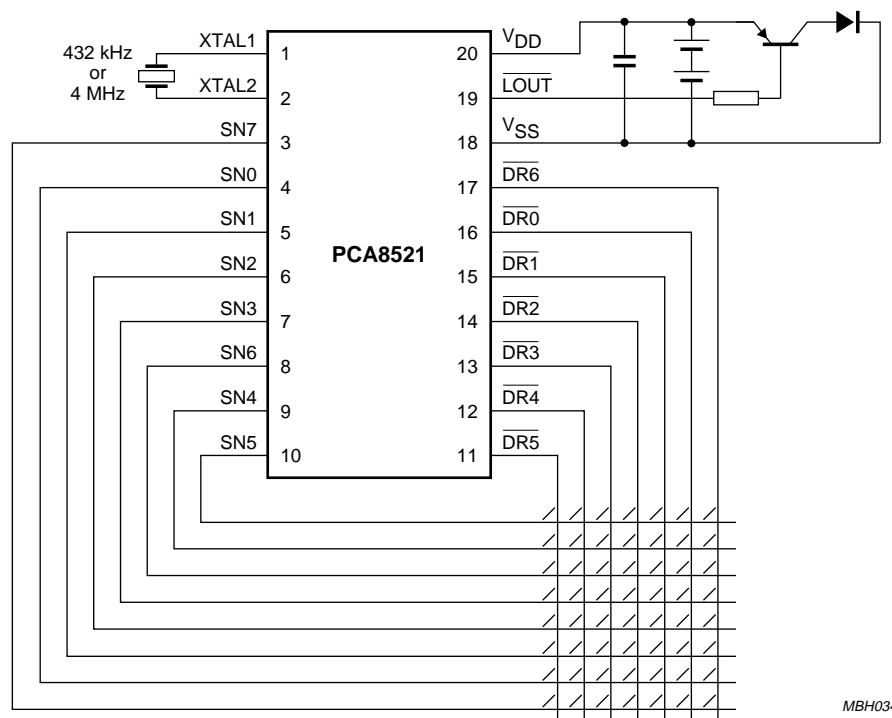
Software (RC8521)

A PC program is provided that enables the user to fill in system and command codes for each key number in each bank. This program converts the input data into a ROM code-file needed to produce the metal mask and to program an EPROM to be used in the hardware emulator.

Hardware (OM4839)

An emulator is available that functionally emulates the IC. An EPROM with the ROM code information is inserted into the emulator to produce the required remote control codes corresponding to the keys in the prototype device.

APPLICATION INFORMATION



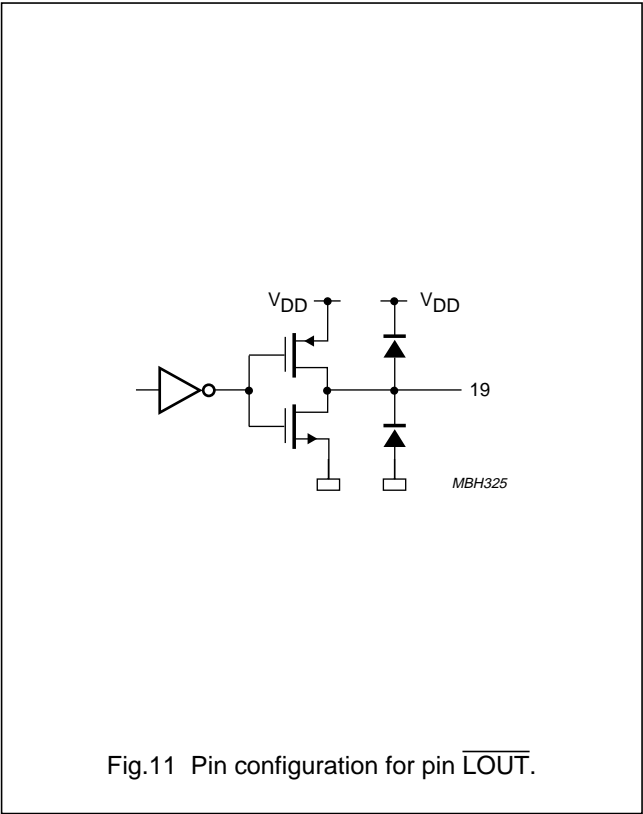
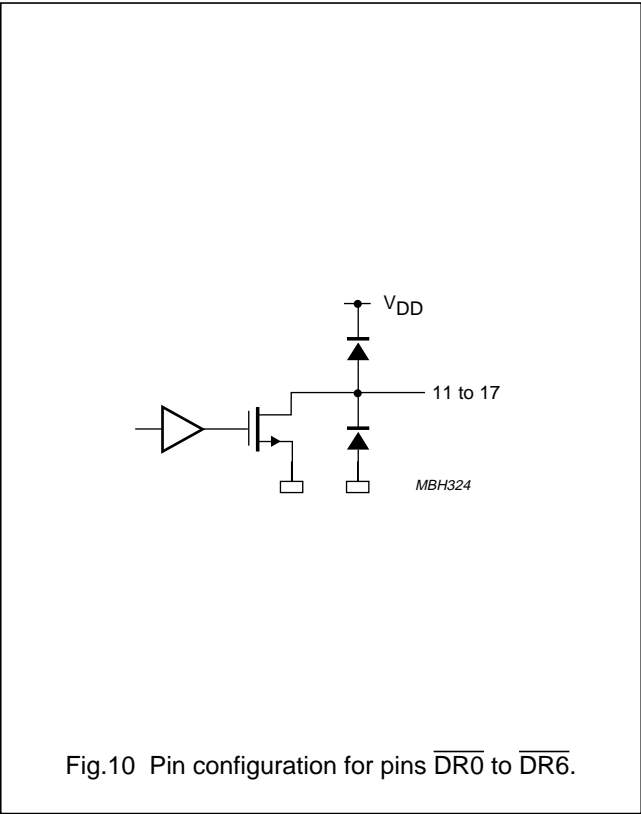
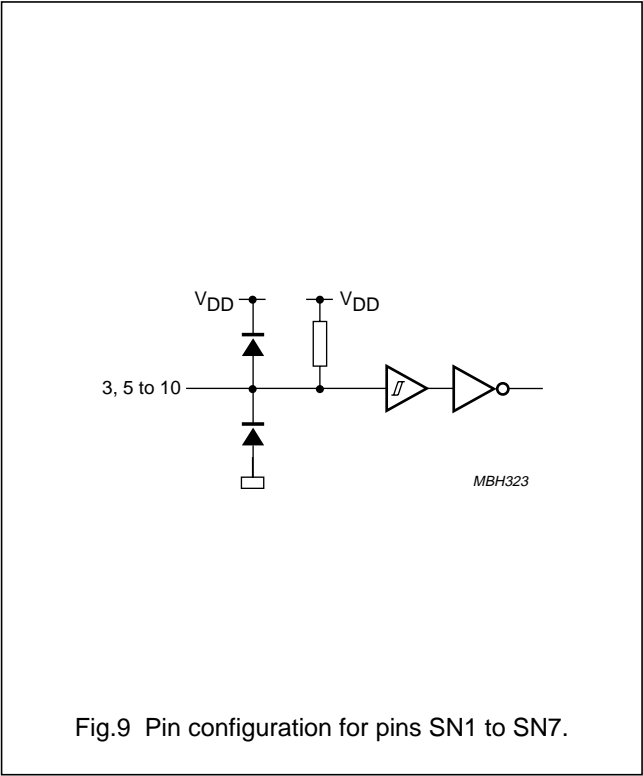
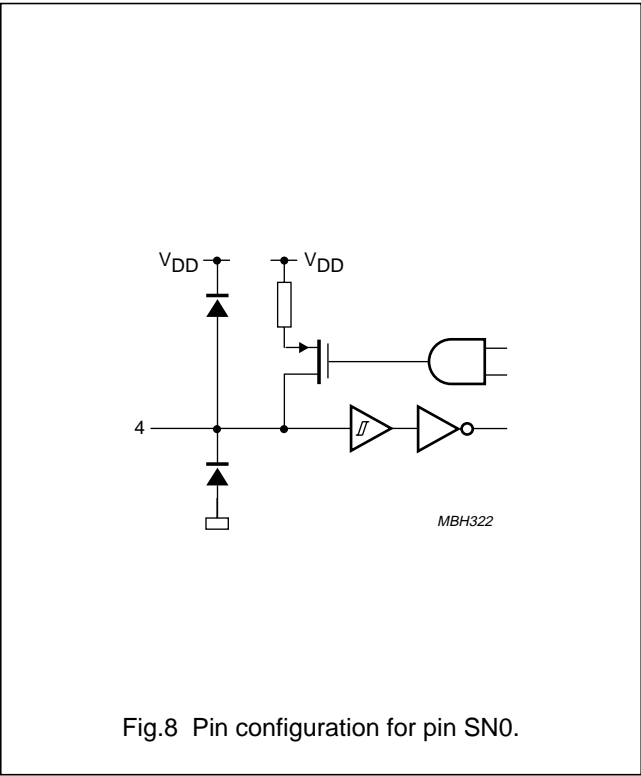
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Fig.7 Application diagram (for DIP20 and SO20 packages).

Infrared remote control transmitter RC5

PCA8521

INTERNAL PIN CONFIGURATION



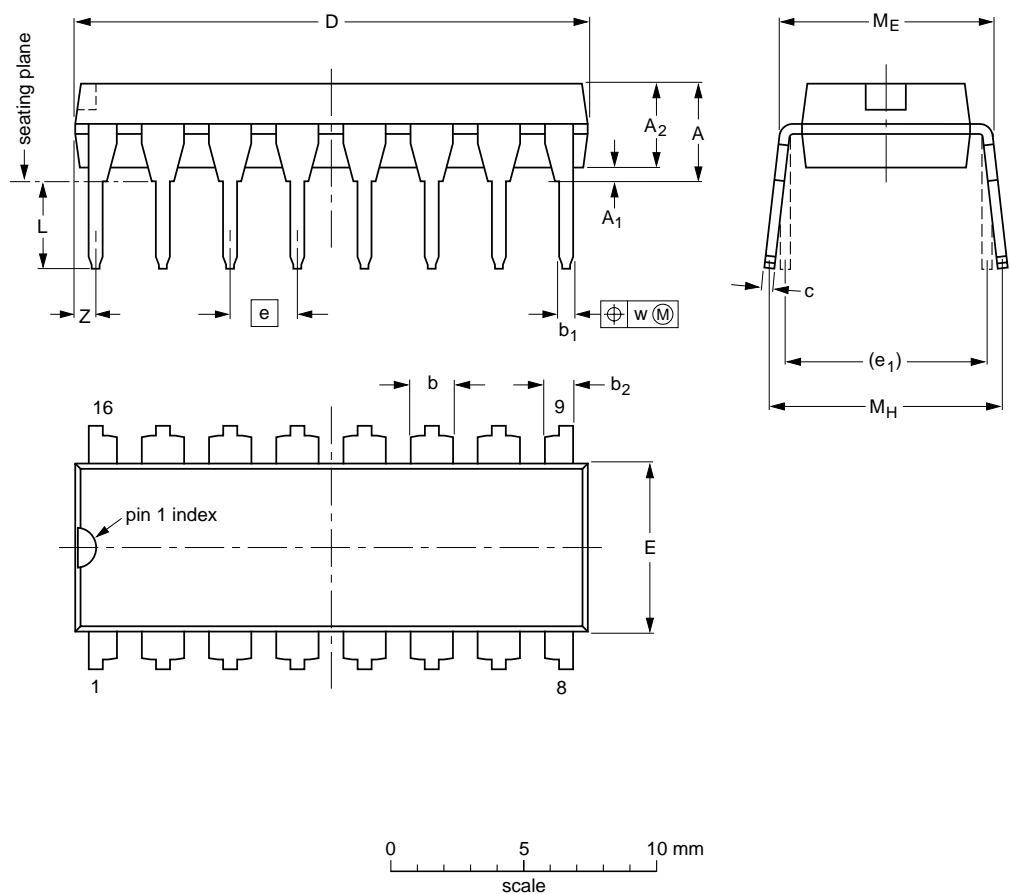
Infrared remote control transmitter RC5

PCA8521

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil)


SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

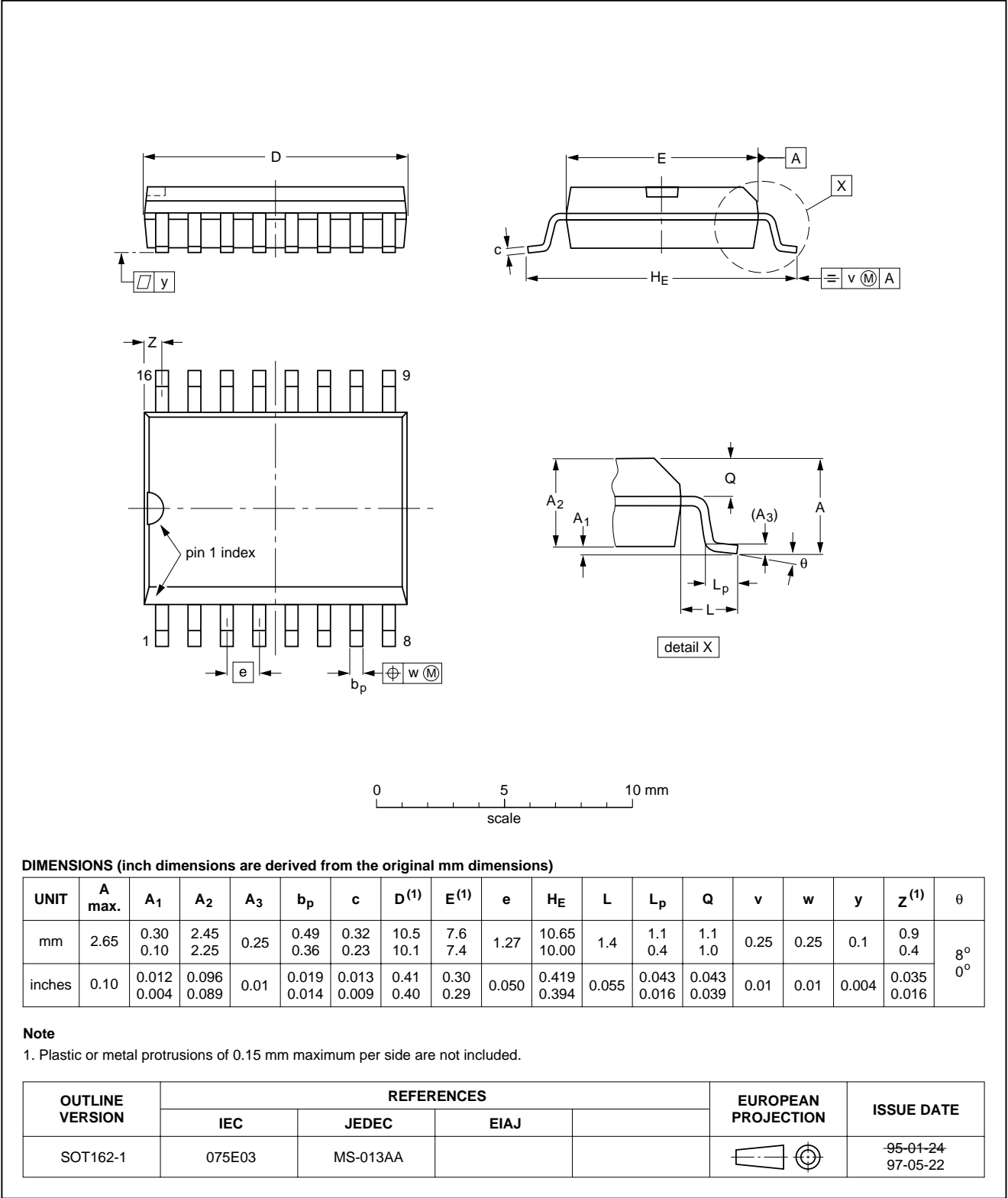
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17- 95-01-14

Infrared remote control transmitter RC5

PCA8521

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

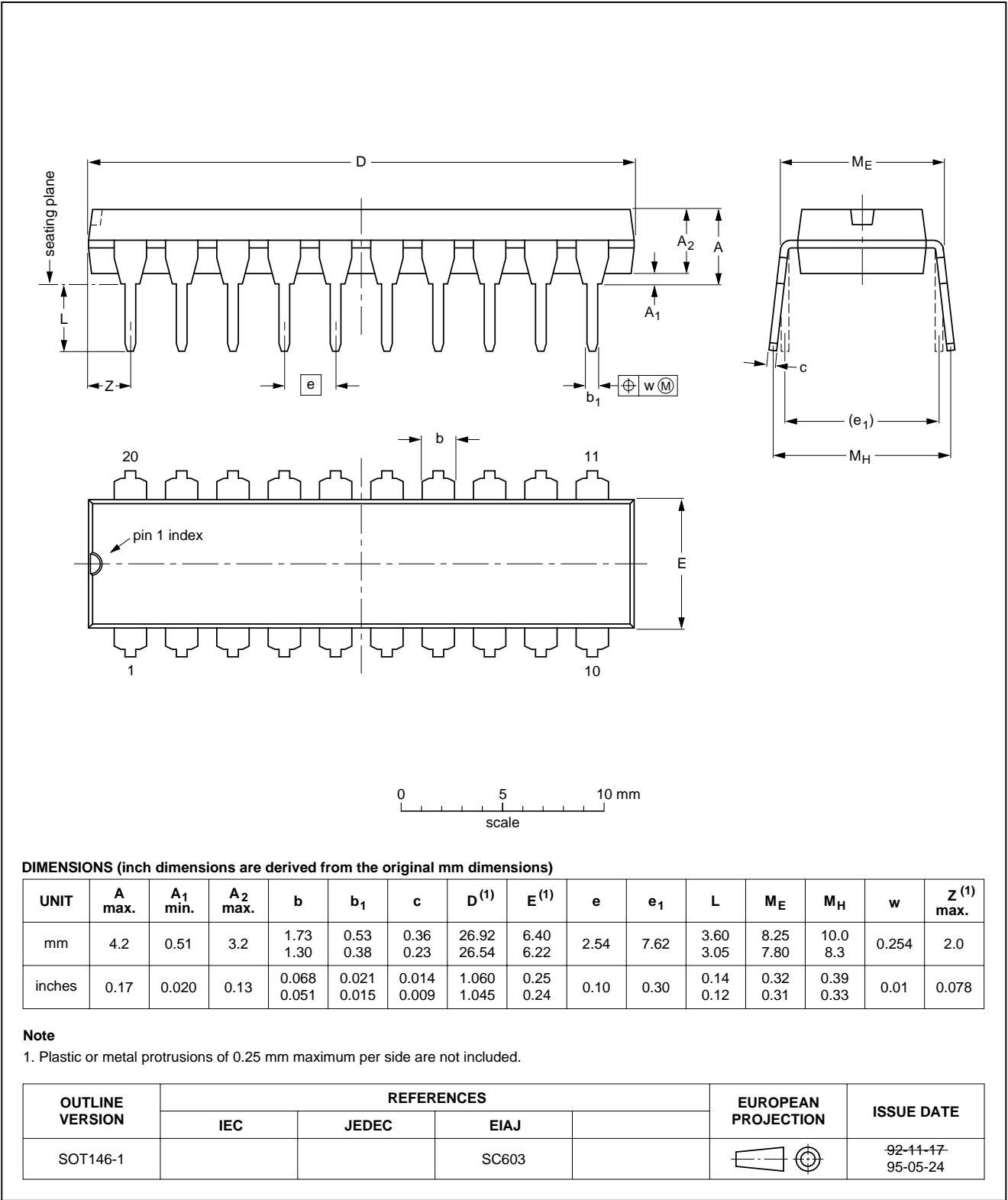


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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

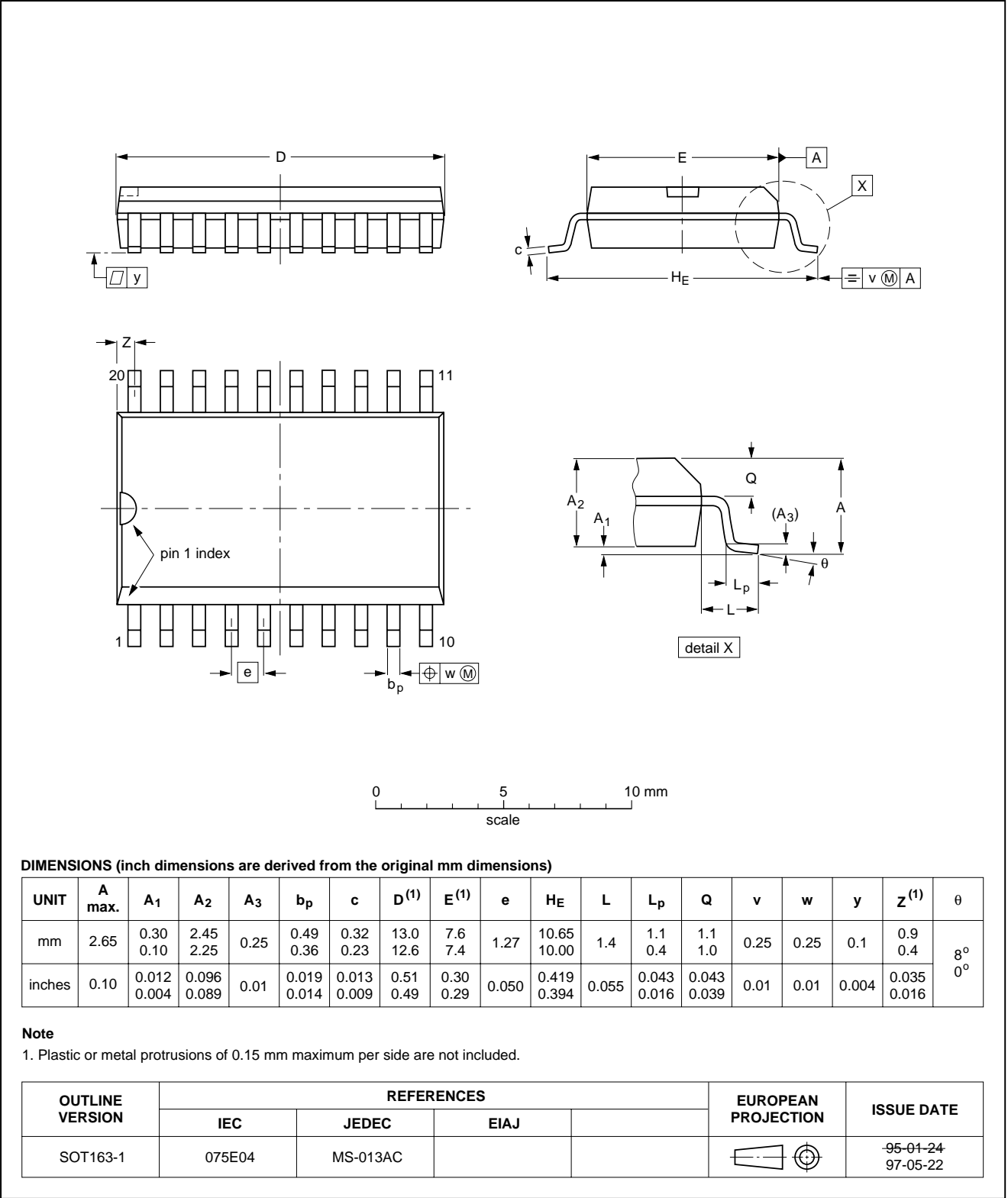


Infrared remote control transmitter RC5

PCA8521

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Infrared remote control transmitter RC5

PCA8521

SOLDERING**Introduction**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages**SOLDERING BY DIPPING OR BY SOLDER WAVE**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages**REFLOW SOLDERING**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Infrared remote control transmitter RC5

PCA8521

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW ⁽¹⁾	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable ⁽²⁾	—	suitable
Surface mount	BGA, SQFP	not suitable	suitable	—
	HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽³⁾	suitable	—
	PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable	—
	LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable	—
	SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable	—

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

Infrared remote control transmitter RC5

PCA8521

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS RC5 COMPONENTS

Purchase of Philips RC5 components conveys a license under the Philips RC5 patent to use the components in RC5 system products conforming to the RC5 standard UATM-5000 for allocation of remote control commands defined by Philips.

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 02 67 52 2531, Fax. +39 02 67 52 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax. +381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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