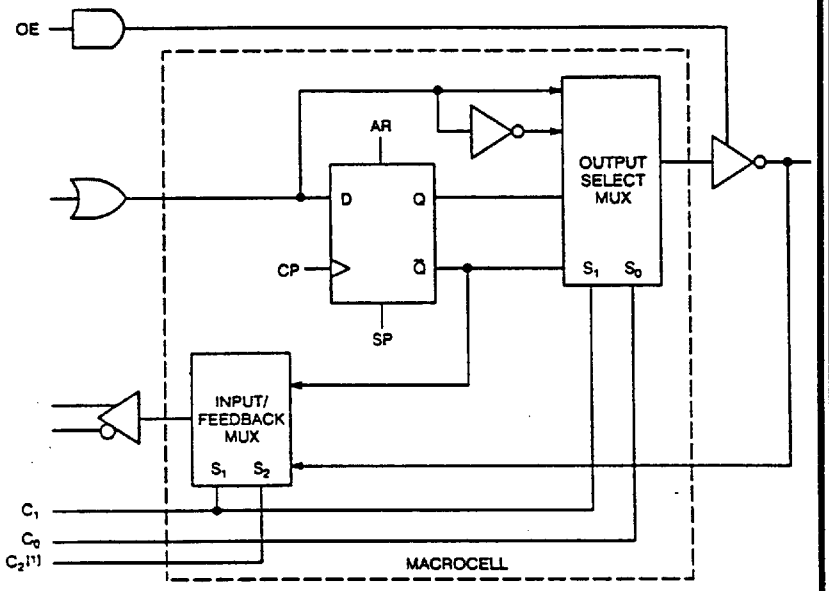
Programmable Logic - Radiation Hardened

22V10RP

Class S Screening High Speed PLD

For Space Applications



SEI's 22V10RP (RP for RAD-PAK®) high speed PLD microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Fully equivalent to the commercial 22V10, the 22V10RP combines BiCMOS technology, Ti-W fuses and SEI's radiation hardened RAD-PAK® packaging. The 22V10RP provides 12 input pins and 10 I/O pins. By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection. It also features a variable product term architecture. Each output is provided with 8 to 16 product terms. This allows more applications to be implemented with this device than with other PLD devices that have fixed number of product terms for each output. This device also features common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions. The 22V10RP automatically resets on power-up. Moreover, the preload capability allows the output registers to be set to any desired state during testing. A security fuse is provided on the device to prevent copying of the device fuse pattern. It is available in Class S packaging and screening.

SPACE ELECTRONICS INCORPORATED

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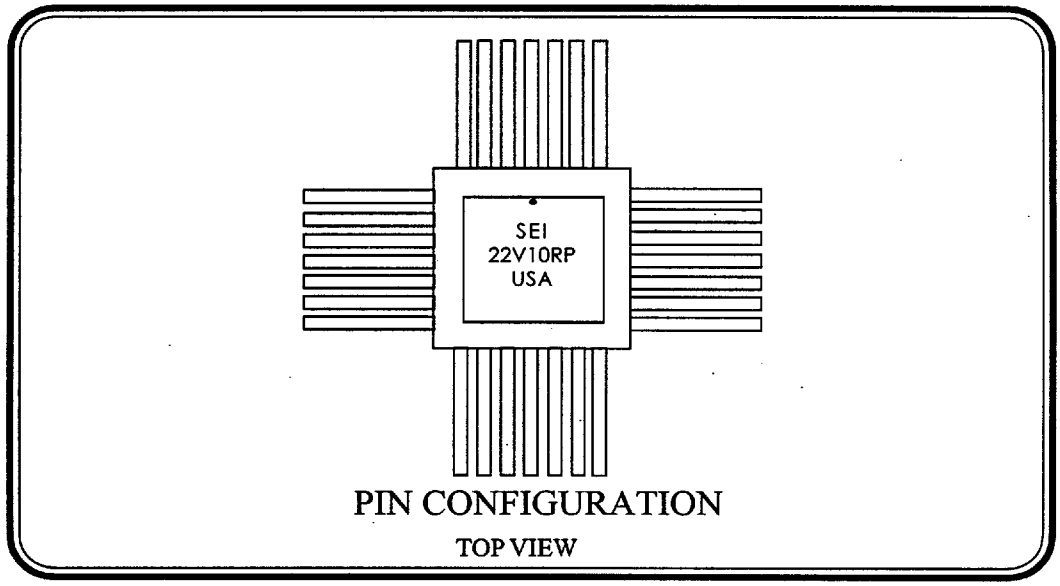
Radiation Hardened
22V10RP Programmable Logic Device



PIN CONFIGURATION

TOP VIEW

Features:

- Second Generation PLD Architecture
- Pin Compatible with 22V10, PAL22V10
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- SEL: None
- SEU: None
- Total Dose Hardness >100 krad (Si)
- Package:
  - 28 Pin RAD-PAK® quad flat pack (1.15 in. x 1.15 in.)
  - Weight – 6.0 grams
  - 24 Pin RAD-PAK® flat pack (0.60 in. x 0.40 in.) Weight - 4.8 grams
  - 24 Pin RAD-PAK® DIP (1.25 in. x 0.40 in.) Weight - 5.0 grams
- Fast Propagation Time: - 15, 20, 25, 30 ns
- Each output user programmable for registered or combinatorial output
- High Speed BiCMOS Technology
  - Up to 22 inputs and 10 outputs
  - Increased product terms, average 12 per output
  - Extra terms provide logical synchronous PRESET and asynchronous RESET capability
- Screening per TM 5004
- QCI per TM5005
- 950 mW max @57MHz

TQM
Total Quality Management

February 1995

For Further Information Contact:

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22V10RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	V_{cc}	-0.5	7.0	V
DC Voltage to Outputs (Except during programming)		-0.5	+V_{cc} max	V
DC Voltage to Outputs (During programming)			16	V
Output Current into Outputs (During programming, 1 sec)			200	mA
DC Input Voltage	V_{IN}	-0.5	5.5	V
DC Input Current	I_{IN}	-30	+5	mA
Power Dissipation	P_d		1200	mW
Storage Temperature Range	T_S	-65	+150	°C
Operating Temperature Range	T_A	-55	+125	°C

22V10RP RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Positive Supply Voltage	V_{dd}	4.75	5.25	V
High Level Input Voltage	V_{IH}	2.0		V
Low Level Input Voltage	V_{IL}		0.8	V

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22V10RP DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage: I_{OL} = 12 mA	V_{OL}		0.5	V
Output High Voltage: I_{OH} = -2 mA	V_{OH}	2.4		V
Input Leakage Current: $V_{SS} \leq V_{IN} \leq 2.7V$, V_{CC}=Max	I_{IL}	-250	50	uA
Maximum Input Current: $V_{IN}=V_{CC}$, V_{CC}=Max	I_I		250	uA
Output Short Circuit Current: V_{OUT} = 0.5V, V_{cc} = Max	I_{OS}	-30	-120	mA
Power Supply Current: V_{cc} = Max	I_{CC}		190	mA
Output High Leakage Current: $V_{SS} \leq V_{OUT} \leq V_{IL}$, V_{cc} = Max	I_{OZH}		100	uA
Output Low Leakage Current: $V_{SS} \leq V_{OUT} \leq V_{CC}$, V_{CC} = Max	I_{OZL}		-100	uA
Input Capacitance[2]	C_{IN}		8	pF
Output Capacitance[2]	C_{OUT}		10	pF

Notes:

1. V_{cc} = 5±5% volts; T_A = -55 to +125 °C.
2. Guaranteed by design, f = 1 MHz.

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22V10RP TIMING CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input to Output Propagation Delay[2]	t_{PD}			
22V10RP-10			10	ns
22V10RP-15			15	
22V10RP-20			20	
22V10RP-25			25	
Input to Output Enable Delay	t_{EA}			
22V10RP-10			10	ns
22V10RP-15			15	
22V10RP-20			20	
22V10RP-25			25	
Input to Output Disable Delay	t_{ER}			
22V10RP-10			10	ns
22V10RP-15			15	
22V10RP-20			20	
22V10RP-25			25	
Clock to Output Delay	t_{CO}			
22V10RP-10			7.5	ns
22V10RP-15			10	
22V10RP-20			12.5	
22V10RP-25			15	
Input to Feedback Setup Time	t_S			
22V10RP-10		3.6		ns
22V10RP-15		7.5		
22V10RP-20		11.0		
22V10RP-25		14.5		
Hold Time	t_H			
22V10RP-10		0		ns
22V10RP-15		0		
22V10RP-20		0		
22V10RP-25		0		
Clock Period ($t_S + t_{CO}$)	t_P			
22V10RP-10		11.1		ns
22V10RP-15		17.5		
22V10RP-20		24.0		
22V10RP-25		30.5		

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PARAMETER	SYMBOL	MIN	MAX	UNITS
Clock Width	t_W			
22V10RP-10		3		ns
22V10RP-15		6		
22V10RP-20		9		
22V10RP-25		12		
Maximum Frequency	f_{MAX}			
22V10RP-10		100		MHz
22V10RP-15		66		
22V10RP-20		43		
22V10RP-25		12		
Asynchronous Reset Width	t_{AW}			
22V10RP-10		10		ns
22V10RP-15		15		
22V10RP-20		20		
22V10RP-25		25		
Asynchronous Reset Recovery Time	t_{AR}			
22V10RP-10		6		ns
22V10RP-15		10		
22V10RP-20		14		
22V10RP-25		20		
Asynchronous Reset to Registered Output Reset	t_{AP}			
22V10RP-10		2	12	ns
22V10RP-15		2	20	
22V10RP-20		2	28	
22V10RP-25		2	36	

Notes:

1. V_{cc} = +5 volts; T_A = +25 °C; use switching test circuit.
2. t_{PD} is tested with switch S_1 closed.
3. For three state outputs, output enable times are tested with C_L = 50 pF to the 1.5 volt level; S is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5 volt with S open; LOW to high impedance tests are made to the V_{OL} + 0.5 volt level with S_1 closed.

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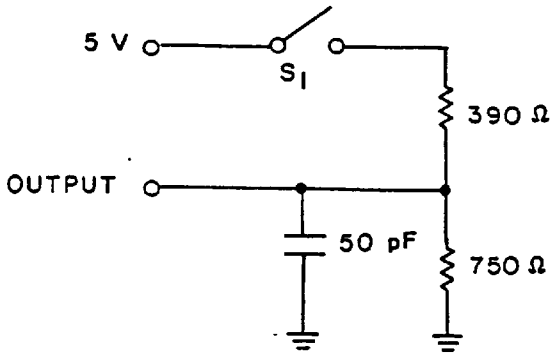

Figure 1. SWITCHING TEST CIRCUIT

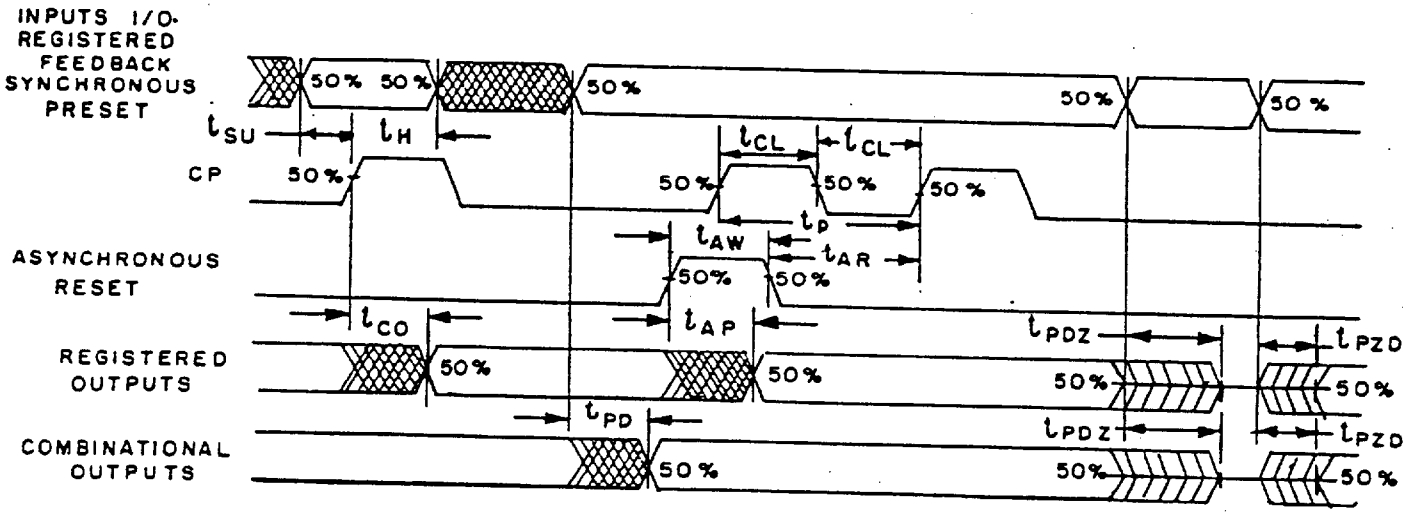

Figure 2. SWITCHING WAVEFORMS

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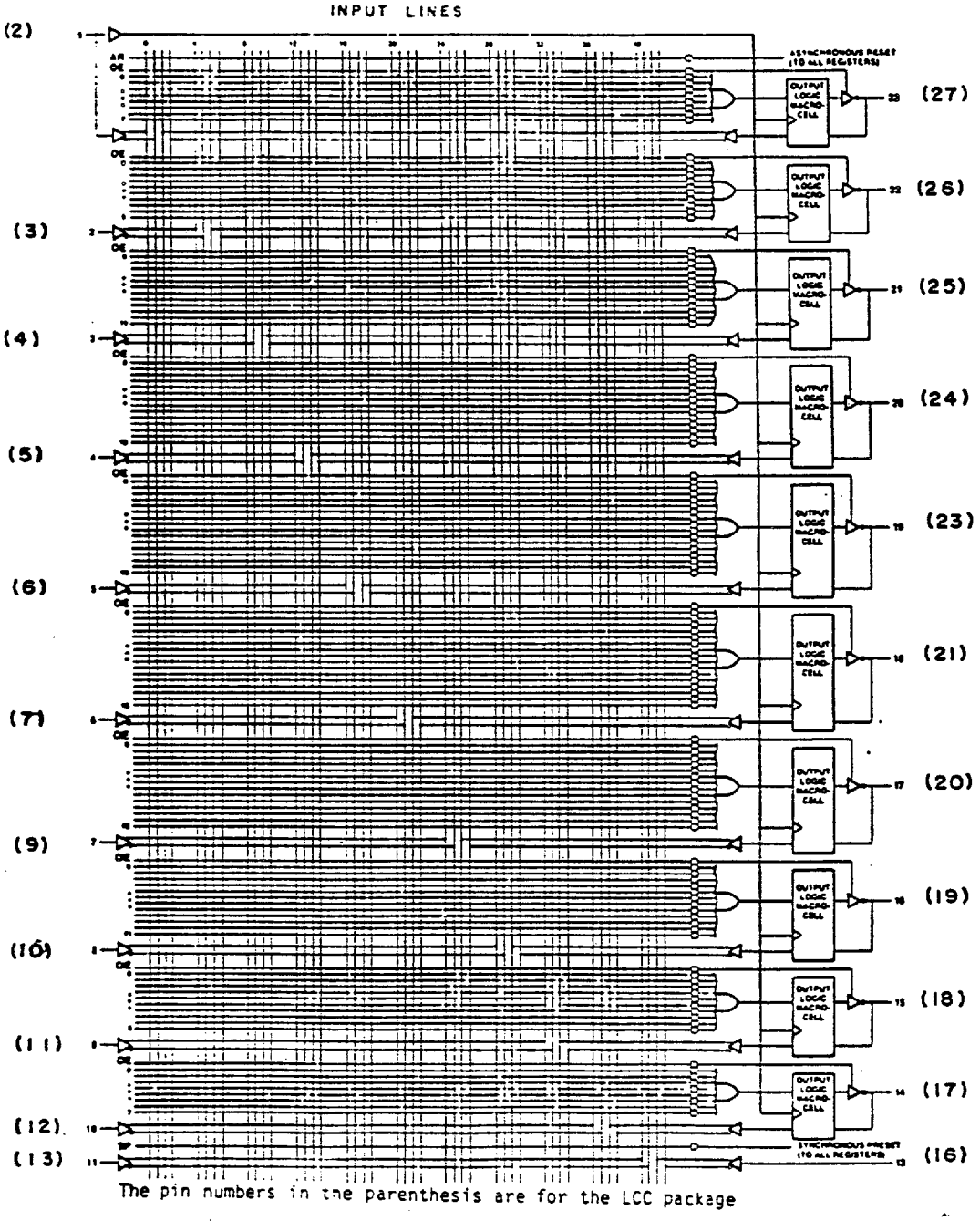

Figure 3. LOGIC DIAGRAM (UNPROGRAMMED)

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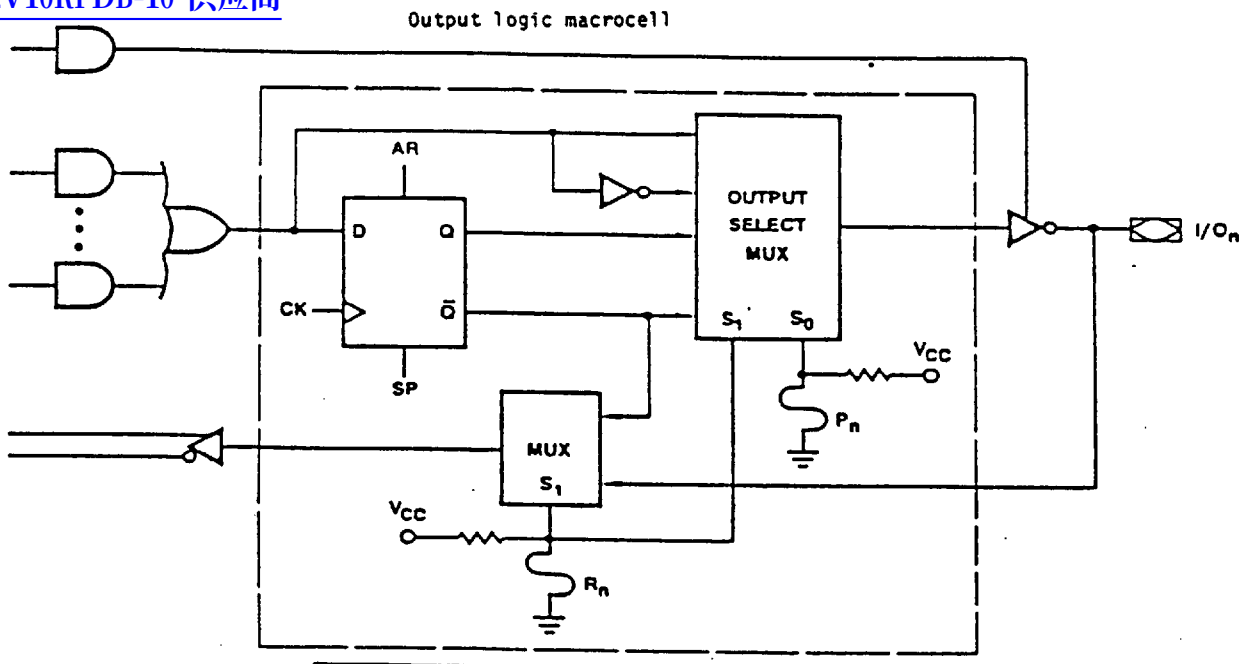

S_1	S_0	Output configuration
0	0	Registered/active low
0	1	Registered/active high
1	0	Combinatorial/active low
1	1	Combinatorial/active high

0 = Unblown fuse
1 = Blown fuse

Figure 3. LOGIC DIAGRAM (UNPROGRAMMED) - Continued

22V10RP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-24	24 Pin Dual In Line Package
F	F-24	24 Pin Flat Package
Q	Q-28	28 Pin Quad Flat Package

Note:
1/ For outline information, see Appendix A (Package Information - Outline Dimension)

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