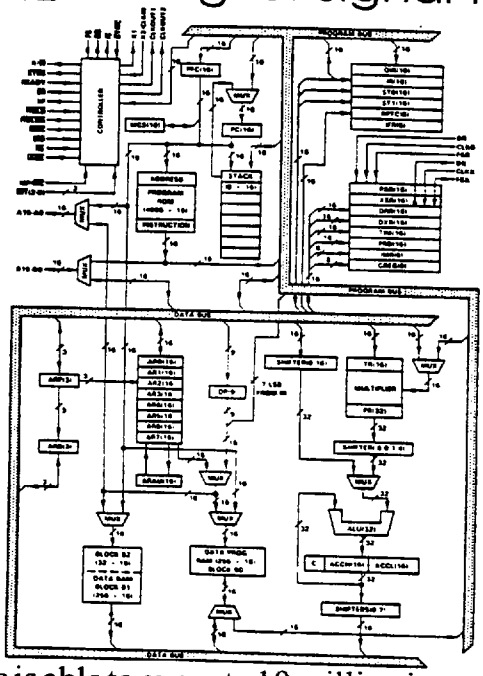
Preliminary

Radiation Hardened 320C25RP

16-Bit Fixed Point CMOS Digital Signal Processor

For Space Applications



SEI's 320C25RP (RP for RAD-PAK®) high speed CMOS microcircuit features a minimum 100 kilorad (Si) total dose tolerance. Fully equivalent to the SMJ320C25, the 320C25RP combines Texas Instruments advanced 16-bit microprocessor and SEI's radiation hardened RAD-PAK® packaging. This device is able to execute 10 million instructions per second, since most of the instructions can be executed in a single cycle. Externally, the program and data memory spaces are multiplexed over the same bus so as to maximize the address range for both spaces and minimize the pin count of the device. Internally, the 320C25RP architecture maximizes processing power by maintaining two separate bus structures, program and data, for full-speed execution. Two large, on-chip data RAM blocks (a total of 544 words), one of which is configurable either as program or data memory, are provided. Four-K words of on-chip program ROM and 64K words of off-chip program address space are also available. From this memory space, large programs are able to be executed at full speed. Programs can also be downloaded from slow external memory to on-chip RAM for full-speed operation. Capable of surviving space environments, the 320C25RP is ideal for satellite, spacecraft, and space probe missions. The RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 320C25RP is available in Class S packaging and screening.

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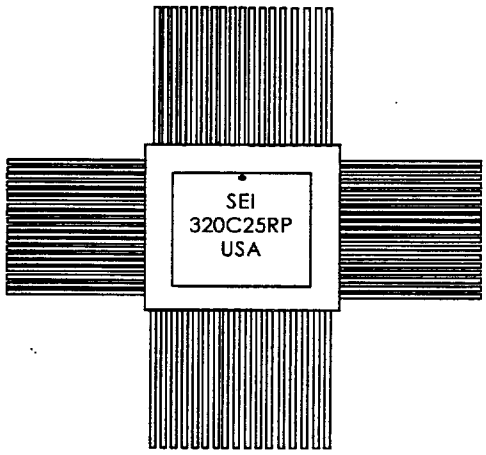
SEI 320C25RP RAD HARD DSP MICROPROCESSOR

Radiation Hardened

320C25RP

16-Bit Fixed Point CMOS
Digital Signal Processor



PIN CONFIGURATION
Top View

Features

- DSP 16-Bit Microprocessor
- Pin Compatible to SMJ320C25
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
  - 68 Pin RAD-PAK® quad flat pack (0.950 in. x 0.950 in.)
- Weight - 12 grams
- High Speed CMOS Technology
- 100 nsec Single-Cycle Instruction Time
- 544 Word RAM
- 4K Word ROM
- 32-bit Accumulator
- Auxiliary Register ALU
- Full Duplex Serial Port
- Multiprocessor Interface
- Screening per TM5004
- QCI per TM5005

TQM
Total Quality Management

May 1994

For Further Information Contact:
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320C25RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage Range	V_{CC}	-0.3	7	V
Input Voltage Range	V_{IN}	-0.3	7	V
Output Voltage Range	V_{OUT}	-0.3	7	V
Continuous Power Dissipation	P_D		1.0	W
Storage Temperature Range	T_S	-55	150	°C

320C25RP RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5.5	V
Supply Voltage	V_{SS}	0	0	V
High-level Input Voltage READY D15-D0, FSX CLKR, CLKX CLKIN All others	V_{IH}	 2.35 2.20 3.50 3.50 3.00		 V V V V V
Low-level Output Current D15-D0, FSX, CLKIN, CLKR, CLKX HOLD All others	V_{IL}		 0.80 0.70 0.70	 V V V
High-level Output Current	I_{OH}		300	uA
Low-level Output Current	I_{OL}		2	mA
Operating Free-air Temperature	T_A	-55		°C
Operating Case Temperature	T_C		125	°C

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320C25RP ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
High-level Output Voltage V_{CC}=MIN, I_{OH}=MAX	V_{OH}	2.4	3		V
Low-level Output Voltage V_{CC}=MIN, I_{OL}=MAX	V_{OL}		0.3	0.6	V
Three-state Current V_{CC}=MAX	I_Z	-20		20	uA
Input Current V_I=V_{SS} to V_{CC}	I_I	-10		10	uA
Supply Current Normal V_{CC}=,f_X=MAX Idle/HOLD\ V_{CC}=,f_X=MAX	I_{CC}			 185 100	 mA mA
Input Capacitance	C_i		15		pF
Output Capacitance	C_o		15		pF

320C25RP SWITCHING REQUIREMENTS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLKOUT1/CLKOUT2 Cycle Time	t_c(C)	100		600	ns
CLKIN High to CLKOUT1/CLKOUT2/STRB\ High/Low	t_d(CIH-C)	5		30	ns
CLKOUT1/CLKOUT2/STRB\ Fall Time	t_f(C)			5	ns
CLKOUT1/CLKOUT2/STRB\ Rise Time	t_r(C)			5	ns
CLKOUT1/CLKOUT2 Low Pulse Duration	t_w(CL)	2Q-8	2Q	2Q+8	
CLKOUT1/CLKOUT2 High Pulse Duration	t_w(CH)	2Q-8	2Q	2Q+8	ns
CLKOUT1 High to CLKOUT2 Low, CLKOUT2 High to CLKOUT1 High, etc.	t_d(C1-C2)	Q-6	Q	Q+6	ns

Note:

1. $Q=1/4t_c(C)$.

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320C25RP TIMING REQUIREMENTS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLKIN Cycle Time	t_c(CI)	25		150	ns
CLKIN Low Pulse Duration, t_c(CI)=25ns[2]	t_w(CIL)	10		15	ns
CLKIN High Pulse Duration, t_c(CI)=25ns[2]	t_w(CIH)	10		15	ns
SYNC\ Setup Time Before CLKIN Low	t_{su}(S)	5		Q-5	ns
SYNC\ Hold Time from CLKIN Low	t_h(S)	8			ns

Notes:

1. Q=1/4t_c(C).
2. CLKIN duty cycle $[t_{r(CI)}+t_{w(CIH)}]/t_{c(CI)}$ must be within 40-60%. CLKIN rise and fall times must be less than 5 ns.

MEMORY AND PERIPHERAL INTERFACE TIMING

320C25RP TIMING REQUIREMENTS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Read Data Access Time from Address Time (Read Cycle[3,5])	t_a(A)			3Q-35	ns
Data Read Setup time before STRB\ High	t_{su}(D)R	23			ns
Data Read Hold time from STRB\ High	t_h(D)R	0			ns
READY Valid after STRB\ Low (No Wait States)	t_s(SL-R)			Q-20	ns
READY Valid after CLKOUT2 High	t_d(C2H-R)			Q-20	ns
READY Hold Time after STRB\ low (No Wait States)	t_h(SL-R)	Q+3			ns
READY Hold after CLKOUT2 High	t_h(C2H-R)	Q+3			ns
READY Hold after MSC\ Valid	t_d(M-R)			2Q-25	ns
READY Hold Time after MSC\ Valid	t_h(M-R)	0			ns

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320C25RP SWITCHING CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
STRB\ From CLKOUT1 (if STRB\ is present)	t_d(C1-S)	Q-6	Q	Q+6	ns
CLKOUT2 To STRB\ (if STRB\ is present)	t_d(C2-S)	-6	0	6	ns
Address Setup Time Before STRB\ Low[3]	t_{su}(A)	Q-12			ns
Address Hold Time After STRB\ High[3]	t_h(A)	Q-8			ns
STRB\ Low Pulse Duration (No Wait States)[4]	t_w(SL)	2Q-5	2Q	2Q+5	ns
STRB\ High Pulse Duration (Between Consecutive Cycles[4])	t_s(SH)		2Q		ns
Data Write Setup Before STRB\ High (No Wait States)	t_{su}(D)W	2Q-20			ns
Data Write Hold Time From STRB\ High	t_h(D)W	Q-10	Q		ns
Data Bus Starts Being Driven After STRB\ Low (Write Cycle)	t_{en}(D)	0			ns
Data Bus Three-state After STRB\ High (Write Cycle)	t_{dis}(D)		Q	Q+15	ns
MSC\ Valid from CLKOUT1	t_d(MSC)	-10	0	10	ns

Notes:

1. Q = 1/4tc(C).
3. A15-A0, PS\, DS\, IS\, R/W\, and BR\ timings are address timings.
4. Delays between CLKOUT1/CLKOUT2 edges and STRB\ edges track each other, resulting in t_w(SL) and t_w(SH) being 2Q with no wait states.
5. Read data access time is defined as t_a(A) = t_{su}(A) + t_w(SL) - t_{su}(D)R + t_r(C).

RS\, INT\, BIO\, AND XF TIMING

320C25RP SWITCHING CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLKOUT1 Low to Reset State Entered	t_d(RS)			22[2]	ns
CLKOUT1 to IACK\ Valid	t_d(IACK)	-8	0	8	ns
XF Valid Before Falling Edge of STRB\	t_d(XF)	Q-12			ns

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320C25RP TIMING REQUIREMENTS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INTVBIOVRS\ Setup before CLKOUT1 High	t_{su}(IN)	32			ns
INTVBIOVRS\ Hold after CLKOUT1 High	t_h(IN)	0			ns
INTVBIO\ Low Pulse Duration	t_w(IN)	t_C(C)			ns
RS\ Low Pulse Duration	t_w(RS)	$3t_C$(C)			ns

Notes:
1. $Q = 1/4t_{c(C)}$.
2. Not tested.

HOLD\ TIMING

320C25RP SWITCHING CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
HOLDA\ Low After CLKOUT1 Low	t_d(C1L-AL)	0		10	ns
HOLDA\ Low to Address Three-state	t_{dis}(AL-A)		0		ns
Address Three-state After CLKOUT1 Low (HOLD\ Mode)[2]	t_{dis}(C1L-A)			20[3]	ns
HOLD\ High to HOLDA\ High	t_d(HH-AH)			25	ns
Address Driven before CLKOUT1 Low (HOLD\ Mode)[2]	t_{en}(A-C1L)			8[3]	ns

320C25RP TIMING REQUIREMENTS[1]

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
HOLD\ Valid After CLKOUT2 High	td(C2H-H)			Q-24	ns

Notes:
1. $Q = 1/4t_{c(C)}$.
2. A15-A0, PS\, DS\, IS\, STRB\, and R/W\ timings are address timings.
3. Not tested.

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SERIAL PORT TIMING

320C25RP SWITCHING CHARACTERISTICS[1]

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
DX Valid After CLKX Rising Edge[2]	t_d(CH-DX)			80	ns
DX Valid After FSX Falling Edge (TXM = 0)[8]	t_d(FL-DX)			45	ns
FSX Valid After CLKX Rising Edge (TXM = 1)	t_d(CH-FS)			45	ns

320C25RP TIMING REQUIREMENTS[1]

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Serial Port Frequency	f_{sx}	1.25		5000	kHz
Serial Port Clock (CLKX/CLKR) Cycle Time	t_c(SCK)	200		800,000	ns
Serial Port Clock (CLKX/CLKR) Low Pulse Duration[3]	t_w(SCK)	80			ns
Serial Port Clock (CLKX/CLKR) High Pulse Duration[3]	t_w(SCK)	80			ns
FSX/FSR Setup Time Before CLKX/CLKR Falling Edge (TXM = 0)	t_{su}(FS)	18			ns
FSX/FSR Hold Time After CLKX/CLKR Falling Edge (TXM = 0)	t_h(FS)	20			ns
DR Setup Time Before CLKR Falling Edge	t_{su}(DR)	10			ns
DR Hold Time After CLKR Falling Edge	t_h(DR)	20			ns

Notes:

1. $Q = 1/4t_{c(C)}$.
2. The last occurrence of FSX falling and CLKX rising.
3. The duty cycle of the serial port clock must be within 40-60%. Serial port clock (CLKX/CLKR) rise and fall times must be less than 25 ns.

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