



93AA46A/B/C, 93LC46A/B/C, 93C46A/B/C
 93AA56A/B/C, 93LC56A/B/C, 93C56A/B/C
 93AA66A/B/C, 93LC66A/B/C, 93C66A/B/C
 93AA76A/B/C, 93LC76A/B/C, 93C76A/B/C
 93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

1K-16K Microwire Compatible Serial EEPROMs

Features:

- Densities from 1 Kbits through 16 Kbits
- Low-power CMOS technology
- Available with or without ORG function:
 - With ORG function:
 - ORG pin at Logic Low: 8-bit word
 - ORG pin at Logic High: 16-bit word
 - Without ORG function:
 - 'A' version: 8-bit word
 - 'B' version: 16-bit word
- Program Enable pin:
 - Write-protect for entire array (93XX76C and 93XX86C only)
- Self-timed Erase/Write cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power-on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device Status signal (Ready/Busy)
- Sequential Read function
- 1,000,000 E/W cycles
- Data retention > 200 years
- Pb-free and RoHS compliant
- Temperature ranges supported:
 - Industrial (I) -40°C to +85°C
 - Automotive (E) -40°C to +125°C

Pin Function Table

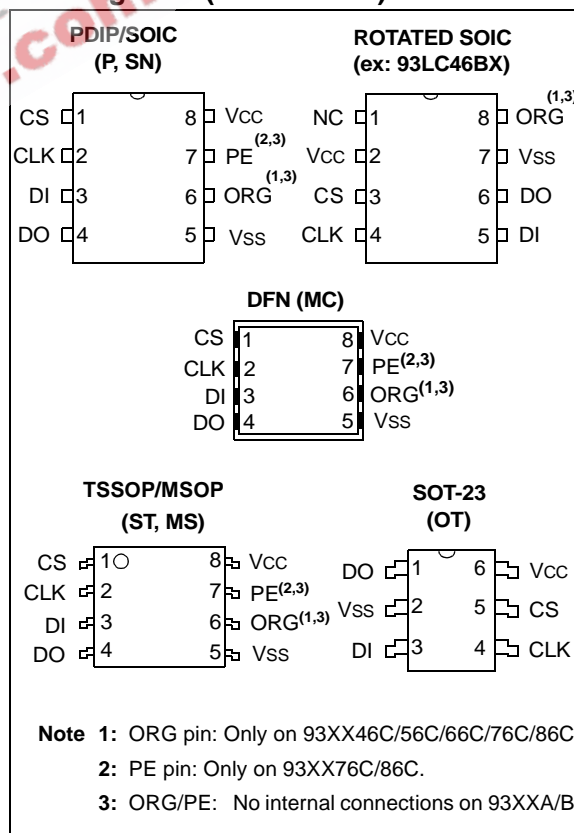
| Name | Function |
|------|----------------------|
| CS | Chip Select |
| CLK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| Vss | Ground |
| PE | Program Enable |
| ORG | Memory Configuration |
| Vcc | Power Supply |

Note: ORG and PE functionality not available in all products. See Table 1-1, Device Selection Table.

Description:

Microchip Technology Inc. supports the 3-wire Microwire bus with low-voltage serial Electrically Erasable PROMs (EEPROM) that range in density from 1 Kbits up to 16 Kbits. Each density is available with and without the ORG functionality, and selected by the part number ordered. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications. The entire series of Microwire devices are available in the standard 8-lead PDIP and SOIC packages, as well as the more advanced packaging such as the 8-lead MSOP, 8-lead TSSOP, 6-lead SOT-23, and 8-lead DFN (2x3). All packages are Pb-free.

Pin Diagrams (not to scale)



93XX46X/56X/66X/76X/86X

TABLE 1-1: DEVICE SELECTION TABLE

| Part Number | Density (Kbits) | Vcc Range | ORG Pin | Organization (Words) | PE Pin | Temp Range | Packages |
|--|-----------------|-----------|---------|----------------------|--------|------------|-----------------------|
| 93XX46A/B/C | | | | | | | |
| 93AA46A | 1 | 1.8-5.5 | No | 128 x 8 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA46B | 1 | 1.8-5.5 | No | 64 x 16 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA46C | 1 | 1.8-5.5 | Yes | Selectable x8 or x16 | No | I | P, SN, ST, MS, MC |
| 93LC46A | 1 | 2.5-5.5 | No | 128 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC46B | 1 | 2.5-5.5 | No | 64 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC46C | 1 | 2.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |
| 93C46A | 1 | 4.5-5.5 | No | 128 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C46B | 1 | 4.5-5.5 | No | 64 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C46C | 1 | 4.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |
| 93AA46AX/BX/CX, 93LC46AX/BX/CX, 93C46AX/BX/CX (Alternate pinout with die rotated 90°) | | | | | | | |
| 93AA46AX | 1 | 1.8-5.5 | No | 128 x 8 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA46BX | 1 | 1.8-5.5 | No | 64 x 16 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA46CX | 1 | 1.8-5.5 | Yes | Selectable x8 or x16 | No | I | P, SN, ST, MS, MC |
| 93LC46AX | 1 | 2.5-5.5 | No | 128 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC46BX | 1 | 2.5-5.5 | No | 64 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC46CX | 1 | 2.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |
| 93C46AX | 1 | 4.5-5.5 | No | 128 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C46BX | 1 | 4.5-5.5 | No | 64 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C46CX | 1 | 4.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |
| 93XX56A/B/C | | | | | | | |
| 93AA56A | 2 | 1.8-5.5 | No | 256 x 8 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA56B | 2 | 1.8-5.5 | No | 128 x 16 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA56C | 2 | 1.8-5.5 | Yes | Selectable x8 or x16 | No | I | P, SN, ST, MS, MC |
| 93LC56A | 2 | 2.5-5.5 | No | 256 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC56B | 2 | 2.5-5.5 | No | 128 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC56C | 2 | 2.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |
| 93C56A | 2 | 4.5-5.5 | No | 256 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C56B | 2 | 4.5-5.5 | No | 128 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C56C | 2 | 4.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |
| 93XX66A/B/C | | | | | | | |
| 93AA66A | 4 | 1.8-5.5 | No | 512 x 8 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA66B | 4 | 1.8-5.5 | No | 256 x 16 bits | No | I | P, SN, ST, MS, OT, MC |
| 93AA66C | 4 | 1.8-5.5 | Yes | Selectable x8 or x16 | No | I | P, SN, ST, MS, MC |
| 93LC66A | 4 | 2.5-5.5 | No | 512 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC66B | 4 | 2.5-5.5 | No | 256 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93LC66C | 4 | 2.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |
| 93C66A | 4 | 4.5-5.5 | No | 512 x 8 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C66B | 4 | 4.5-5.5 | No | 256 x 16 bits | No | I, E | P, SN, ST, MS, OT, MC |
| 93C66C | 4 | 4.5-5.5 | Yes | Selectable x8 or x16 | No | I, E | P, SN, ST, MS, MC |

93XX46X/56X/66X/76X/86X

TABLE 1-1: DEVICE SELECTION TABLE (CONTINUED)

| Part Number | Density (Kbits) | Vcc Range | ORG Pin | Organization (Words) | PE Pin | Temp Range | Packages |
|--------------------|-----------------|-----------|---------|----------------------|--------|------------|-------------------|
| 93XX76A/B/C | | | | | | | |
| 93AA76A | 8 | 1.8-5.5 | No | 1024 x 8 bits | No | I | OT |
| 93AA76B | 8 | 1.8-5.5 | No | 512 x 16 bits | No | I | OT |
| 93AA76C | 8 | 1.8-5.5 | Yes | Selectable x8 or x16 | Yes | I | P, SN, ST, MS, MC |
| 93LC76A | 8 | 2.5-5.5 | No | 1024 x 8 bits | No | I, E | OT |
| 93LC76B | 8 | 2.5-5.5 | No | 512 x 16 bits | No | I, E | OT |
| 93LC76C | 8 | 2.5-5.5 | Yes | Selectable x8 or x16 | Yes | I, E | P, SN, ST, MS, MC |
| 93C76A | 8 | 4.5-5.5 | No | 1024 x 8 bits | No | I, E | OT |
| 93C76B | 8 | 4.5-5.5 | No | 512 x 16 bits | No | I, E | OT |
| 93C76C | 8 | 4.5-5.5 | Yes | Selectable x8 or x16 | Yes | I, E | P, SN, ST, MS, MC |
| 93XX86A/B/C | | | | | | | |
| 93AA86A | 16 | 1.8-5.5 | No | 2048 x 8 bits | No | I | OT |
| 93AA86B | 16 | 1.8-5.5 | No | 1024 x 16 bits | No | I | OT |
| 93AA86C | 16 | 1.8-5.5 | Yes | Selectable x8 or x16 | Yes | I | P, SN, ST, MS, MC |
| 93LC86A | 16 | 2.5-5.5 | No | 2048 x 8 bits | No | I, E | OT |
| 93LC86B | 16 | 2.5-5.5 | No | 1024 x 16 bits | No | I, E | OT |
| 93LC86C | 16 | 2.5-5.5 | Yes | Selectable x8 or x16 | Yes | I, E | P, SN, ST, MS, MC |
| 93C86A | 16 | 4.5-5.5 | No | 2048 x 8 bits | No | I, E | OT |
| 93C86B | 16 | 4.5-5.5 | No | 1024 x 16 bits | No | I, E | OT |
| 93C86C | 16 | 4.5-5.5 | Yes | Selectable x8 or x16 | Yes | I, E | P, SN, ST, MS, MC |

93XX46X/56X/66X/76X/86X

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

| | |
|---|--------------------------------|
| V _{CC} | 7.0V |
| All inputs and outputs w.r.t. V _{SS} | -0.6V to V _{CC} +1.0V |
| Storage temperature | -65°C to +150°C |
| Ambient temperature with power applied..... | -40°C to +125°C |
| ESD protection on all pins | ≥ 4 kV |

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: DC CHARACTERISTICS

| All parameters apply over the specified ranges unless otherwise noted. | | | V _{CC} = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C | | | | |
|--|---------------------------------------|---|---|------|---------------------|-------|---|
| Param. No. | Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
| D1 | V _{IH1} | High-level input voltage | 2.0 | — | V _{CC} +1 | V | V _{CC} ≥ 2.7V |
| | V _{IH2} | | 0.7 V _{CC} | — | V _{CC} +1 | V | V _{CC} < 2.7V |
| D2 | V _{IL1} | Low-level input voltage | -0.3 | — | 0.8 | V | V _{CC} ≥ 2.7V |
| | V _{IL2} | | -0.3 | — | 0.2 V _{CC} | V | V _{CC} < 2.7V |
| D3 | V _{OL1} | Low-level output voltage | — | — | 0.4 | V | I _{OL} = 2.1 mA, V _{CC} = 4.5V |
| | V _{OL2} | | — | — | 0.2 | V | I _{OL} = 100 μA, V _{CC} = 2.5V |
| D4 | V _{OH1} | High-level output voltage | 2.4 | — | — | V | I _{OH} = -400 μA, V _{CC} = 4.5V |
| | V _{OH2} | | V _{CC} -0.2 | — | — | V | I _{OH} = -100 μA, V _{CC} = 2.5V |
| D5 | I _{LI} | Input leakage current | — | — | ±1 | μA | V _{IN} = V _{SS} to V _{CC} |
| D6 | I _{LO} | Output leakage current | — | — | ±1 | μA | V _{OUT} = V _{SS} to V _{CC} |
| D7 | C _{IN} , C _{OUT} | Pin capacitance (all inputs/outputs) | — | — | 7 | pF | V _{IN} /V _{OUT} = 0V (Note 1) TA = 25°C, F _{CLK} = 1 MHz |
| D8 | I _{CC} write | Write current | — | — | 2 | mA | F _{CLK} = 3 MHz, V _{CC} = 5.5V (93XX46X/56X/66X) |
| | | | — | — | 3 | mA | F _{CLK} = 3 MHz, V _{CC} = 5.5V (93XX76X/86X) |
| | | | — | 500 | — | μA | F _{CLK} = 2 MHz, V _{CC} = 2.5V |
| D9 | I _{CC} read | Read current | — | — | 1 | mA | F _{CLK} = 3 MHz, V _{CC} = 5.5V |
| | | | — | — | 500 | μA | F _{CLK} = 2 MHz, V _{CC} = 3.0V |
| | | | — | 100 | — | μA | F _{CLK} = 2 MHz, V _{CC} = 2.5V |
| D10 | I _{CCS} | Standby current | — | — | 1 | μA | I-Temp (Note 2, 3) |
| | | | — | — | 5 | μA | E-Temp CLK = Cs = 0V ORG = DI = V _{SS} or V _{CC} |
| D11 | V _{POR} | V _{CC} voltage detect | — | 1.5V | — | V | 93AAX6A/B/C, 93LCX6A/B/C, |
| | | | — | 3.8V | — | V | 93CX6A/B/C (Note 1) |

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG and PE pins not available on 'A' or 'B' versions.

3: Ready/Busy status must be cleared from DO, see **Section 4.4 "Data Out (DO)"**.

93XX46X/56X/66X/76X/86X

TABLE 2-2: AC CHARACTERISTICS

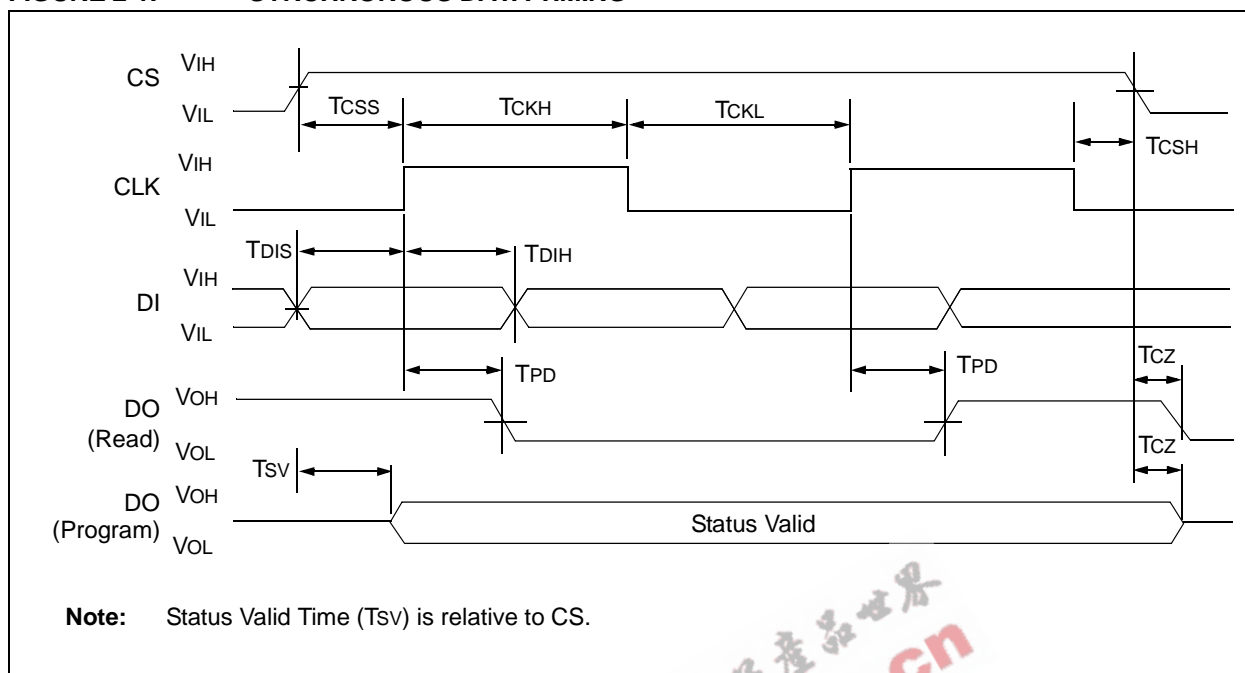
| All parameters apply over the specified ranges unless otherwise noted. | | | VCC = 1.8V to 5.5V Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C | | | |
|--|--------|--------------------------|---|-------------------|-------------------|--|
| Param. No. | Symbol | Parameter | Min. | Max. | Units | Conditions |
| A1 | FCLK | Clock frequency | — | 3 2 1 | MHz MHz MHz | 4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V |
| A2 | TCKH | Clock high time | 200 250 450 | — | ns ns ns | 4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V |
| A3 | TCKL | Clock low time | 100 200 450 | — | ns ns ns | 4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V |
| A4 | TCSS | Chip Select setup time | 50 100 250 | — | ns ns ns | 4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V |
| A5 | TCSH | Chip Select hold time | 0 | — | ns | 1.8V ≤ VCC < 5.5V |
| A6 | TCSL | Chip Select low time | 250 | — | ns | 1.8V ≤ VCC < 5.5V |
| A7 | TDIS | Data input setup time | 50 100 250 | — | ns ns ns | 4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V |
| A8 | TDIH | Data input hold time | 50 100 250 | — | ns ns ns | 4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V |
| A9 | TPD | Data output delay time | — | 100 | ns | 4.5V ≤ VCC < 5.5V, CL = 100 pF (93C76X/86X) |
| | | | — | 200 | ns | 4.5V ≤ VCC < 5.5V, CL = 100 pF |
| | | | — | 250 | ns | 2.5V ≤ VCC < 4.5V, CL = 100 pF |
| | | | — | 400 | ns | 1.8V ≤ VCC < 2.5V, CL = 100 pF |
| A10 | TCZ | Data output disable time | — | 100 200 | ns ns | 4.5V ≤ VCC < 5.5V, (Note 1) 1.8V ≤ VCC < 4.5V, (Note 1) |
| A11 | Tsv | Status valid time | — | 200 300 500 | ns ns ns | 4.5V ≤ VCC < 5.5V, CL = 100 pF 2.5V ≤ VCC < 4.5V, CL = 100 pF 1.8V ≤ VCC < 2.5V, CL = 100 pF |
| A12 | TWC | Program cycle time | — | 5 | ms | Erase/Write mode 93XX76X/86X (AA and LC versions) |
| | | | — | 6 | ms | 93XX46X/56X/66X (AA and LC versions) |
| A13 | TWC | | — | 2 | ms | 93C46X/56X/66X/76X/86X |
| A14 | TEC | Program cycle time | — | 6 | ms | ERAL mode, 4.5V ≤ VCC ≤ 5.5V |
| A15 | TWL | | — | 15 | ms | WRAL mode, 4.5V ≤ VCC ≤ 5.5V |
| A16 | — | Endurance | 1M | — | cycles | 25°C, VCC = 5.0V, (Note 2) |

Note 1: This parameter is periodically sampled and not 100% tested.

2: This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which may be downloaded from Microchip's web site at www.microchip.com.

93XX46X/56X/66X/76X/86X

FIGURE 2-1: SYNCHRONOUS DATA TIMING



93XX46X/56X/66X/76X/86X

TABLE 2-3: INSTRUCTION SET FOR 93XX46A/B/C

| Instruction | SB | Opcode | Address | | | | | | | | Data In | Data Out | Req. CLK Cycles |
|--|----|--------|---------|----|----|----|----|----|----|--------|-----------|-----------|-----------------|
| 93XX46B OR 93XX46C WITH ORG = 1 (16-BIT WORD ORGANIZATION) | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 9 | |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | — | (RDY/BSY) | 9 | |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | — | High-Z | 9 | |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | — | High-Z | 9 | |
| READ | 1 | 10 | | A5 | A4 | A3 | A2 | A1 | A0 | — | D15-D0 | 25 | |
| WRITE | 1 | 01 | | A5 | A4 | A3 | A2 | A1 | A0 | D15-D0 | (RDY/BSY) | 25 | |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | D15-D0 | (RDY/BSY) | 25 | |
| 93XX46A OR 93XX46C WITH ORG = 0 (8-BIT WORD ORGANIZATION) | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 10 |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | x | — | (RDY/BSY) | 10 |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | x | — | High-Z | 10 |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | x | — | High-Z | 10 |
| READ | 1 | 10 | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D7-D0 | 18 |
| WRITE | 1 | 01 | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7-D0 | (RDY/BSY) | 18 |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | x | D7-D0 | (RDY/BSY) | 18 |

TABLE 2-4: INSTRUCTION SET FOR 93XX56A/B/C

| Instruction | SB | Opcode | Address | | | | | | | | | Data In | Data Out | Req. CLK Cycles | |
|--|----|--------|---------|---|----|----|----|----|----|----|----|---------|-----------|-----------------|----|
| 93XX56B OR 93XX56C WITH ORG = 1 (16-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | x | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 11 | |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | x | x | — | (RDY/BSY) | 11 | |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | x | x | — | High-Z | 11 | |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | x | x | — | High-Z | 11 | |
| READ | 1 | 10 | | x | A6 | A5 | A4 | A3 | S2 | A1 | A0 | — | D15-D0 | 27 | |
| WRITE | 1 | 01 | | x | A6 | A5 | A4 | A3 | S2 | A1 | A0 | D15-D0 | (RDY/BSY) | 27 | |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | x | x | D15-D0 | (RDY/BSY) | 27 | |
| 93XX56A OR 93XX56C WITH ORG = 0 (8-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | x | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 12 |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | x | x | x | — | (RDY/BSY) | 12 |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | x | x | x | — | High-Z | 12 |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | x | x | x | — | High-Z | 12 |
| READ | 1 | 10 | | x | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D7-D0 | 20 |
| WRITE | 1 | 01 | | x | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7-D0 | (RDY/BSY) | 20 |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | x | x | x | D7-D0 | (RDY/BSY) | 20 |

93XX46X/56X/66X/76X/86X

TABLE 2-5: INSTRUCTION SET FOR 93XX66A/B/C

| Instruction | SB | Opcode | Address | | | | | | | | | Data In | Data Out | Req. CLK Cycles | |
|--|----|--------|---------|----|----|----|----|----|----|----|----|---------|-----------|-----------------|----|
| 93XX66B OR 93XX66C WITH ORG = 1 (16-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 11 | |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | x | x | — | (RDY/BSY) | 11 | |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | x | x | — | High-Z | 11 | |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | x | x | — | High-Z | 11 | |
| READ | 1 | 10 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D15-D0 | 27 | |
| WRITE | 1 | 01 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15-D0 | (RDY/BSY) | 27 | |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | x | x | D15-D0 | (RDY/BSY) | 27 | |
| 93XX66A OR 93XX66C WITH ORG = 0 (8-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 12 |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | x | x | x | — | (RDY/BSY) | 12 |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | x | x | x | — | High-Z | 12 |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | x | x | x | — | High-Z | 12 |
| READ | 1 | 10 | | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D7-D0 | 20 |
| WRITE | 1 | 01 | | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7-D0 | (RDY/BSY) | 20 |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | x | x | x | D7-D0 | (RDY/BSY) | 20 |

TABLE 2-6: INSTRUCTION SET FOR 93XX76A/B/C

| Instruction | SB | Opcode | Address | | | | | | | | | | | Data In | Data Out | Req. CLK Cycles |
|--|----|--------|---------|----|----|----|----|----|----|----|----|----|----|---------|-----------|-----------------|
| 93XX76B OR 93XX76C WITH ORG = 1 (16-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | x | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 13 |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | x | x | x | x | — | (RDY/BSY) | 13 |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | x | x | x | x | — | High-Z | 13 |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | x | x | x | x | — | High-Z | 13 |
| READ | 1 | 10 | | x | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D15-D0 | 29 |
| WRITE | 1 | 01 | | x | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15-D0 | (RDY/BSY) | 29 |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | x | x | x | x | D15-D0 | (RDY/BSY) | 29 |
| 93XX76A OR 93XX76C WITH ORG = 0 (8-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | x | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 14 |
| ERAL | 1 | 00 | 1 | 0 | x | x | x | x | x | x | x | x | x | — | (RDY/BSY) | 14 |
| EWDS | 1 | 00 | 0 | 0 | x | x | x | x | x | x | x | x | x | — | High-Z | 14 |
| EWEN | 1 | 00 | 1 | 1 | x | x | x | x | x | x | x | x | x | — | High-Z | 14 |
| READ | 1 | 10 | x | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D7-D0 | 22 |
| WRITE | 1 | 01 | x | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7-D0 | (RDY/BSY) | 22 |
| WRAL | 1 | 00 | 0 | 1 | x | x | x | x | x | x | x | x | x | D7-D0 | (RDY/BSY) | 22 |

93XX46X/56X/66X/76X/86X

TABLE 2-7: INSTRUCTION SET FOR 93XX86A/B/C

| Instruction | SB | Opcode | Address | | | | | | | | | | | Data In | Data Out | Req. CLK Cycles |
|--|----|--------|---------|----|----|----|----|----|----|----|----|----|----|---------|-----------|-----------------|
| 93XX86B OR 93XX86C WITH ORG = 1 (16-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 13 |
| ERAL | 1 | 00 | | 1 | 0 | x | x | x | x | x | x | x | x | — | (RDY/BSY) | 13 |
| EWDS | 1 | 00 | | 0 | 0 | x | x | x | x | x | x | x | x | — | High-Z | 13 |
| EWEN | 1 | 00 | | 1 | 1 | x | x | x | x | x | x | x | x | — | High-Z | 13 |
| READ | 1 | 10 | | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D15-D0 | 29 |
| WRITE | 1 | 01 | | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D15-D0 | (RDY/BSY) | 29 |
| WRAL | 1 | 00 | | 0 | 1 | x | x | x | x | x | x | x | x | D15-D0 | (RDY/BSY) | 29 |
| 93XX86A OR 93XX86C WITH ORG = 0 (8-BIT WORD ORGANIZATION) | | | | | | | | | | | | | | | | |
| ERASE | 1 | 11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | (RDY/BSY) | 14 |
| ERAL | 1 | 00 | 1 | 0 | x | x | x | x | x | x | x | x | x | — | (RDY/BSY) | 14 |
| EWDS | 1 | 00 | 0 | 0 | x | x | x | x | x | x | x | x | x | — | High-Z | 14 |
| EWEN | 1 | 00 | 1 | 1 | x | x | x | x | x | x | x | x | x | — | High-Z | 14 |
| READ | 1 | 10 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | — | D7-D0 | 22 |
| WRITE | 1 | 01 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7-D0 | (RDY/BSY) | 22 |
| WRAL | 1 | 00 | 0 | 1 | x | x | x | x | x | x | x | x | x | D7-D0 | (RDY/BSY) | 22 |

93XX46X/56X/66X/76X/86X

3.0 FUNCTIONAL DESCRIPTION

When the ORG pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

3.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note: When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active high.

3.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of the driver, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

3.3 Data Protection

All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for '93AAXX' and '93LCXX' devices or 3.8V for '93CXX' devices.

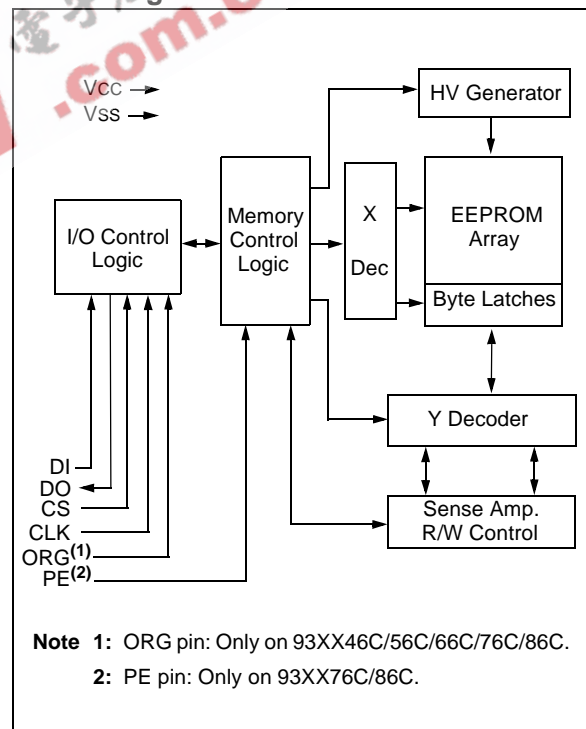
The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note: For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Note: To prevent accidental writes to the array in the 93XX76C/86C devices, set the PE pin to a logic low.

Block Diagram



93XX46X/56X/66X/76X/86X

3.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on '93CXX' devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note: After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 3-1: ERASE TIMING FOR 93AAXX AND 93LCXX DEVICES

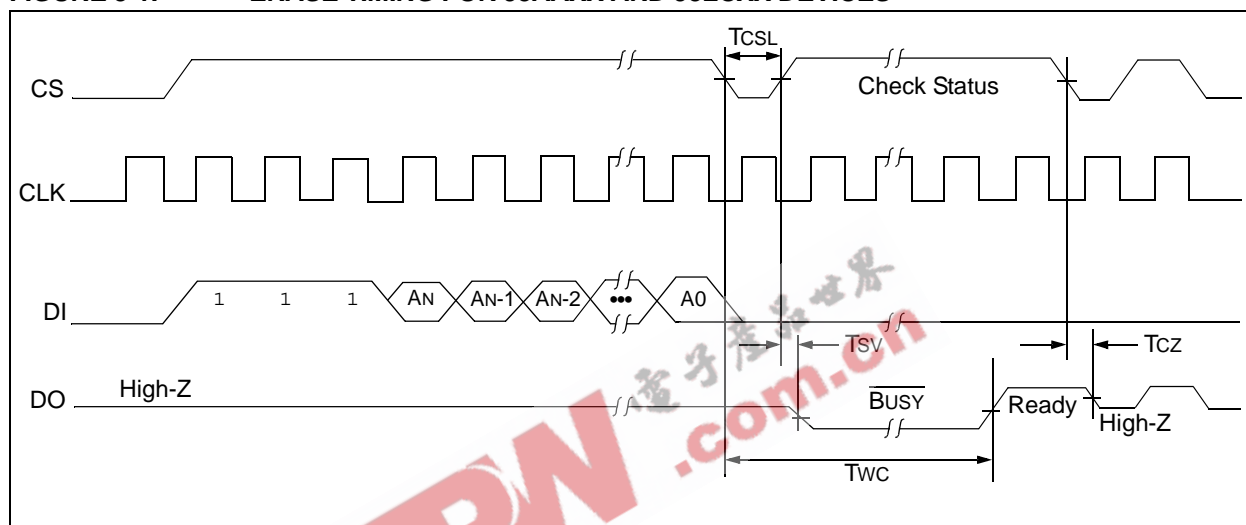
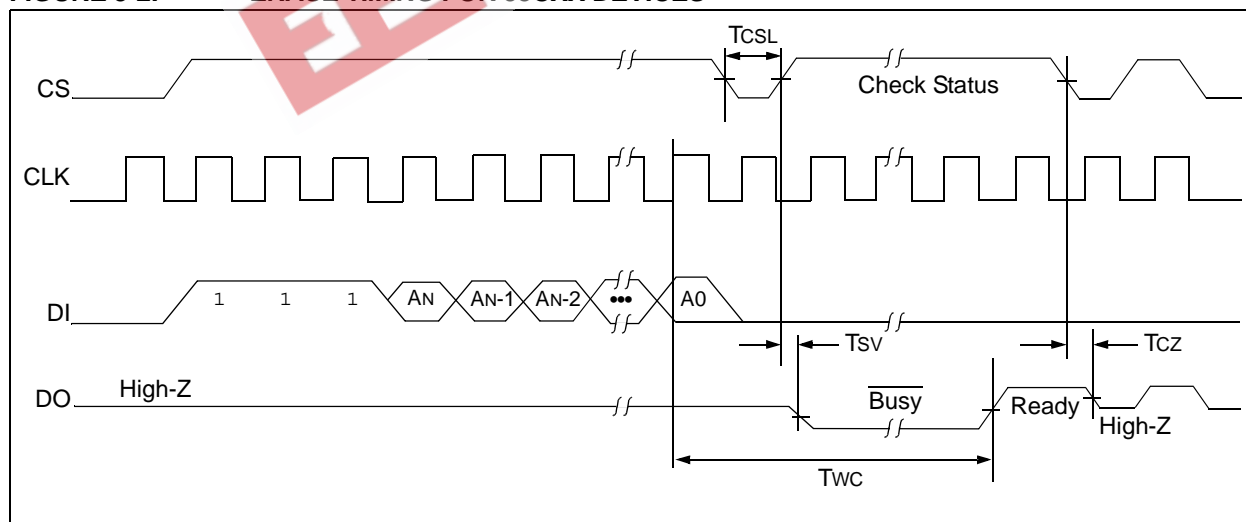


FIGURE 3-2: ERASE TIMING FOR 93CXX DEVICES



93XX46X/56X/66X/76X/86X

3.5 ERASE ALL (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the Erase cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on '93CXX' devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/Busy status of the device, if CS is brought high after a minimum of 250 ns low (TCSL).

VCC must be $\geq 4.5V$ for proper operation of ERAL.

Note: After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 3-3: ERAL TIMING FOR 93AAXX AND 93LCXX DEVICES

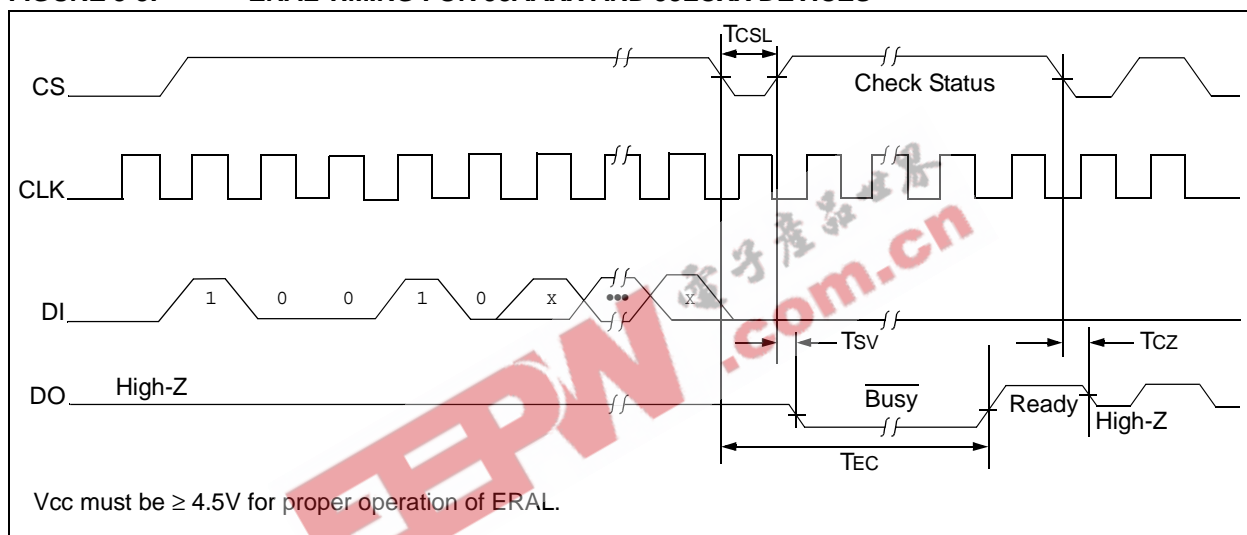
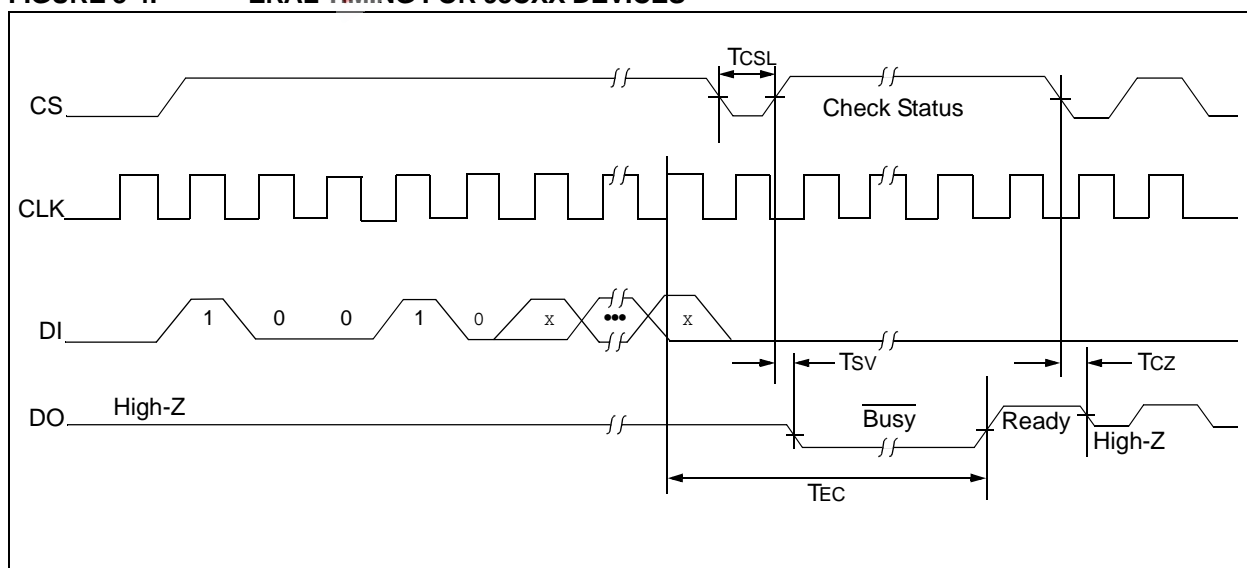


FIGURE 3-4: ERAL TIMING FOR 93CXX DEVICES



3.6 ERASE/WRITE DISABLE And ENABLE (EWDS/EWEN)

The 93XX series devices power-up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all Erase/Write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 3-5: EWDS TIMING

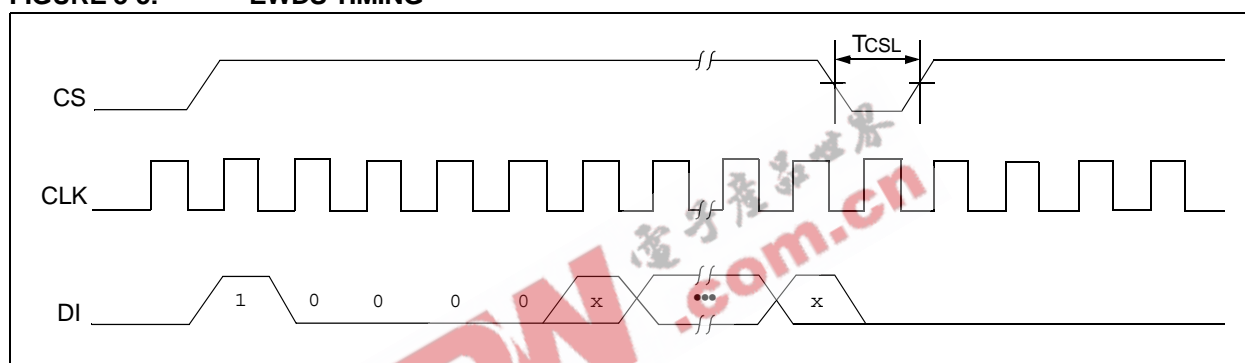
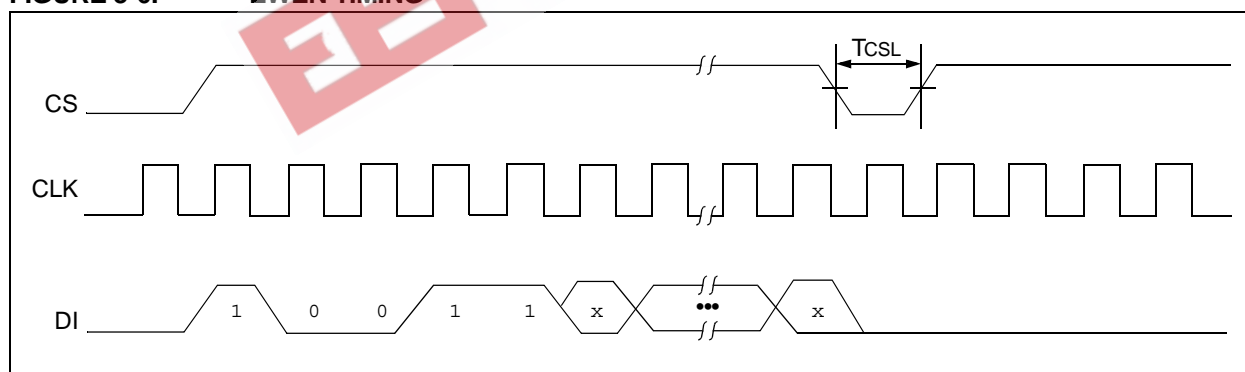


FIGURE 3-6: EWEN TIMING

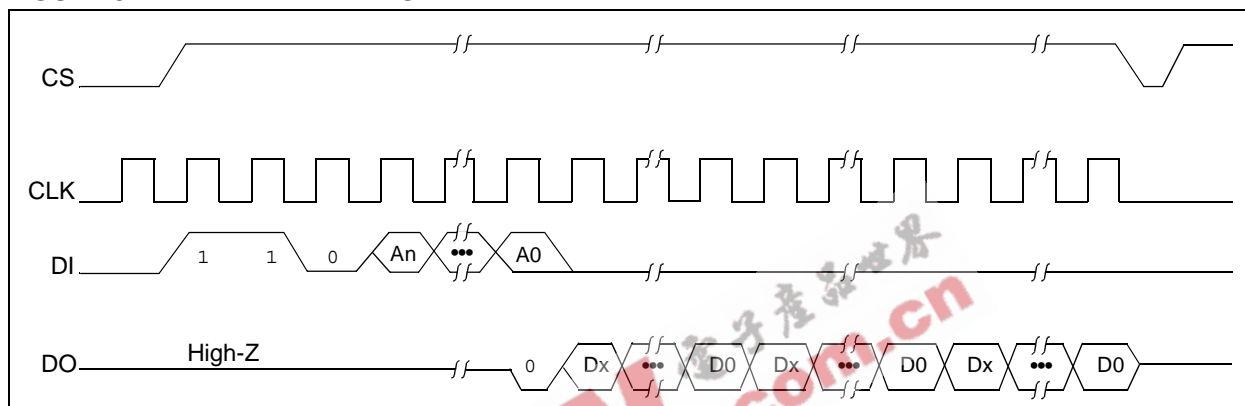


93XX46X/56X/66X/76X/86X

3.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-version devices) or 16-bit (If ORG pin is high or B-version devices) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 3-7: READ TIMING



93XX46X/56X/66X/76X/86X

3.8 WRITE

The **WRITE** instruction is followed by 8 bits (If ORG is low or A-version devices) or 16 bits (If ORG pin is high or B-version devices) of data which are written into the specified address. For 93AAXX and 93LCXX devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93CXX devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/Busy status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note: For devices with PE functionality such as the 93XX76C or 93XX86C, the write sequence requires a logic high signal on the PE pin prior to the rising edge of clock on the last data bit.

Note: After the Write cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 3-8: WRITE TIMING FOR 93AAXX AND 93LCXX DEVICES

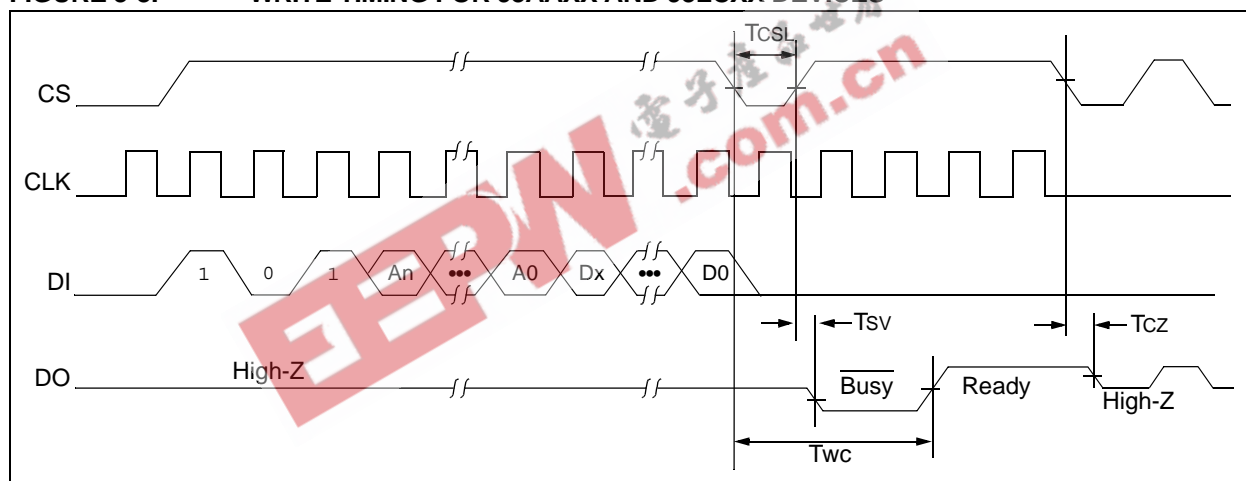
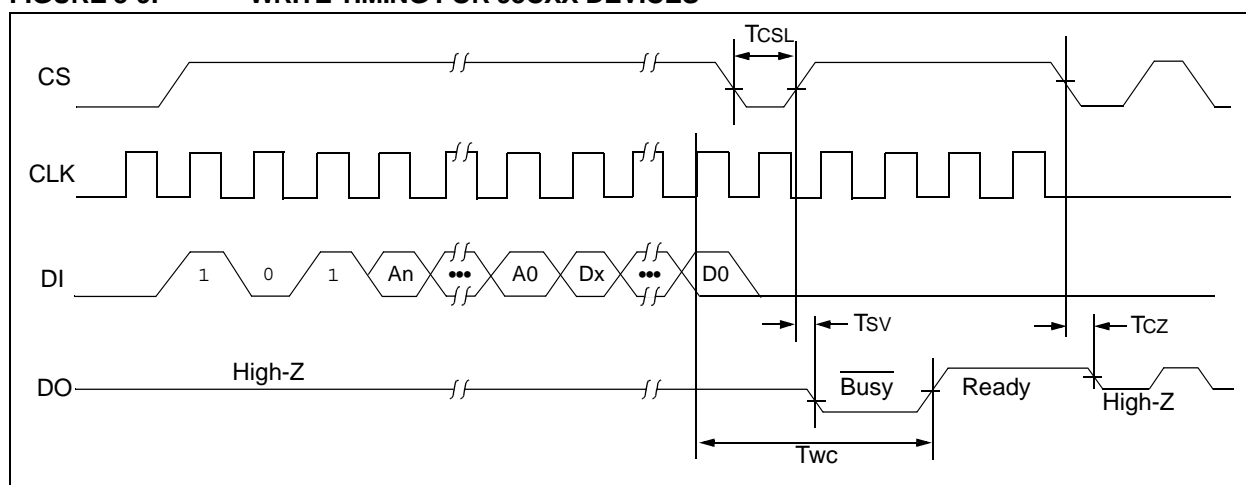


FIGURE 3-9: WRITE TIMING FOR 93CXX DEVICES



93XX46X/56X/66X/76X/86X

3.9 WRITE ALL (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AAXX and 93LCXX devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93CXX devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

VCC must be $\geq 4.5V$ for proper operation of WRAL.

Note: For devices with PE functionality such as the 93XX76C or 93XX86C, the write sequence requires a logic high signal on the PE pin prior to the rising edge of clock on the last data bit.

Note: After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 3-10: WRAL TIMING FOR 93AAXX AND 93LCXX DEVICES

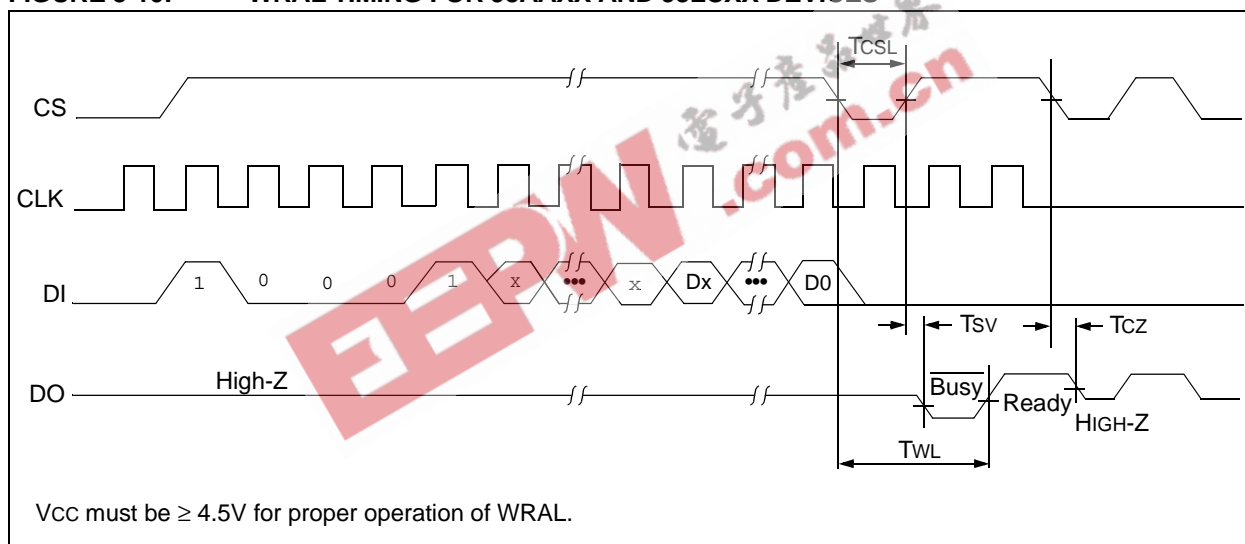
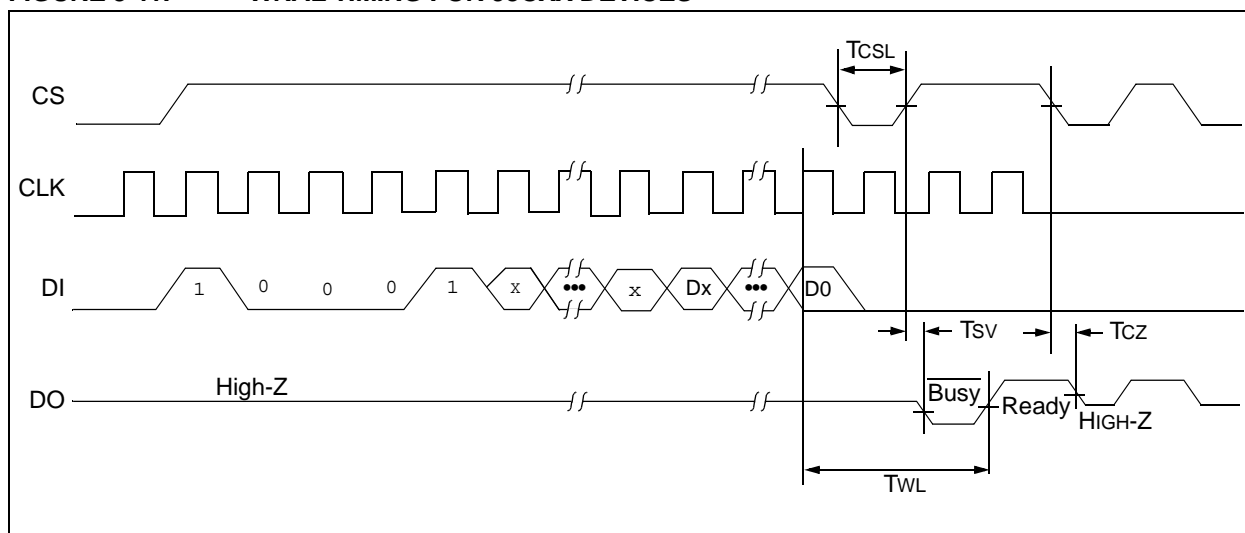


FIGURE 3-11: WRAL TIMING FOR 93CXX DEVICES



93XX46X/56X/66X/76X/86X

4.0 PIN DESCRIPTIONS

TABLE 4-1: PIN DESCRIPTIONS

| Name | SOIC/PDIP/MSOP/ TSSOP/DFN | SOT-23 | Function |
|-------------------|------------------------------|--------|--|
| CS | 1 | 5 | Chip Select |
| CLK | 2 | 4 | Serial Clock |
| DI | 3 | 3 | Data In |
| DO | 4 | 1 | Data Out |
| Vss | 5 | 2 | Ground |
| ORG | 6 | N/A | Organization (93XX46C/56C/66C/76C/86C) |
| NC ⁽¹⁾ | | | No connect on 93XXA/B devices |
| PE | 7 | N/A | Program Enable (93XX76C/86C) |
| NC ⁽¹⁾ | | | No connect on 93XXA/B devices |
| Vcc | 8 | 6 | Power Supply |

Note 1: With no internal connection, logic levels on NC pins are “don't cares.”

4.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T_{CSL}) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to Clock High Time (T_{CKH}) and Clock Low Time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “don't care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed Write (i.e., auto Erase/Write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become “don't care” inputs waiting for a new Start condition to be detected.

4.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

4.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides Ready/Busy status information during Erase and Write cycles. Ready/Busy status information is available on the DO pin if CS is brought high after being low for minimum Chip Select Low Time (T_{CSL}) and an erase or write operation has been initiated.

The Status signal is not available on DO, if CS is held low during the entire Erase or Write cycle. In this case, DO is in the High-Z mode. If status is checked after the Erase/Write cycle, the data line will be high to indicate the device is ready.

Note: After the Read cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

93XX46X/56X/66X/76X/86X

4.5 Organization (ORG)

When the ORG pin is connected to VCC or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to Vss or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

For devices without the ORG functionality, there is no internal connection to the ORG pin. In these devices the functionality has been set at the factory to support a single word size.

'A' series devices – x8 organization

'B' series devices – x16 organization

4.6 Program Enable (PE)

A logic level on the PE pin will enable or disable the ability to write data to the memory array in only the 8-lead 93XX76C and 93XX86C devices. For all other devices the PE function is not present and the PE pin is a no connect. When driving the PE pin to a logic High, the device can be programmed, but when the PE pin is driven Low, programming is inhibited. This pin is used in parallel with the EWEN/EWDS latch to protect the memory array from inadvertent writes, as shown in Table 4-2.

In either the 93XX76C or 93XX86C devices, the PE pin must be tied to a specific logic level and cannot be floated. In all other devices without the PE function, the PE pin has no internal connections and programming is always enabled.

TABLE 4-2: WRITE PROTECTION SCHEME

| EWEN/EWDS Latch | PE Pin* | Array WRITE |
|-----------------|---------|-------------|
| Enabled | 1 | Yes |
| Disabled | 1 | No |
| Enabled | 0 | No |
| Disabled | 0 | No |

* PE pin level does not alter the state of the EWEN/EWDS latch.

Note: For devices with PE functionality such as 93XX76C or 93XX86C, the write sequence requires a logic high signal on the PE pin prior to the rising edge of clock on the last data bit.

APPENDIX A: REVISION HISTORY

Revision A

Original release of document. Combined all the 93-Series Microwire Serial EEPROM device data sheets.

Revision B

Revised 2x3 (MC) DFN package drawing.

Revision C

Correction to Table 2-6, 93XX76A (EWDS).

Revision D (03/2007)

Revised Description; Delete Pb-free notes; Replaced Package Drawings; Revised Product ID System.

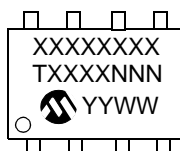
EEPW 电子產品世界
.com.cn

93XX46X/56X/66X/76X/86X

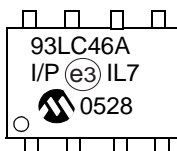
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead PDIP



Example: Pb-free



| 3-Wire 8-Lead PDIP Package Marking | | | | | |
|------------------------------------|----------------|---------|----------------|--------|----------------|
| Part | Line 1 Marking | Part | Line 1 Marking | Part | Line 1 Marking |
| 93AA46A | 93AA46A | 93LC46A | 93LC46A | 93C46A | 93C46A |
| 93AA46B | 93AA46B | 93LC46B | 93LC46B | 93C46B | 93C46B |
| 93AA46C | 93AA46C | 93LC46C | 93LC46C | 93C46C | 93C46C |
| 93AA56A | 93AA56A | 93LC56A | 93LC56A | 93C56A | 93C56A |
| 93AA56B | 93AA56B | 93LC56B | 93LC56B | 93C56B | 93C56B |
| 93AA56C | 93AA56C | 93LC56C | 93LC56C | 93C56C | 93C56C |
| 93AA66A | 93AA66A | 93LC66A | 93LC66A | 93C66A | 93C66A |
| 93AA66B | 93AA66B | 93LC66B | 93LC66B | 93C66B | 93C66B |
| 93AA66C | 93AA66C | 93LC66C | 93LC66C | 93C66C | 93C66C |
| 93AA76A | 93AA76A | 93LC76A | 93LC76A | 93C76A | 93C76A |
| 93AA76B | 93AA76B | 93LC76B | 93LC76B | 93C76B | 93C76B |
| 93AA76C | 93AA76C | 93LC76C | 93LC76C | 93C76C | 93C76C |
| 93AA86A | 93AA86A | 93LC86A | 93LC86A | 93C86A | 93C86A |
| 93AA86B | 93AA86B | 93LC86B | 93LC86B | 93C86B | 93C86B |
| 93AA86C | 93AA86C | 93LC86C | 93LC86C | 93C86C | 93C86C |

Note: Temperature range on second line.

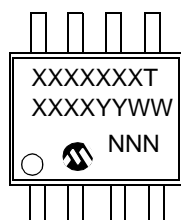
Legend: XX...X Part number or part number code
T Temperature (I, E)
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code (2 characters for small packages)
(e3) Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

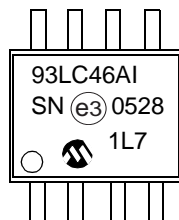
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

93XX46X/56X/66X/76X/86X

8-Lead SOIC



Example: Pb-free



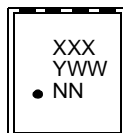
| 3-Wire 8-Lead SOIC (SN) Package Marking | | | | | |
|---|----------------|---------|----------------|--------|----------------|
| Part | Line 1 Marking | Part | Line 1 Marking | Part | Line 1 Marking |
| 93AA46A | 93AA46AT | 93LC46A | 93LC46AT | 93C46A | 93C46AT |
| 93AA46B | 93AA46BT | 93LC46B | 93LC46BT | 93C46B | 93C46BT |
| 93AA46C | 93AA46CT | 93LC46C | 93LC46CT | 93C46C | 93C46CT |
| 93AA56A | 93AA56AT | 93LC56A | 93LC56AT | 93C56A | 93C56AT |
| 93AA56B | 93AA56BT | 93LC56B | 93LC56BT | 93C56B | 93C56BT |
| 93AA56C | 93AA56CT | 93LC56C | 93LC56CT | 93C56C | 93C56CT |
| 93AA66A | 93AA66AT | 93LC66A | 93LC66AT | 93C66A | 93C66AT |
| 93AA66B | 93AA66BT | 93LC66B | 93LC66BT | 93C66B | 93C66BT |
| 93AA66C | 93AA66CT | 93LC66C | 93LC66CT | 93C66C | 93C66CT |
| 93AA76A | 93AA76AT | 93LC76A | 93LC76AT | 93C76A | 93C76AT |
| 93AA76B | 93AA76BT | 93LC76B | 93LC76BT | 93C76B | 93C76BT |
| 93AA76C | 93AA76CT | 93LC76C | 93LC76CT | 93C76C | 93C76CT |
| 93AA86A | 93AA86AT | 93LC86A | 93LC86AT | 93C86A | 93C86AT |
| 93AA86B | 93AA86BT | 93LC86B | 93LC86BT | 93C86B | 93C86BT |
| 93AA86C | 93AA86CT | 93LC86C | 93LC86CT | 93C86C | 93C86CT |

Note: T = Temperature Range: I = Industrial, E = Extended

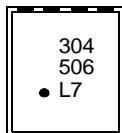
| | | |
|----------------|---|--|
| Legend: | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| Note: | For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label. | |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. | |

93XX46X/56X/66X/76X/86X

8-Lead 2x3 DFN



Example:



| 3-Wire 2x3 DFN Package Marking | | | | | | | | |
|--------------------------------|---------------------------|-----------------------|---------|---------------------------|-----------------------|--------|---------------------------|-----------------------|
| Part | Industrial Line 1 Marking | E-Temp Line 1 Marking | Part | Industrial Line 1 Marking | E-Temp Line 1 Marking | Part | Industrial Line 1 Marking | E-Temp Line 1 Marking |
| 93AA46A | 301 | 302 | 93LC46A | 304 | 305 | 93C46A | 307 | 308 |
| 93AA46B | 311 | 312 | 93LC46B | 314 | 315 | 93C46B | 317 | 318 |
| 93AA46C | 321 | 322 | 93LC46C | 324 | 325 | 93C46C | 327 | 328 |
| | | | | | | | | |
| 93AA56A | 331 | 332 | 93LC56A | 334 | 335 | 93C56A | 337 | 338 |
| 93AA56B | 341 | 342 | 93LC56B | 344 | 345 | 93C56B | 347 | 348 |
| 93AA56C | 351 | 352 | 93LC56C | 354 | 355 | 93C56C | 357 | 358 |
| | | | | | | | | |
| 93AA66A | 361 | 362 | 93LC66A | 364 | 365 | 93C66A | 367 | 368 |
| 93AA66B | 371 | 372 | 93LC66B | 374 | 375 | 93C66B | 377 | 378 |
| 93AA66C | 381 | 382 | 93LC66C | 384 | 385 | 93C66C | 387 | 388 |
| | | | | | | | | |
| 93AA76C | 3B1 | 3B2 | 93LC76C | 3B4 | 3B5 | 93C76C | 3B7 | 3B8 |
| | | | | | | | | |
| 93AA86C | 3E1 | 3E2 | 93LC86C | 3E4 | 3E5 | 93C86C | 3E7 | 3E8 |

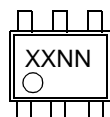
Legend: XX...X Part number or part number code
T Temperature (I, E)
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code (2 characters for small packages)
(e3) Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

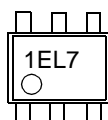
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

93XX46X/56X/66X/76X/86X

6-Lead SOT-23



Example:

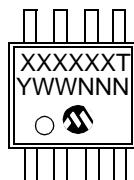


| 3-Wire 6-Lead SOT-23 Package Marking | | | | | | | | |
|--------------------------------------|---------------------------|-----------------------|---------|---------------------------|-----------------------|--------|---------------------------|-----------------------|
| Part | Industrial Line 1 Marking | E-Temp Line 1 Marking | Part | Industrial Line 1 Marking | E-Temp Line 1 Marking | Part | Industrial Line 1 Marking | E-Temp Line 1 Marking |
| 93AA46A | 1BNN | 1CNN | 93LC46A | 1ENN | 1FNN | 93C46A | 1HNN | 1JNN |
| 93AA46B | 1LNN | 1MNN | 93LC46B | 1PNN | 1RNN | 93C46B | 1TNN | 1UNN |
| 93AA56A | 2BNN | 2CNN | 93LC56A | 2ENN | 2FNN | 93C56A | 2HNN | 2JNN |
| 93AA56B | 2LNN | 2MNN | 93LC56B | 2PNN | 2RNN | 93C56B | 2TNN | 2UNN |
| 93AA66A | 3BNN | 3CNN | 93LC66A | 3ENN | 3FNN | 93C66A | 3HNN | 3JNN |
| 93AA66B | 3LNN | 3MNN | 93LC66B | 3PNN | 3RNN | 93C66B | 3TNN | 3UNN |
| 93AA76A | 4BNN | 4CNN | 93LC76A | 4ENN | 4FNN | 93C76A | 4HNN | 4JNN |
| 93AA76B | 4LNN | 4MNN | 93LC76B | 4PNN | 4RNN | 93C76B | 4TNN | 4UNN |
| 93AA86A | 5BNN | 5CNN | 93LC86A | 5ENN | 5FNN | 93C86A | 5HNN | 5JNN |
| 93AA86B | 5LNN | 5MNN | 93LC86B | 5PNN | 5RNN | 93C86B | 5TNN | 5UNN |

| | | |
|----------------|---|--|
| Legend: | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | e3 | Pb-free JEDEC designator for Matte Tin (Sn) |
| Note: | For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label. | |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. | |

93XX46X/56X/66X/76X/86X

8-Lead MSOP (150 mil)



Example:



| 3-Wire 8-Lead MSOP Package Marking | | | | | |
|------------------------------------|----------------|---------|----------------|--------|----------------|
| Part | Line 1 Marking | Part | Line 1 Marking | Part | Line 1 Marking |
| 93AA46A | 3A46AT | 93LC46A | 3L46AT | 93C46A | 3C46AT |
| 93AA46B | 3A46BT | 93LC46B | 3L46BT | 93C46B | 3C46BT |
| 93AA46C | 3A46CT | 93LC46C | 3L46CT | 93C46C | 3C46CT |
| 93AA56A | 3A56AT | 93LC56A | 3L56AT | 93C56A | 3C56AT |
| 93AA56B | 3A56BT | 93LC56B | 3L56BT | 93C56B | 3C56BT |
| 93AA56C | 3A56CT | 93LC56C | 3L56CT | 93C56C | 3C56CT |
| 93AA66A | 3A66AT | 93LC66A | 3L66AT | 93C66A | 3C66AT |
| 93AA66B | 3A66BT | 93LC66B | 3L66BT | 93C66B | 3C66BT |
| 93AA66C | 3A66CT | 93LC66C | 3L66CT | 93C66C | 3C66CT |
| 93AA76A | 3A76AT | 93LC76A | 3L76AT | 93C76A | 3C76AT |
| 93AA76B | 3A76BT | 93LC76B | 3L76BT | 93C76B | 3C76BT |
| 93AA76C | 3A76CT | 93LC76C | 3L76CT | 93C76C | 3C76CT |
| 93AA86A | 3A86AT | 93LC86A | 3L86AT | 93C86A | 3C86AT |
| 93AA86B | 3A86BT | 93LC86B | 3L86BT | 93C86B | 3C86BT |
| 93AA86C | 3A86CT | 93LC86C | 3L86CT | 93C86C | 3C86CT |

Note: T = Temperature Range: I = Industrial, E = Extended

Legend: XX...X Part number or part number code
T Temperature (I, E)
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code (2 characters for small packages)
(e3) Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

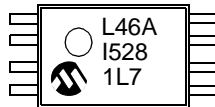
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

93XX46X/56X/66X/76X/86X

8-Lead TSSOP



Example:



| 3-Wire 8-Lead TSSOP Package Marking | | | | | |
|-------------------------------------|----------------|---------|----------------|--------|----------------|
| Part | Line 1 Marking | Part | Line 1 Marking | Part | Line 1 Marking |
| 93AA46A | A46A | 93LC46A | L46A | 93C46A | C46A |
| 93AA46B | A46B | 93LC46B | L46B | 93C46B | C46B |
| 93AA46C | A46C | 93LC46C | L46C | 93C46C | C46C |
| 93AA56A | A56A | 93LC56A | L56A | 93C56A | C56A |
| 93AA56B | A56B | 93LC56B | L56B | 93C56B | C56B |
| 93AA56C | A56C | 93LC56C | L56C | 93C56C | C56C |
| 93AA66A | A66A | 93LC66A | L66A | 93C66A | C66A |
| 93AA66B | A66B | 93LC66B | L66B | 93C66B | C66B |
| 93AA66C | A66C | 93LC66C | L66C | 93C66C | C66C |
| 93AA76A | A76A | 93LC76A | L76A | 93C76A | C76A |
| 93AA76B | A76B | 93LC76B | L76B | 93C76B | C76B |
| 93AA76C | A76C | 93LC76C | L76C | 93C76C | C76C |
| 93AA86A | A86A | 93LC86A | L86A | 93C86A | C86A |
| 93AA86B | A86B | 93LC86B | L86B | 93C86B | C86B |
| 93AA86C | A86C | 93LC86C | L86C | 93C86C | C86C |

Note: Temperature range on second line.

| | | |
|----------------|--------|--|
| Legend: | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |

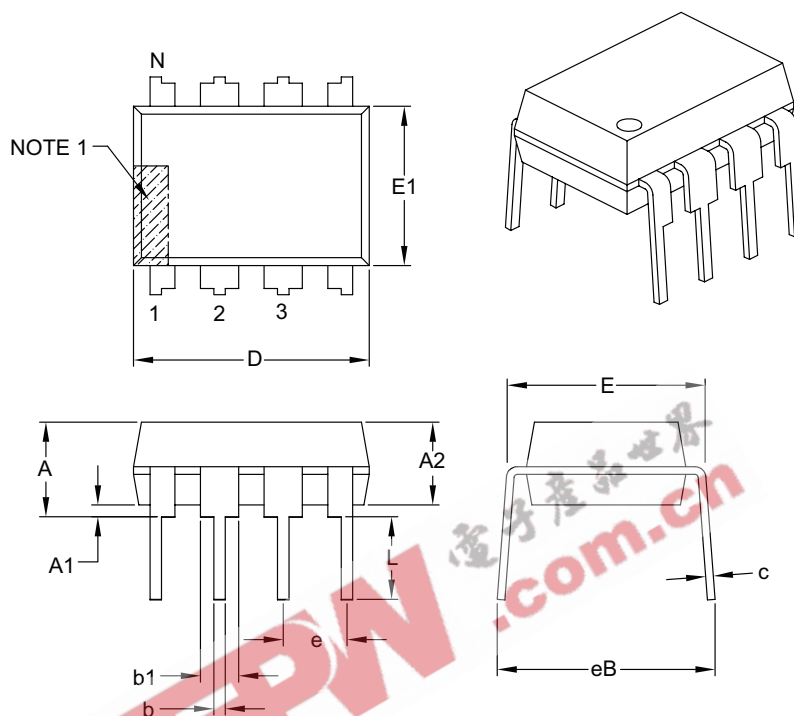
Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

93XX46X/56X/66X/76X/86X

8-Lead Plastic Dual In-Line (P or PA) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | INCHES | | |
|----------------------------|----|----------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | — | — | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | — | — |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | — | — | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

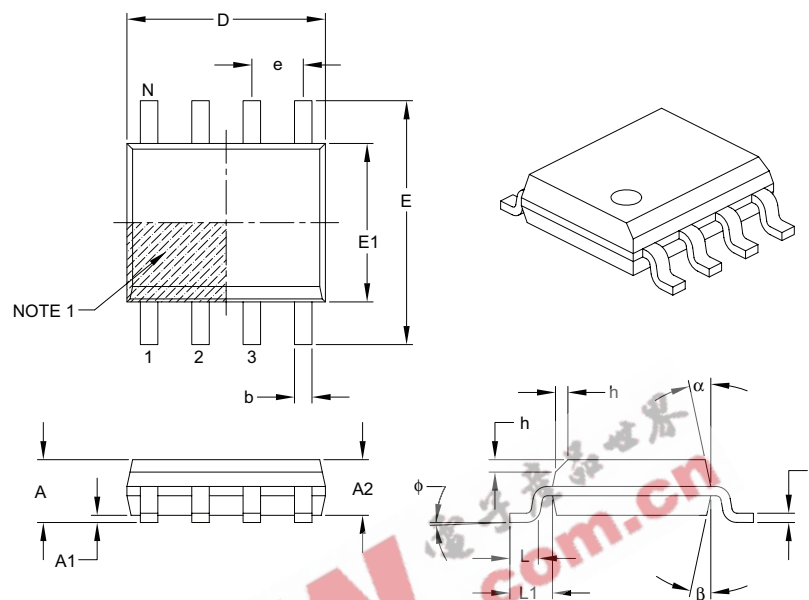
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

93XX46X/56X/66X/76X/86X

8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

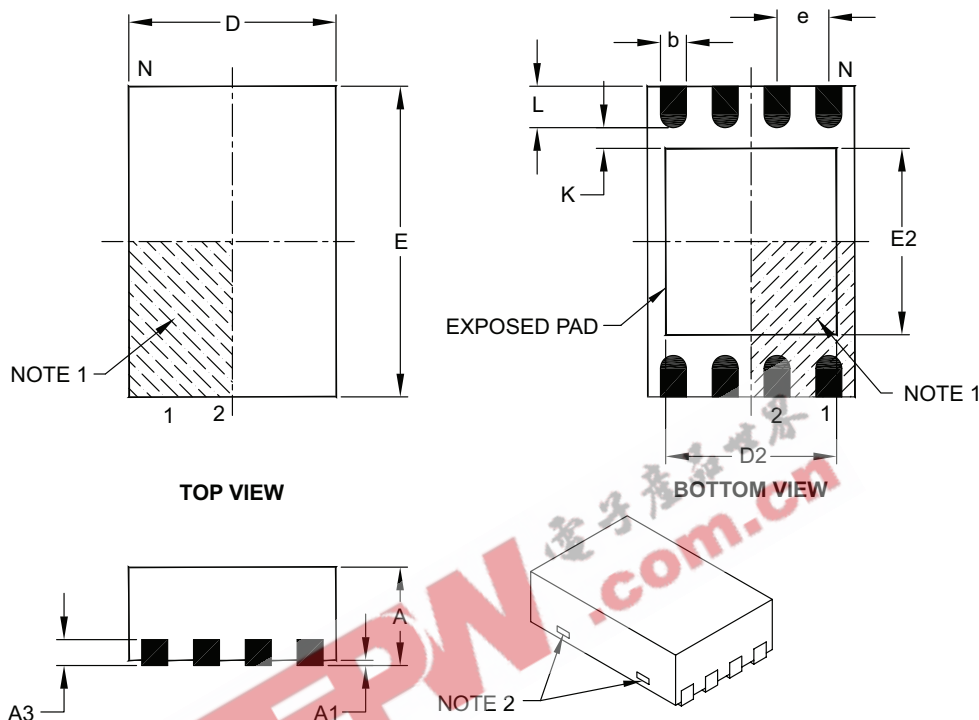
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

93XX46X/56X/66X/76X/86X

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 2.00 BSC | | |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Length | D2 | 1.30 | – | 1.75 |
| Exposed Pad Width | E2 | 1.50 | – | 1.90 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

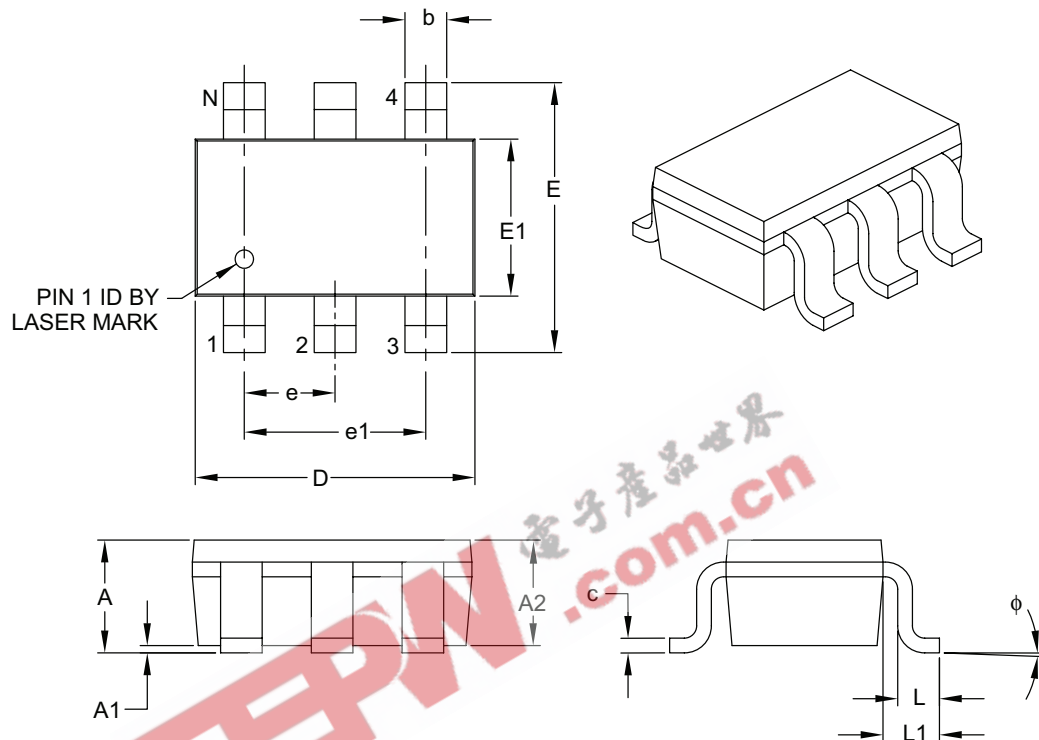
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B

93XX46X/56X/66X/76X/86X

6-Lead Plastic Small Outline Transistor (CH or OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 6 | | |
| Pitch | e | 0.95 BSC | | |
| Outside Lead Pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | — | 1.45 |
| Molded Package Thickness | A2 | 0.89 | — | 1.30 |
| Standoff | A1 | 0.00 | — | 0.15 |
| Overall Width | E | 2.20 | — | 3.20 |
| Molded Package Width | E1 | 1.30 | — | 1.80 |
| Overall Length | D | 2.70 | — | 3.10 |
| Foot Length | L | 0.10 | — | 0.60 |
| Footprint | L1 | 0.35 | — | 0.80 |
| Foot Angle | φ | 0° | — | 30° |
| Lead Thickness | c | 0.08 | — | 0.26 |
| Lead Width | b | 0.20 | — | 0.51 |

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

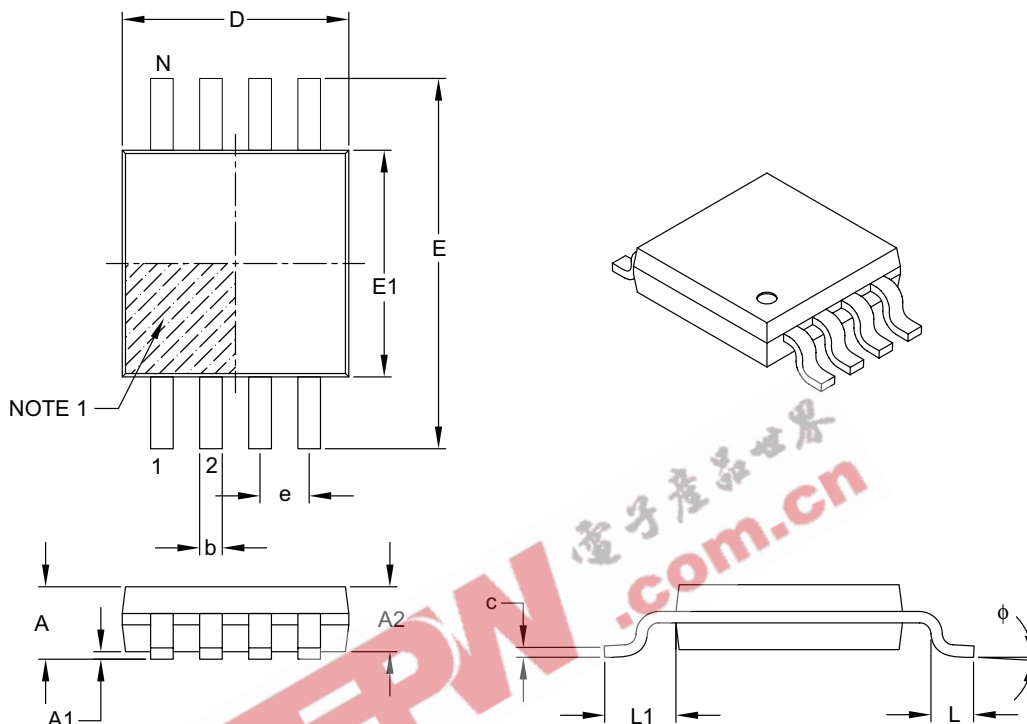
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

93XX46X/56X/66X/76X/86X

8-Lead Plastic Micro Small Outline Package (MS or UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| | | Units | MILLIMETERS | | |
|--------------------------|----|-------|-------------|------|------|
| Dimension Limits | | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | | |
| Pitch | e | | 0.65 BSC | | |
| Overall Height | A | | — | — | 1.10 |
| Molded Package Thickness | A2 | | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | | 0.00 | — | 0.15 |
| Overall Width | E | | 4.90 BSC | | |
| Molded Package Width | E1 | | 3.00 BSC | | |
| Overall Length | D | | 3.00 BSC | | |
| Foot Length | L | | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | | |
| Foot Angle | φ | | 0° | — | 8° |
| Lead Thickness | c | | 0.08 | — | 0.23 |
| Lead Width | b | | 0.22 | — | 0.40 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

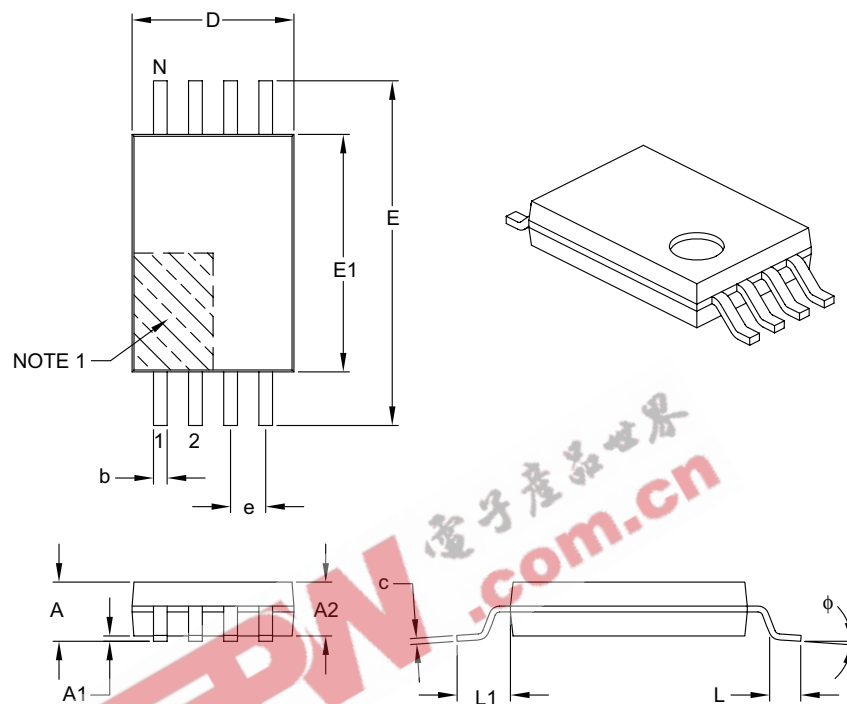
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

93XX46X/56X/66X/76X/86X

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|--------------------------|----|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | 6.40 BSC | | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | 1.00 REF | | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

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93XX46X/56X/66X/76X/86X

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93XX46X/56X/66X/76X/86X

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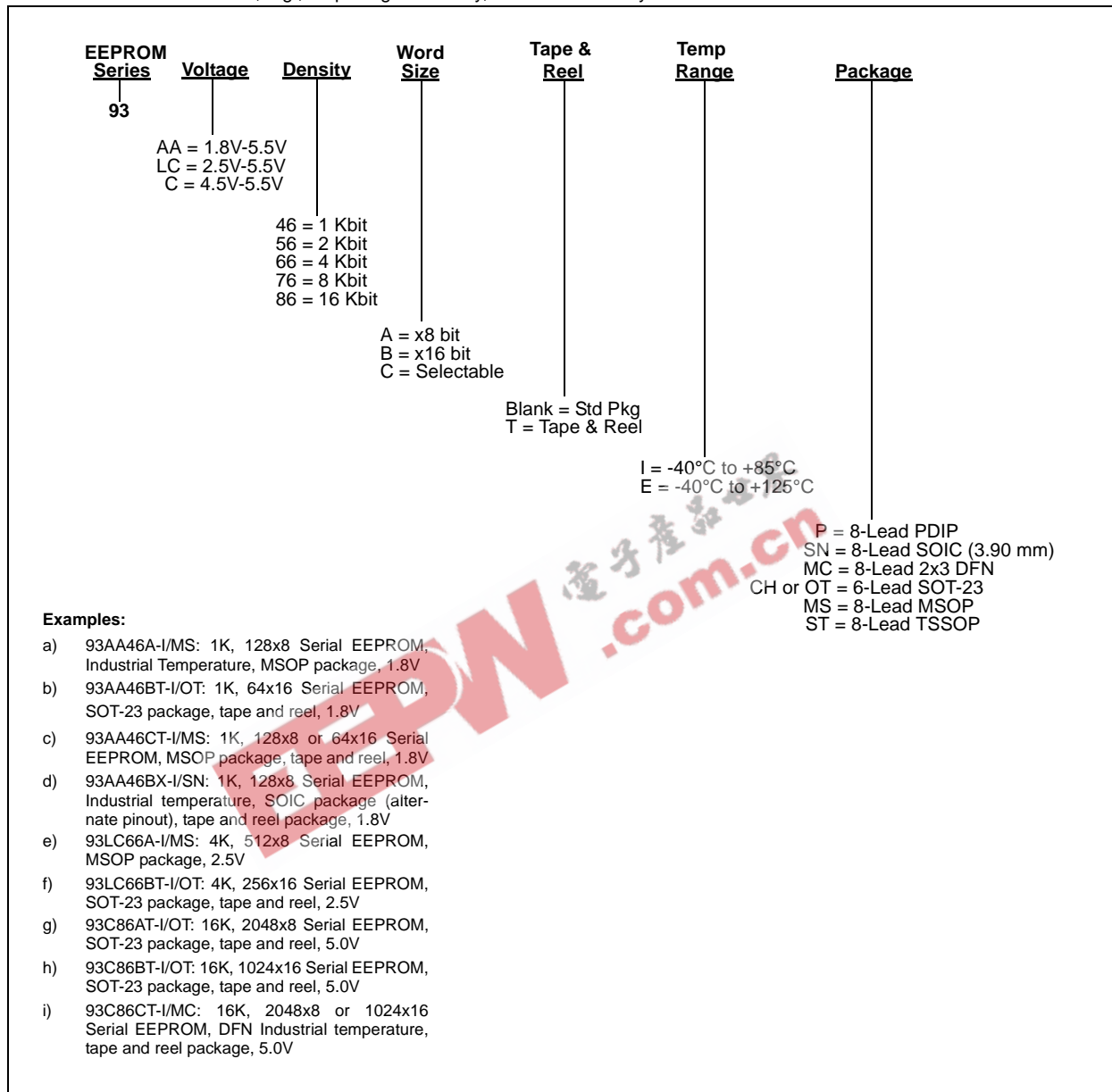
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