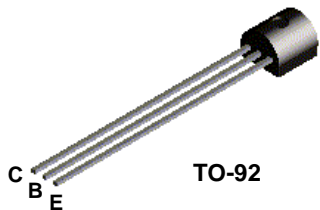




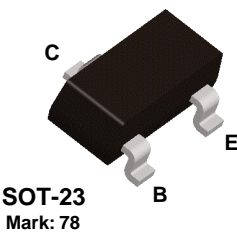
Discrete POWER & Signal
Technologies

PN4258 / MMBT4258

PN4258



MMBT4258



PNP Switching Transistor

This device is designed for very high speed saturate switching at collector currents to 100 mA. Sourced from Process 65.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V _{CEO}	Collector-Emitter Voltage	12	V
V _{CBO}	Collector-Base Voltage	12	V
V _{EBO}	Emitter-Base Voltage	4.5	V
I _C	Collector Current - Continuous	200	mA
T _J , T _{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

- 1) These ratings are based on a maximum junction temperature of 150 degrees C.
- 2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics

TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		PN4258	*MMBT4258	
P _D	Total Device Dissipation	350	225	mW
	Derate above 25°C	2.8	1.8	mW/°C
R _{θJC}	Thermal Resistance, Junction to Case	125		°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient	357	556	°C/W

* Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

Electrical Characteristics

TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
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OFF CHARACTERISTICS

$V_{(BR)CES}$	Collector-Emitter Breakdown Voltage*	$I_C = 100\ \mu A, V_{BE} = 0$	12		V
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage*	$I_C = 3.0\ mA, I_E = 0$	12		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100\ \mu A, I_E = 0$	12		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 100\ \mu A, I_C = 0$	4.5		V
I_{CES}	Collector Cutoff Current	$V_{CE} = 6.0\ V, V_{BE} = 0$ $V_{CE} = 6.0\ V, V_{BE} = 0, T_A = 65^\circ C$		0.01 5.0	μA μA

ON CHARACTERISTICS*

h_{FE}	DC Current Gain	$I_C = 1.0\ mA, V_{CE} = 0.5\ V$ $I_C = 10\ mA, V_{CE} = 3.0\ V$ $I_C = 50\ mA, V_{CE} = 1.0\ V$	15 30 30	120	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10\ mA, I_B = 1.0\ mA$ $I_C = 50\ mA, I_B = 5.0\ mA$		0.15 0.5	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 10\ mA, I_B = 1.0\ mA$ $I_C = 50\ mA, I_B = 5.0\ mA$	0.75	0.95 1.5	V V

SMALL SIGNAL CHARACTERISTICS

f_T	Current Gain - Bandwidth Product	$I_C = 10\ mA, V_{CE} = 5.0\ V,$ $f = 100\ MHz$ $I_C = 10\ mA, V_{CE} = 10\ V,$ $f = 100\ MHz$	700 700		MHz MHz
C_{ibo}	Input Capacitance	$V_{BE} = 0.5\ V, I_C = 0,$ $f = 1.0\ MHz$		3.5	pF
C_{cb}	Collector-Base Capacitance	$V_{CB} = 5.0\ V, I_E = 0,$ $f = 1.0\ MHz$		3.0	pF

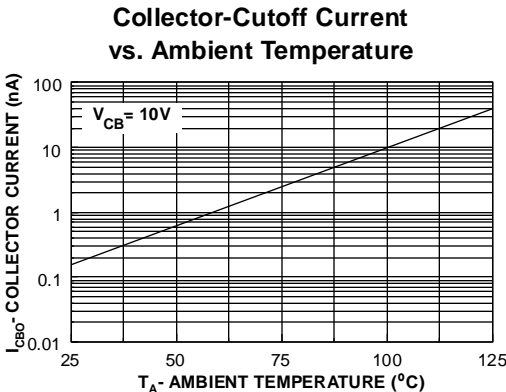
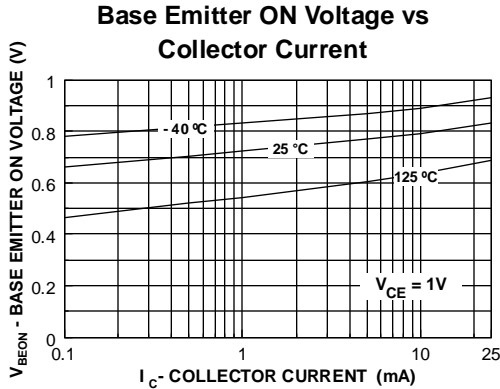
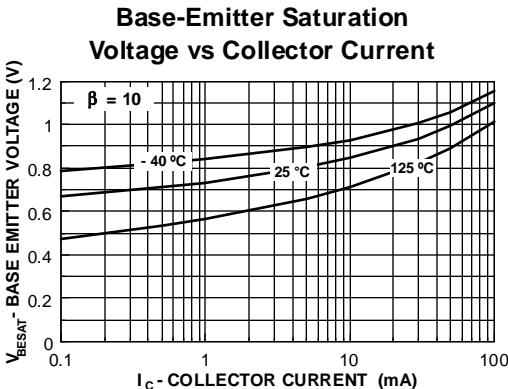
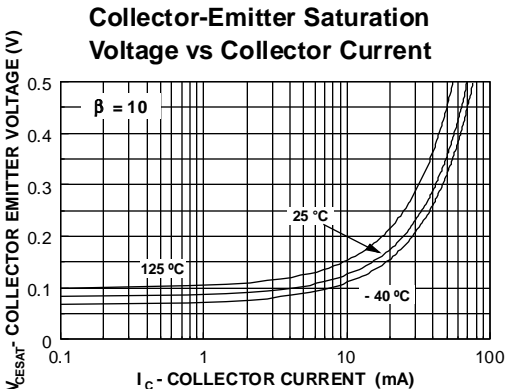
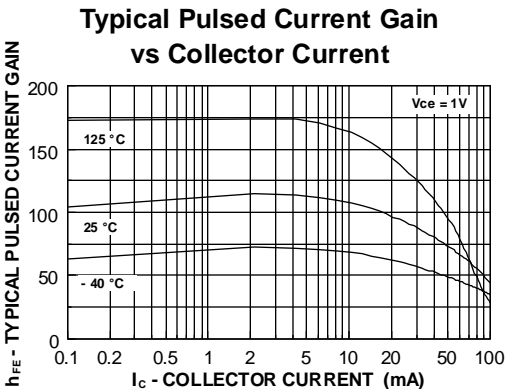
SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{CC} = 1.5\ V, V_{BE(off)} = 0\ V,$		15	ns
t_d	Delay Time	$I_C = 10\ mA, I_{B1} = 1.0\ mA$		10	ns
t_r	Rise Time			15	ns
t_{off}	Turn-Off Time	$V_{CC} = 1.5\ V, I_C = 10\ mA$		20	ns
t_s	Storage Time	$I_{B1} = I_{B2} = 1.0\ mA$		20	ns
t_f	Fall Time			10	ns
t_s	Storage Time	$I_C = 10\ mA, I_{B1} = I_{B2} = 10\ mA$		20	ns

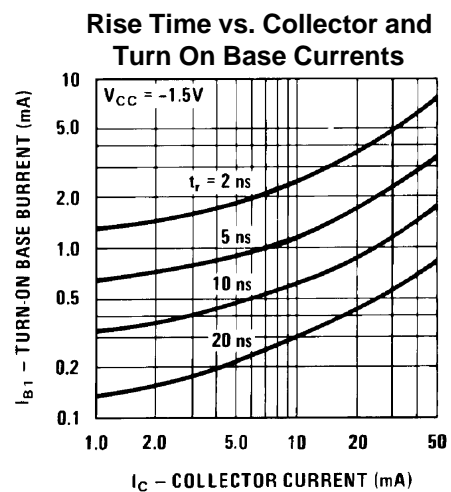
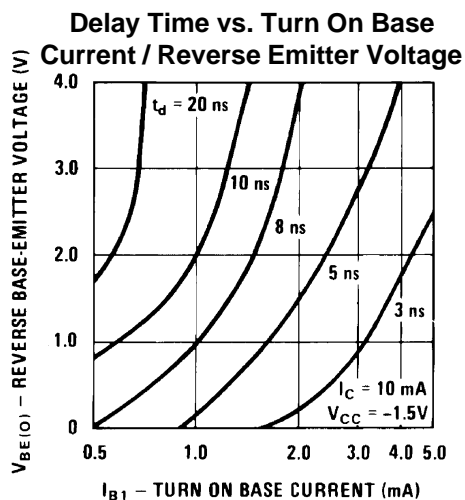
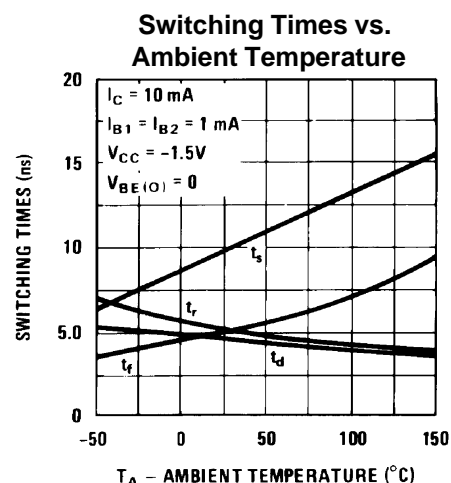
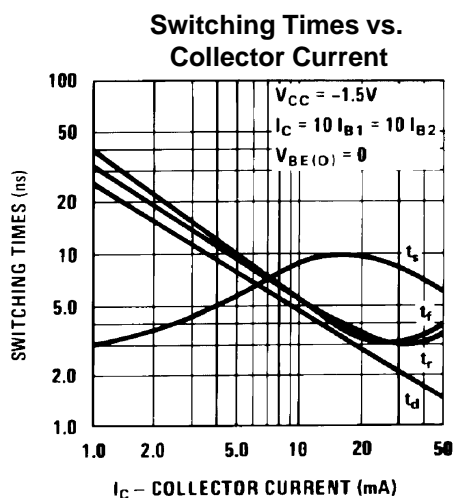
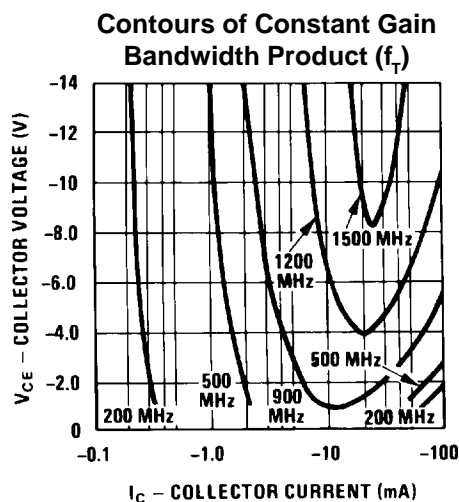
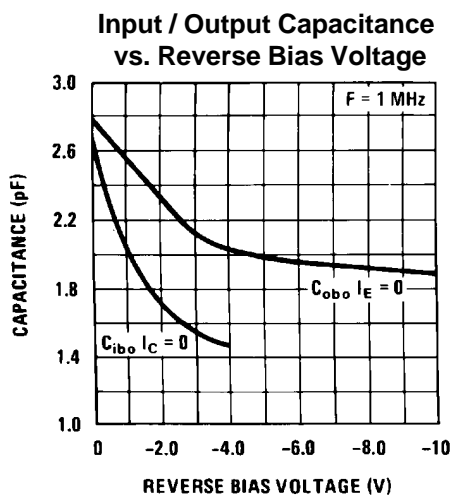
*Pulse Test: Pulse Width $\leq 300\ \mu s$, Duty Cycle $\leq 2.0\%$
Spice Model

PNP (Is=545.6E-18 Xti=3 Eg=1.11 Vaf=100 Bf=61.42 Ne=1.5 Ise=0 Ikf=50m Xtb=1.5 Br=1.426 Nc=2 Isc=0 Ikr=0 Rc=3.75 Cjc=2.77p Mjc=.1416 Vjc=.75 Fc=.5 Cje=2.65p Mje=.3083 Vje=.75 Tr=4.109n Tf=118.5p Itf=.5 Vtf=3 Xtf=6 Rb=10)

DC Typical Characteristics

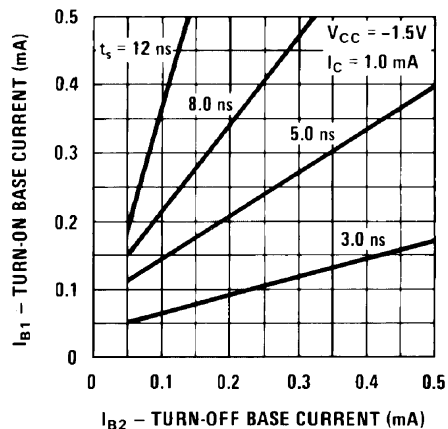


AC Typical Characteristics

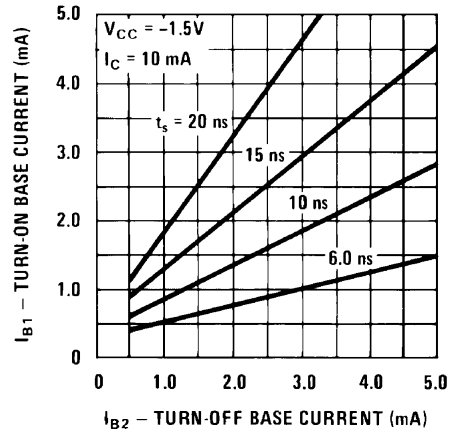


AC Typical Characteristics (continued)

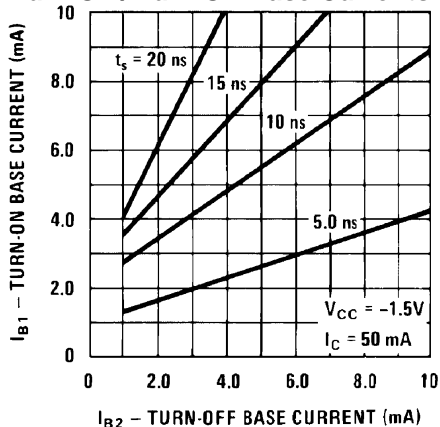
Storage Time vs.
Turn On / Turn Off Base Currents



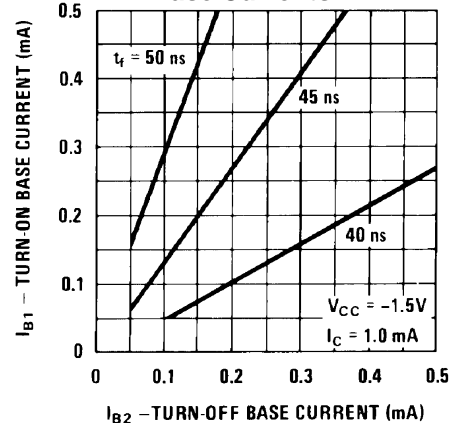
Storage Time vs.
Turn On / Turn Off Base Currents



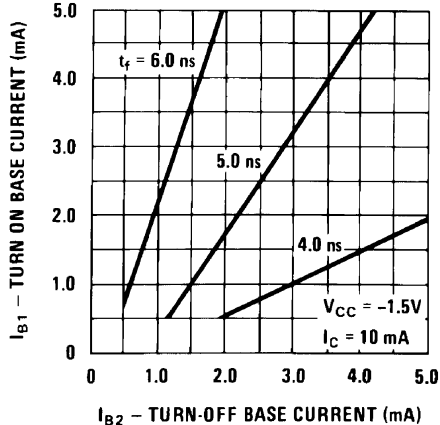
Storage Time vs.
Turn On / Turn Off Base Currents



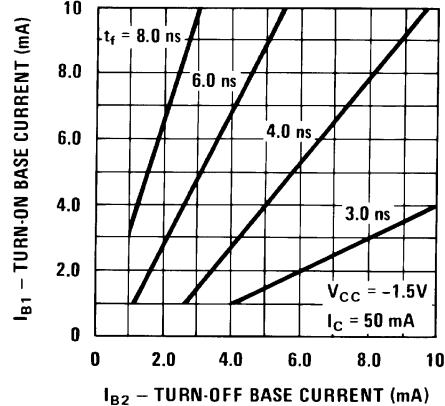
Fall Time vs. Turn On / Turn Off
Base Currents



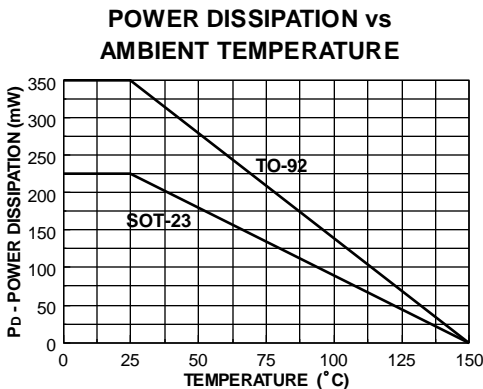
Fall Time vs. Turn On / Turn Off
Base Currents



Fall Time vs. Turn On / Turn Off
Base Currents



AC Typical Characteristics (continued)



Test Circuit

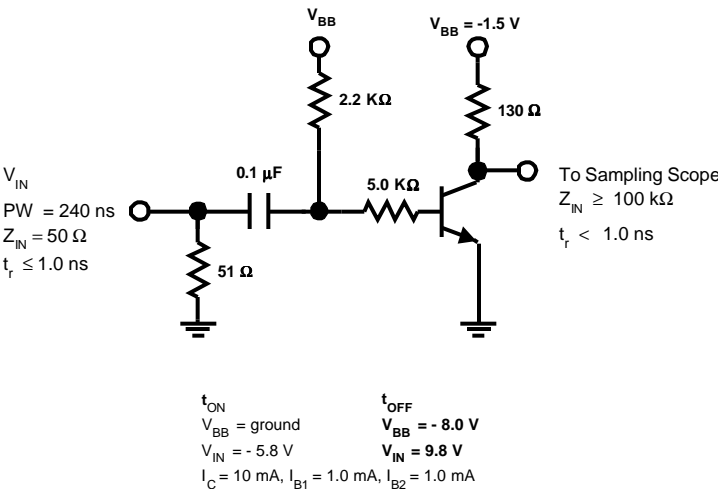


FIGURE 1: t_{ON}, t_{OFF} Test Circuit