



Wireless Components

Gain-controlled IF Amplifier

TDA6192 Version 2.1

Specification May 2002

| CONFIDENTIAL | | |
|--|---------------------------------|--|
| Revision History: Current Version: V1.1, October 2000 | | |
| Previous Version:target Data Sheet V1.0, April 2000 | | |
| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
| all | all | version to V1.1, date to October 2000 |
| div | div | TDA6192-V in VQFN-20 package |
| 3-3 ff | 3-3 ff | DC levels added |
| 5-2 | 5-2 | Thermal resistance TDA6192-T to 230 K/W |
| 5-4 | 5-4 | Current consumption: tbfs replaced |

| Revision History: Current Version: V1.2, March 2001 | | |
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| Previous Version:target Data Sheet V1.1, October 2000 | | |
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| all | all | status to preliminary,version to V1.2, date to March 2001 |
| 5-2 | 5-2 | Footnote ESD-Protection changed |
| 5-4 | 5-4 | Current consumption changed, VREF vs temperature: T_{amb} changed , IF input voltage: typ value added, Take-over point voltage: typ value added and disable threshold specified, IF AGC voltage deleted |
| 5-5 | 5-5 | Tuner AGC max. slope, Intermodulation, SNR: typ value added, OIP3 added |
| | 5-7, 5-8, 5-9 | Diagrams added |

| Revision History: Current Version: V1.3, April 2001 | | |
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| Previous Version:target Data Sheet V1.2, March 2001 | | |
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| all | all | status to preliminary, version to V1.3, date to April 2001 |
| 3-4 | 3-4 | pins 13, 14: DC level corrected |
| 5-4 | 5-4 | Current consumption corrected |

| Revision History: Current Version: V2.0, February 2002 | | |
|---|---------------------------------|---|
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| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
| all | all | status to final, version to V2.0, date to February 2002 |

| Revision History: Current Version: V2.0, February 2002 | | |
|---|----------|---|
| 4-2, 4-3 | 4-2, 4-3 | application circuits changed |
| 5-2 | 5-2 | thermal resistance TDA6192-V added |
| 5-5 | 5-5 | noise figure added, output impedance values added |

| Revision History: Current Version: V2.1, May 2002 | | |
|--|---------------------------|--|
| Previous Version: Data Sheet V2.0, February 2002 | | |
| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
| 3-2, 3-3, 3-5, 4-2 | 3-2, 3-3, 3-5, 4-2 | pinning of TDA6192-V changed |

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Product Info

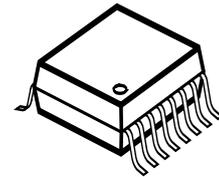
General Description The **TDA6192** is a 5 V gain-controlled IF amplifier for digital and analog front-ends

Package



TDA6192-V

- Features**
- Input frequency range 30 to 65 MHz
 - Low intermodulation distortion
 - 48 dB AGC range
 - balanced 1 V_{pp} buffered output
 - Input for gain-control voltage
 - Output for tuner AGC with take-over point adjust
 - Internal low noise reference voltage
 - Full ESD protection



TDA6192-T

- Application**
- IF amplifier in DVB-C, DVB-T, ATSC and ISDB-T frontends with direct IF-sampling.
 - IF amplifier in PAL or NTSC front-ends

Ordering Information

| Type | Ordering Code | Package |
|-----------|-----------------------------|-----------------------------|
| TDA6192-V | Q67037-A1125(tape and reel) | P-VQFN-20-3 (on request) |
| TDA6192-T | Q67037-A1073(tape and reel) | P-TSSOP-16-1 |

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2 Product Description

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2.1 General Description

The **TDA6192** device combines a gain-controlled amplifier, an output buffer to drive a following channel decoder IC and a delayed tuner AGC with take-over point adjustment. The gain is controlled by an external voltage.

2.2 Features

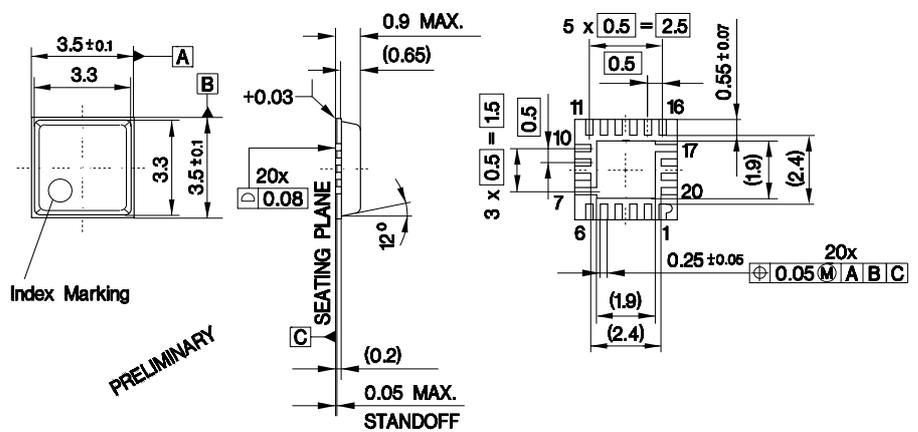
- Input frequency range 30 to 65 MHz
- Low intermodulation distortion
- 48 dB AGC range
- balanced 1 V_{pp} buffered output
- Input for gain-control voltage
- Output for tuner AGC with take-over point adjust
- Internal low noise reference voltage
- Full ESD protection

2.3 Application

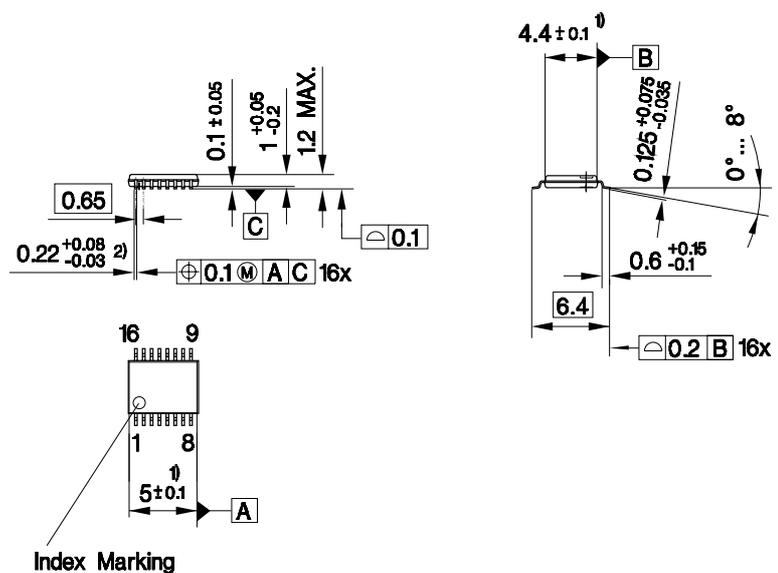
- IF amplifier in DVB-C, DVB-T, ATSC and ISDB-T frontends with direct IF- sampling.
 - IF amplifier in PAL or NTSC frontends
-

2.4 Package Outlines

P-VQFN-20



P-TSSOP-16-1



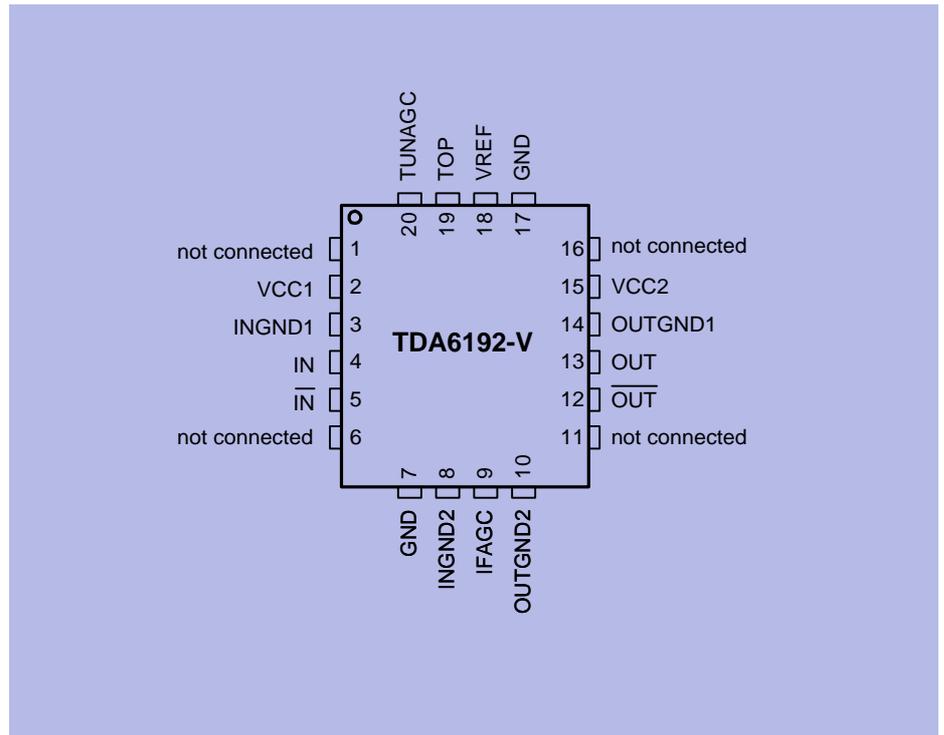
- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

3 Functional Description

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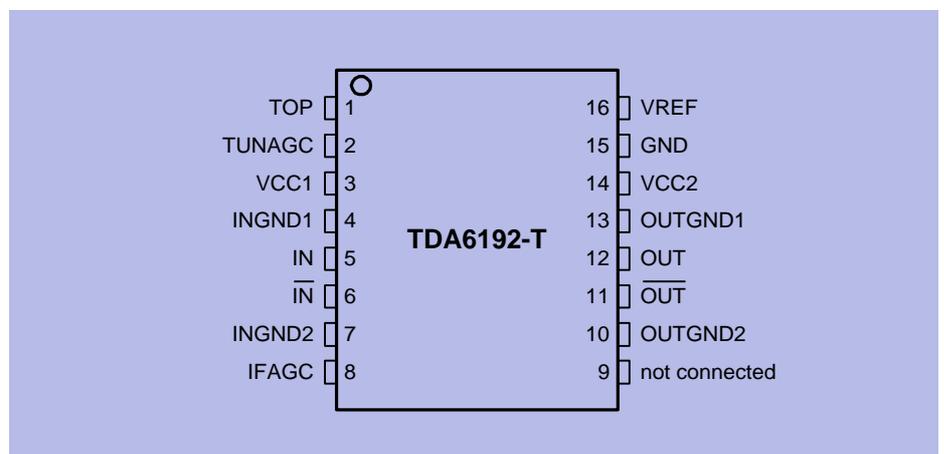
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3.1 Pin Configuration



Pin-configVQFN20

Figure 3-1 TDA6192-V, Pin Configuration

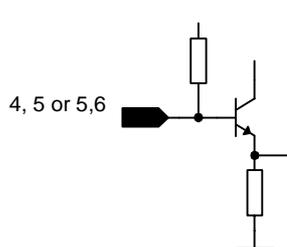
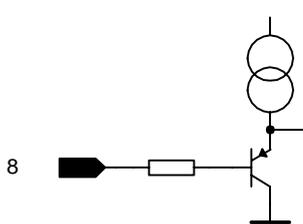


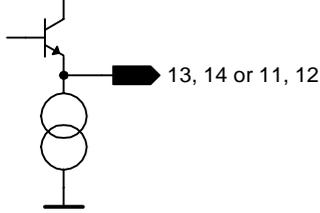
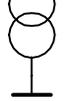
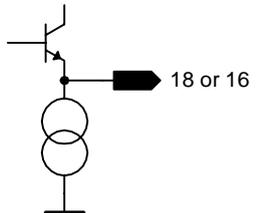
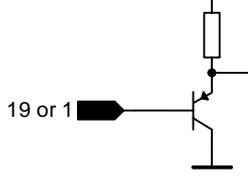
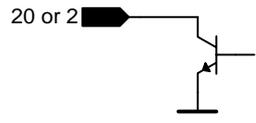
PinconfigT

Figure 3-2 TDA6192-T, Pin Configuration

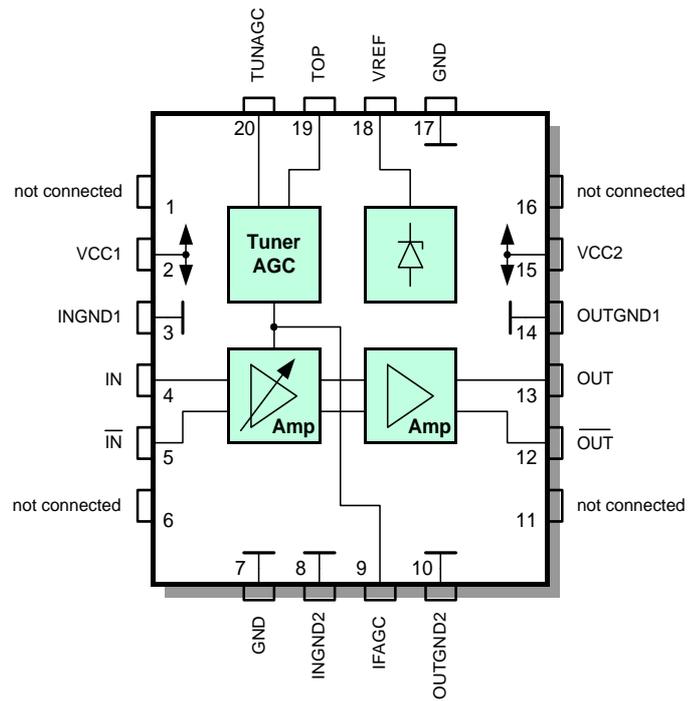
3.2 Internal Pin Configuration

Table 3-1 Pin Definition and Function

| Pin No. | | Symbol | Equivalent I/O-Schematic | Average DC voltage |
|------------|------------|------------------------|--|--------------------|
| TDA 6192-V | TDA 6192-T | | | |
| 1 | --- | not connected | not connected | n.a. |
| 2 | 3 | VCC1 | supply voltage | 5.0 V |
| 3 | 4 | INGND1 | ground | 0.0 V |
| 4 | 5 | IN |  | 3.6 V |
| 5 | 6 | $\overline{\text{IN}}$ | | 3.6 V |
| 6 | --- | not connected | not connected | n.a. |
| 7 | --- | GND | ground | 0.0 V |
| 8 | 7 | INGND2 | ground | 0.0 V |
| 9 | 8 | IFAGC |  | 0 to 1.8 V |
| --- | 9 | not connected | | |
| 10 | 10 | OUTGND2 | ground | 0.0 V |
| 11 | --- | not connected | not connected | n.a. |

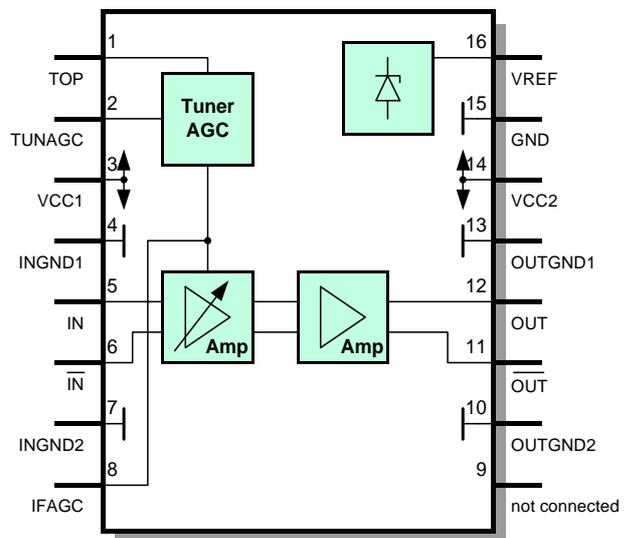
| Table3-2 Table3-4 | | Table 3-5 | | |
|---------------------|------------|-------------------------|--|--------------------|
| TDA 6192-V | TDA 6192-T | Symbol | Equivalent I/O-Schematic | Average DC voltage |
| 12 | 11 | $\overline{\text{OUT}}$ |  | 3.2 V |
| 13 | 12 | OUT |  | 3.2V |
| 14 | 13 | OUTGND1 | ground | 0.0 V |
| 15 | 14 | VCC2 | supply voltage | 5.0 V |
| 16 | --- | not connected | not connected | n.a. |
| 17 | 15 | GND | ground | 0.0 V |
| 18 | 16 | VREF |  | 3.6 V |
| 19 | 1 | TOP |  | 0.2 to 1.6 V |
| 20 | 2 | TUNAGC |  | 0.5 to 5 V |

3.3 Block Diagram



BlockdiagramVQFN20

Figure 3-3 TDA6192-V, Block Diagram



BlockdiagramT

Figure 3-4 TDA6192-T, Block Diagram

3.4 Circuit Description

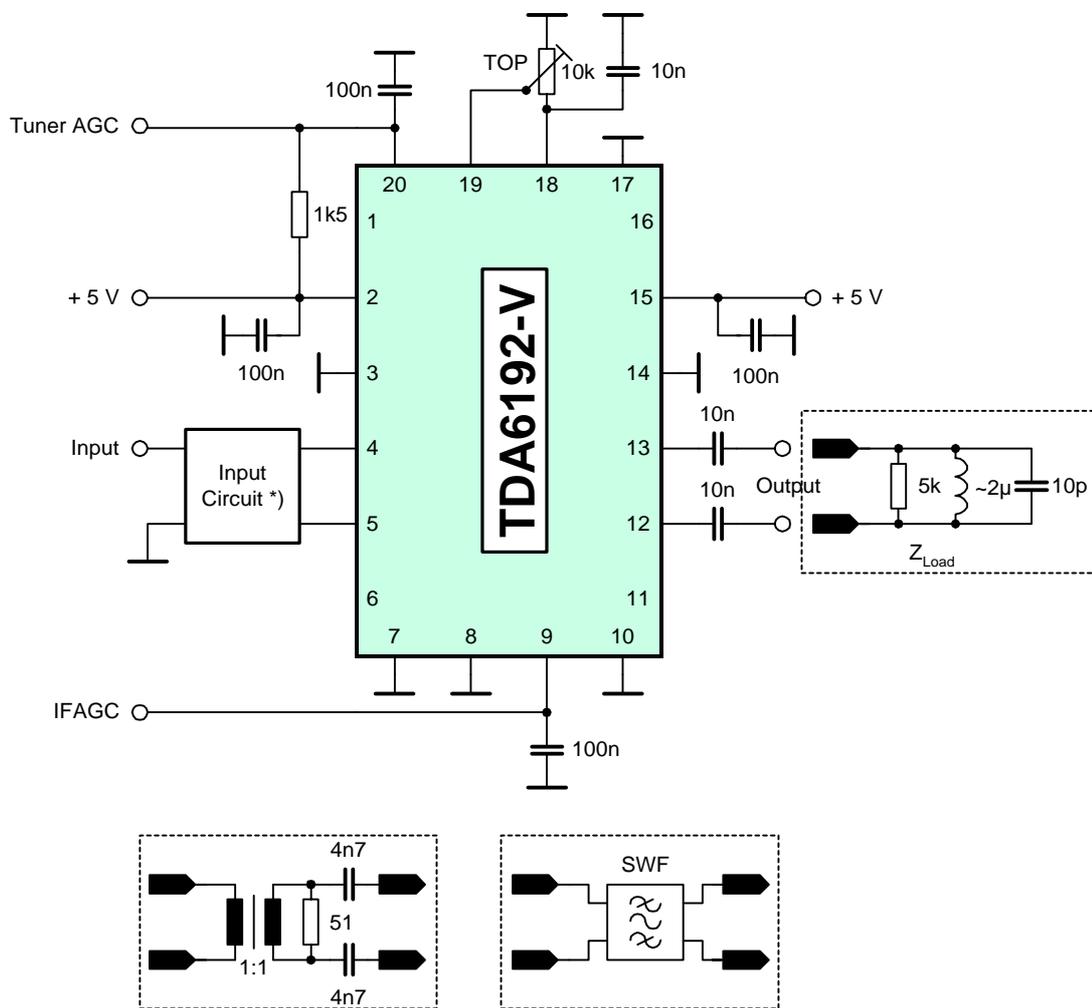
The **TDA6192** device combines an AGC amplifier, an output buffer to drive a following demodulator IC, a delayed tuner AGC with take-over point adjustment, and a low noise reference source VREF. The gain of the AGC amplifier is controlled by an external voltage. VREF is used as a reference for the take-over point adjustment of the tuner AGC voltage. TUNAGC is an open-collector output.

4 Applications

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4.1 TDA6192-V Evaluation board



*) Transformer or SWF

Figure 4-1 TDA6192-V Evaluation board, circuit diagram

4.2 TDA6192-T Evaluation board

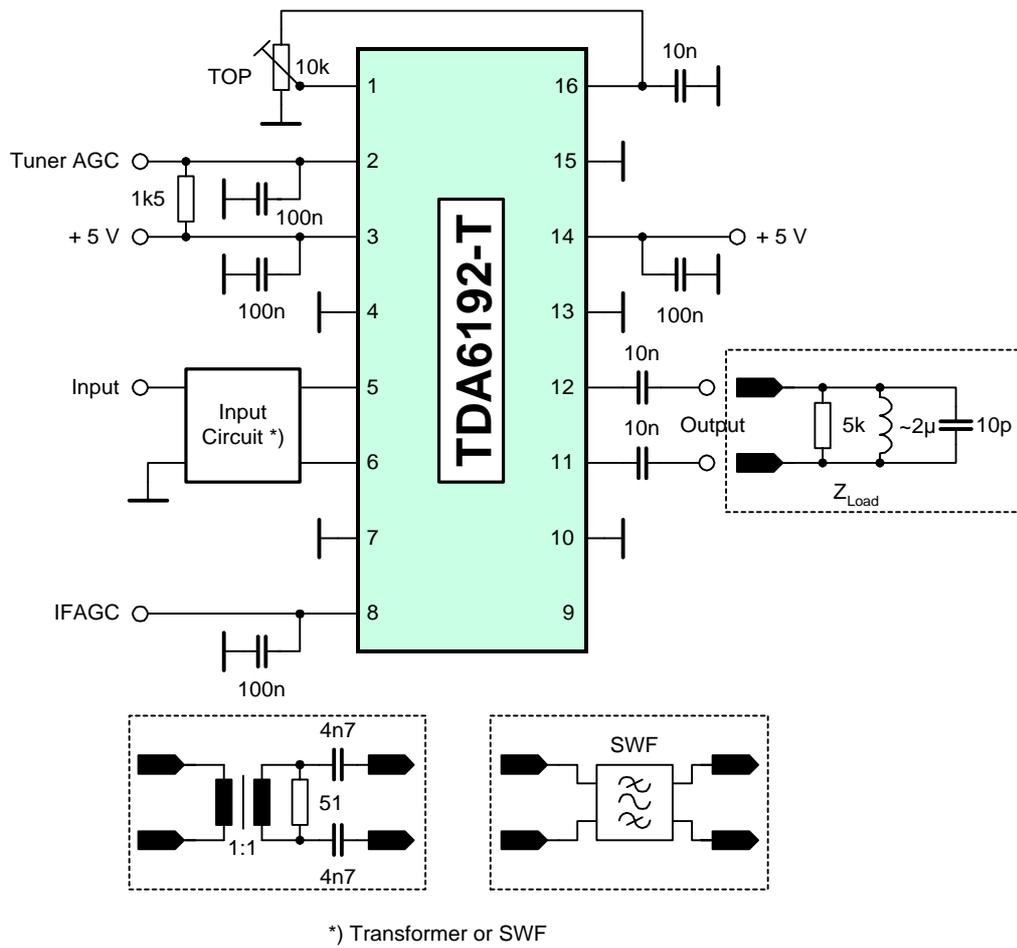


Figure 4-2 TDA6192-T Evaluation board, circuit diagram

5 Reference

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5.1 Electrical Data

5.1.1 Absolute Maximum Ratings



WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 5-1 Absolute Maximum Ratings

| Parameter ¹⁾ | Symbol | Limit Values | | Unit | Remarks |
|---|---------------------------|--------------|-----------|------|---------|
| | | min | max | | |
| Supply voltage | V_{CC1}, V_{CC2} | -0.3 | 6 | V | |
| Supply voltage difference | $\Delta V_{CC1}, V_{CC2}$ | -0.3 | +0.3 | V | |
| Ambient temperature TDA6192-V | T_{AMB} | -20 | +85 | °C | |
| Ambient temperature TDA6192-T | T_{AMB} | -20 | +70 | °C | |
| Junction temperature | T_J | | +125 | °C | |
| Storage temperature | T_S | -40 | +125 | °C | |
| Thermal resistance TDA6192-V (junction to ambient) | R_{thJA} | | 70 | K/W | |
| Thermal resistance TDA6192-T (junction to ambient) | R_{thJA} | | 230 | K/W | |
| IF input | $V_{IF/\bar{IF}}$ | -0.3 | 4 | V | |
| IF output | $I_{OUT/\bar{OUT}}$ | -5 | 1 | mA | |
| AGC input | V_{IFAGV} | -0.3 | V_{CC1} | V | |
| Tuner AGC take-over point adjust | V_{TOP} | -0.3 | V_{CC1} | V | |
| Tuner AGC output | V_{TUNAGC} | -0.3 | 6 | V | |
| ESD-Protection ²⁾ | | | | | |
| all pins | V_{ESD} | -2 | +2 | kV | HBM |

1).All values are referred to ground (pin), unless stated otherwise.

Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.

2).According to EIA/JESD22-A114-B (HBM incircuit test), as a single device incircuit contact discharge test.

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

Table 5-2 Operating Range

| Parameter | Symbol | Limit Values | | Unit | Test Conditions | Item |
|-------------------------------|--------------------------|--------------|------|------|-----------------|------|
| | | min | max | | | |
| Supply voltage | V_{CC1} , V_{CC2} | 4.5 | 5.5 | V | | |
| Frequency range | f | 30 | 65 | MHz | | |
| Ambient temperature TDA6192-V | T_{AMB} | - 20 | + 85 | °C | | |
| Ambient temperature TDA6192-T | T_{AMB} | - 20 | + 70 | °C | | |

5.1.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 5-3 AC/DC Characteristics with $T_{AMB} = 25\text{ °C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$

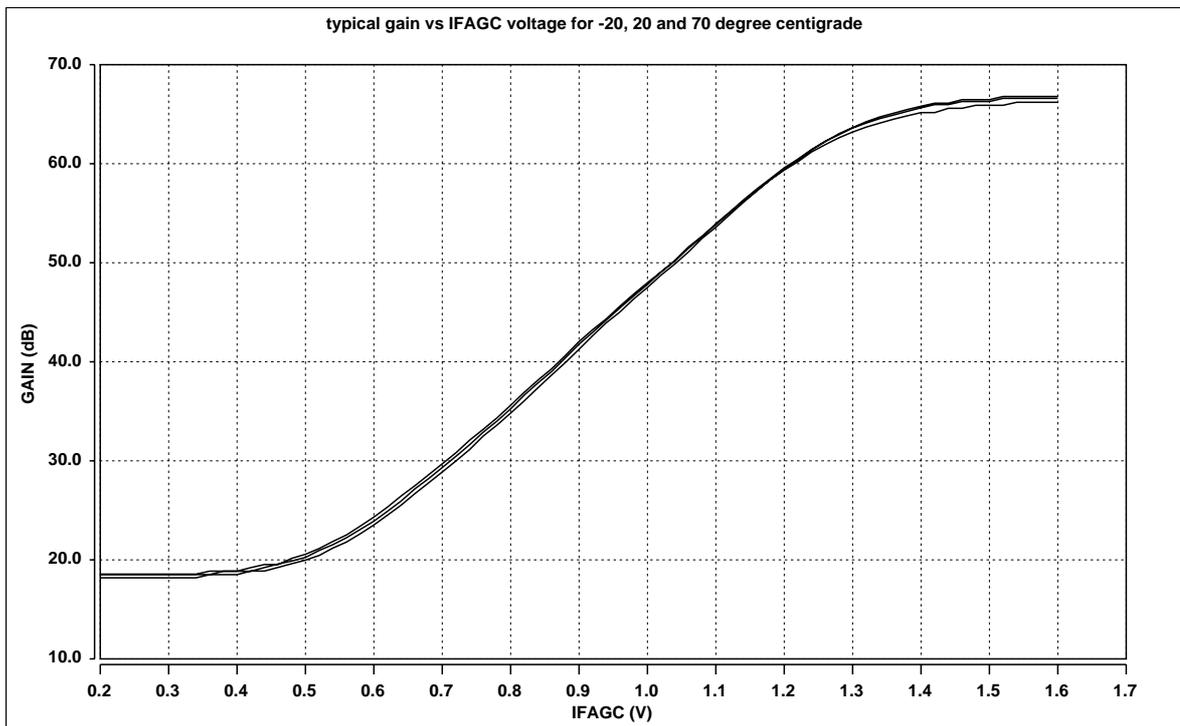
| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|---|----------------------|--------------|-----------|----------|---------------|---|---|------|
| | | min | typ | max | | | | |
| Power supply, reference voltage | | | | | | | | |
| Current consumption | I_{CC1} | | 18 | 22 | mA | max. gain | | |
| Current consumption | I_{CC1} | | 10 | 12 | mA | min. gain | | |
| Current consumption | I_{CC2} | | 9 | | mA | | | |
| Reference voltage | V_{REF} | 3.3 | 3.6 | 3.9 | V | | | |
| VREF line regulation | $\Delta V_{REFLINE}$ | | | 30 | mV | $V_{CC1} = V_{CC2} = 4.5\text{ to }5.5\text{ V}$ | | |
| VREF load regulation | $\Delta V_{REFLOAD}$ | | | 30 | mV | $I_{VREF} = -0.5\text{ to }0.5\text{ mA}$ | | |
| VREF vs temperature | $\Delta V_{REFTEMP}$ | -30 | 10 | 30 | mV | $T_{AMB} = -20\text{ to }70\text{ °C}$ | | |
| AGC amplifier, tuner AGC | | | | | | | | |
| Static characteristics | | | | | | | | |
| IF input voltage | $V_{IF/IF}$ | | V_{REF} | | | | | |
| Take-over point voltage | V_{TOP} | 0 | | 2 | V | Tuner AGC is enabled | | |
| | V_{TOP} | 3.0 | | V_{CC} | V | Tuner AGC is disabled | | |
| Take-over point disable threshold | | 2.0 | 2.3 | 3.0 | V | | | |
| Take-over point current | I_{TOP} | -1 | | 1 | μA | $V_{TOP} = 0\text{ V}$ | | |
| Tuner AGC current | I_{TUNAGC} | 2.5 | 3.5 | 5 | mA | $V_{TUNAGC} = 0.5\text{ V}$, $V_{IFAGC} = 1.0\text{ V}$, $V_{TOP} = 1.5\text{ V}$ | | |
| Tuner AGC current | I_{TUNAGC} | 0 | | 10 | μA | $V_{TUNAGC} = 6\text{ V}$, $V_{IFAGC} = 1.0\text{ V}$, $V_{TOP} = 0.5\text{ V}$ | | |
| Dynamic characteristics | | | | | | | | |
| Voltage gain, see 5.2.1 Gain vs. IF AGC voltage on page 6 | G_{max} | 63 | 67 | 71 | dB | $V_{IFAGC} \geq 1.6\text{ V}$ | | |
| | G_{min} | | 19 | | dB | $V_{IFAGC} \leq 0.2\text{ V}$ | | |

Table 5-4 AC/DC Characteristics with $T_{AMB} = 25\text{ °C}$, $V_{CC1} = V_{CC2} = 5\text{ V}$ (continued)

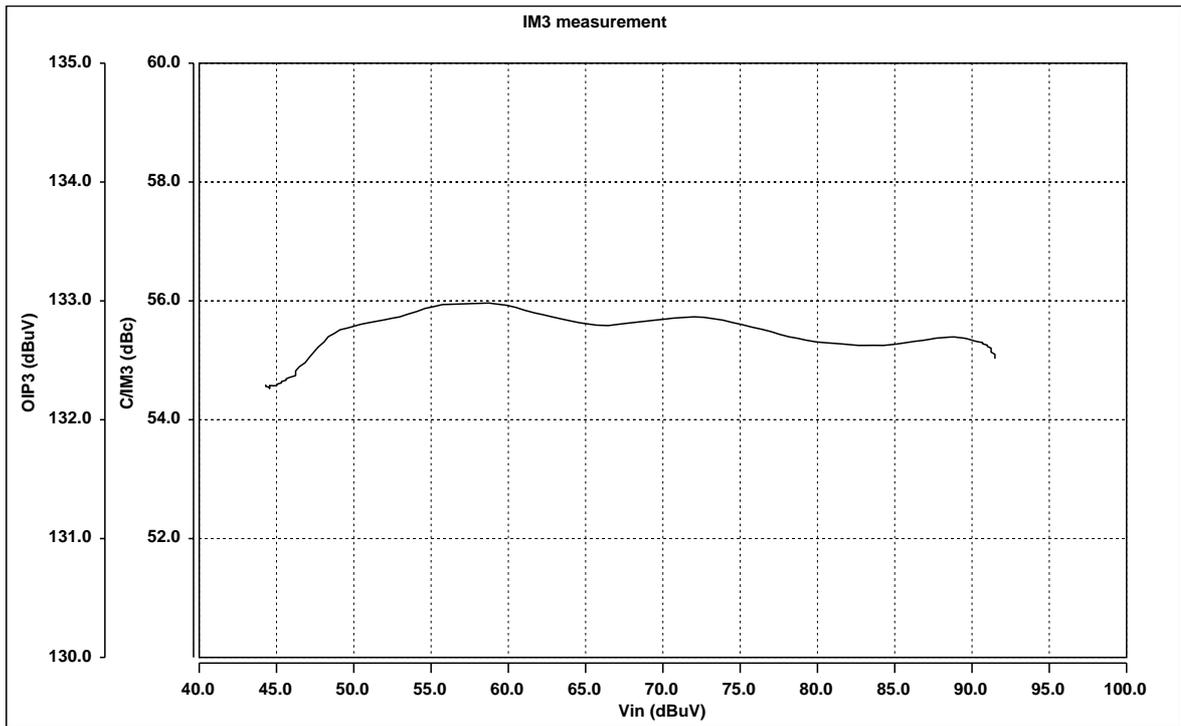
| | Symbol | Limit Values | | | Unit | Test Conditions | L | Item |
|--|--|--------------|-----|-----|------------|---|---|------|
| | | min | typ | max | | | | |
| Maximum IF input level | $V_{IF/IF}$ | 88 | 92 | 96 | dB μ V | min. gain, $f_{IF/IF} = 36\text{ MHz}$ (sine), $V_{IFAGC} = 0.2\text{ V}$, $V_{OUT/OUT} = 1\text{ V}_{pp}$ | | |
| Minimum IF input level | $V_{IF/IF}$ | | 44 | | | max. gain, $f_{IF/IF} = 36\text{ MHz}$ (sine), $V_{IFAGC} = 1.6\text{ V}$, $V_{OUT/OUT} = 1\text{ V}_{pp}$ | | |
| Input impedance | $R_{IF/IF}$ | 1.5 | 2 | 2.5 | k Ω | $f_{IF/IF} = 36\text{ MHz}$, parallel equivalent circuit | | |
| | $C_{IF/IF}$ | | 1.5 | | pF | | | |
| Tuner AGC max. slope | $\Delta I_{TUNAGC} / \Delta V_{IFAGC}$ | 25 | 36 | 50 | mA/V | $V_{IFAGC} = 0.9\text{ to }1.1\text{ V}$, $V_{TOP} = 1.0\text{ V}$, $V_{TUNAGC} = 0.5\text{ V}$ | | |
| Low end cutoff frequency (-1 dB) | f_L | | | 25 | MHz | $V_{IF/IF} = 60\text{ dB}\mu\text{V}$, $R_{LOAD} \geq 5\text{ k}\Omega$, | | |
| High end cutoff frequency (-1 dB) | f_H | 65 | | | MHz | $C_{LOAD} \leq 1.5\text{ pF}$, $V_{OUT/OUT} = 1\text{ V}_{pp}$ at $f_{IF/IF} = 36\text{ MHz}$ (sine) | | |
| Intermodulation, see 5.2.2 Intermodulation and output IP3 vs. input voltage on page 7 | C/IM3 | 50 | 56 | | dBc | $f_{IF/IF1} = 37\text{ MHz}$, $f_{IF/IF2} = 38\text{ MHz}$, $V_{IF/IF1} = 60\text{ dB}\mu\text{V}$, $V_{IF/IF2} = 60\text{ dB}\mu\text{V}$, $R_{LOAD} \geq 5\text{ k}\Omega$, $C_{LOAD} \leq 10\text{ pF}$, $L_{LOAD} \sim 2\text{ }\mu\text{H}$, $V_{OUT/OUT} = 1\text{ V}_{pp}$ | | |
| Third order output intercept point, see 5.2.2 Intermodulation and output IP3 vs. input voltage on page 7 | OIP3 | | 133 | | dB μ V | $f_{IF/IF1} = 37\text{ MHz}$, $f_{IF/IF2} = 38\text{ MHz}$, $V_{IF/IF1} = 60\text{ dB}\mu\text{V}$, $V_{IF/IF2} = 60\text{ dB}\mu\text{V}$, $R_{LOAD} \geq 5\text{ k}\Omega$, $C_{LOAD} \leq 10\text{ pF}$, $L_{LOAD} \sim 2\text{ }\mu\text{H}$, $V_{OUT/OUT} = 1\text{ V}_{pp}$ | | |
| Signal to noise ratio, see 5.2.3 Signal to noise ratio vs. input voltage on page 8 | SNR | 35 | 43 | | dB | $f_{IF/IF} = 36\text{ MHz}$ (sine), $V_{IF/IF} = 60\text{ dB}\mu\text{V}$, $V_{OUT/OUT} = 1\text{ V}_{pp}$, BW = 8 MHz | | |
| Noise figure | | | 10 | 12 | dB | max. gain, see 5.3.1 on page 9 | | |
| Output impedance | $R_{IF/IF}$ | | 60 | 100 | Ω | $f_{OUT/OUT} = 36\text{ MHz}$, series equivalent circuit | | |
| | $L_{IF/IF}$ | | 33 | | nH | | | |

5.2 Electrical Diagrams

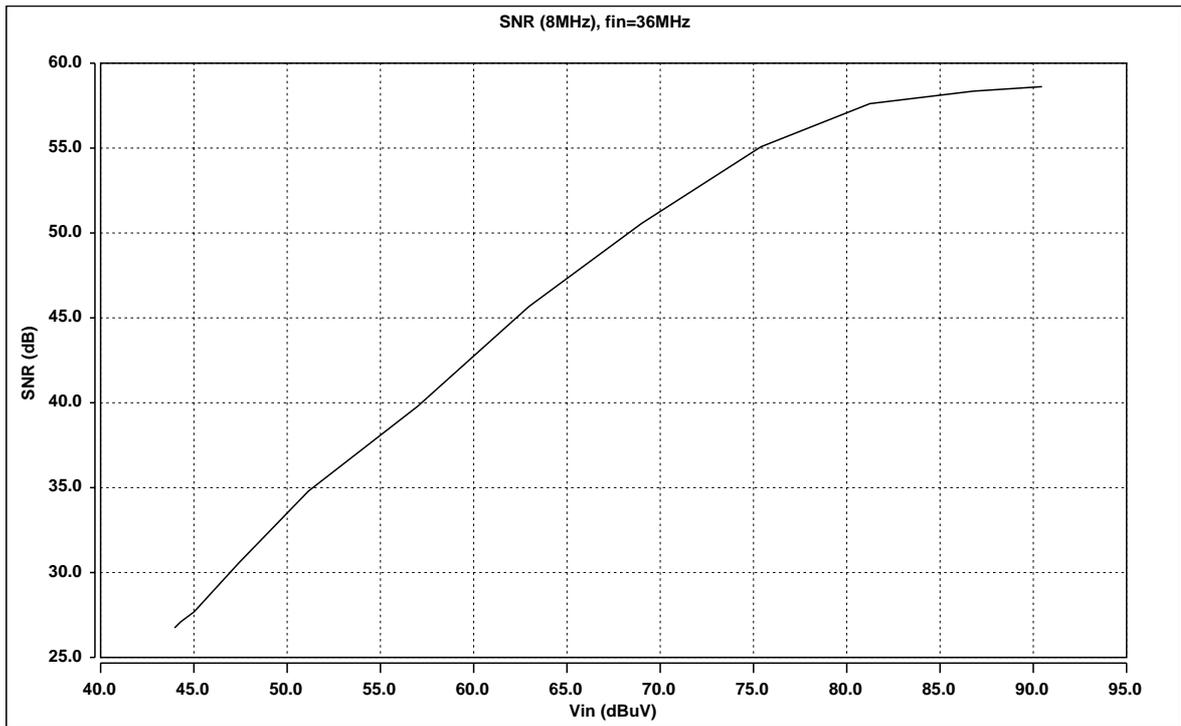
5.2.1 Gain vs. IF AGC voltage



5.2.2 Intermodulation and output IP3 vs. input voltage



5.2.3 Signal to noise ratio vs. input voltage



5.3 Measurement Circuit

5.3.1 Noise Measurement

