



New Product

DG3001/3002/3003

Vishay Siliconix

# Low-Voltage Sub-Ohm SPST/SPDT MICRO FOOT® Analog Switch

## FEATURES

- MICRO FOOT Chip Scale Package (1.0 x 1.5 mm)
- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance -  $r_{DS(on)}$ : 0.4  $\Omega$
- Fast Switching -  $t_{ON}$ : 47 ns,  $t_{OFF}$ : 40 ns
- Low Power Consumption
- TTL/CMOS Compatible

## BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

## APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- PCM Cards
- PDA

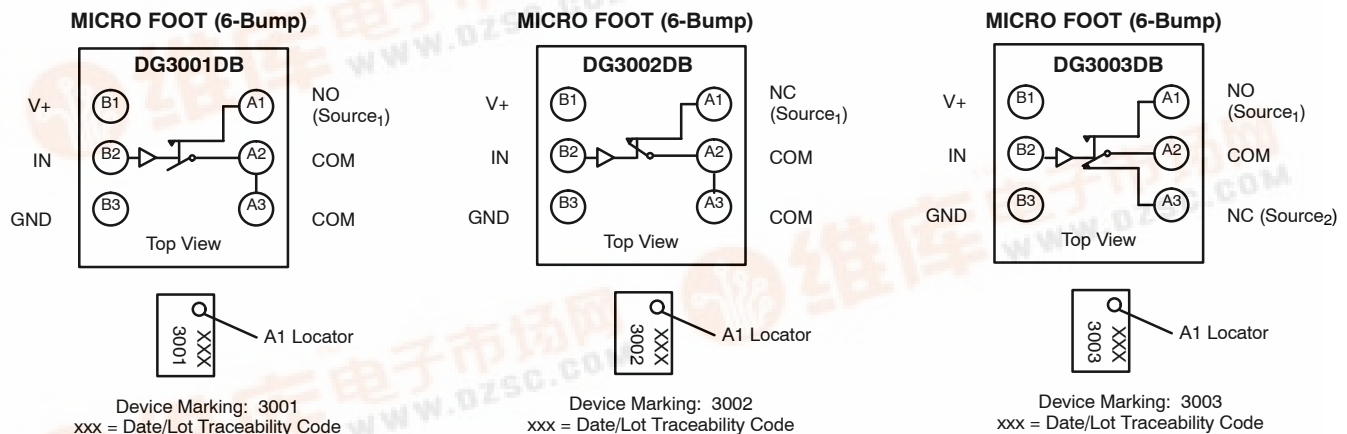
## DESCRIPTION

The DG3001/DG3002/DG3003 are monolithic CMOS analog switches designed for high performance switching of analog signals. The DG3001 and DG3002 are configured as SPST switches, and the DG3003 is an SPDT switch. Combining low power, high speed ( $t_{ON}$ : 47 ns,  $t_{OFF}$ : 40 ns), low on-resistance ( $r_{DS(on)}$ : 0.4  $\Omega$ ) and small physical size (MICRO FOOT, 6-bump), the DG3001/DG3002/DG3003 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG3001/DG3002/DG3003 are built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



## TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

## ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	MICRO FOOT: 6-Bump (3 × 2, 0.5-mm pitch, 165-μm nom. bump height)	DG3001DB
		DG3002DB
		DG3003DB

# DG3001/3002/3003

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## ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +6 V
IN, COM, NC, NO <sup>a</sup>	-0.3 to (V+ + 0.3 V)
Continuous Current (NO, NC, COM)	±250 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	±400 mA
Storage Temperature (D Suffix)	-65 to 150°C

Package Reflow Conditions<sup>b</sup>

VPR	215°C
IR/Convection	220°C

Power Dissipation (Packages)<sup>c</sup>

6-Bump, 2 x 3 MICRO FOOT <sup>d</sup>	250 mW
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Notes:

- a Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b Refer to IPC/JEDEC (J-STD-020A)
- c All bumps soldered to PC Board.
- d Derate 3.1 mW/°C above 70°C

SPECIFICATIONS (V+ = 3.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, VIN = 0.4 or 2.0 V <sup>e</sup>	Temp <sup>a</sup>	Limits −40 to 85° C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
Analog Switch							
Analog Signal Range <sup>d</sup>	V <sub>NO</sub> , V <sub>NC</sub> , V <sub>COM</sub>		Full	0		V+	V
On-Resistance <sup>d</sup>	r <sub>ON</sub>	V+ = 2.7 V, V <sub>COM</sub> = 1.5 V, I <sub>NO</sub> , I <sub>NC</sub> = 10 mA	Room Full		0.4	0.7 0.8	Ω
r <sub>ON</sub> Flatness <sup>d</sup>	r <sub>ON</sub> Flatness	V+ = 2.7 V, V <sub>COM</sub> = 0 to V+, I <sub>NO</sub> , I <sub>NC</sub> = 10 mA	Room		0.1	0.2	
r <sub>ON</sub> Match <sup>d</sup>	Δr <sub>ON</sub>		Room		0.01	0.05	
Switch Off Leakage Current <sup>f</sup>	I <sub>NO(off)</sub> , I <sub>NC(off)</sub>	V+ = 3.3 V V <sub>NO</sub> , V <sub>NC</sub> = 0.3 V/3 V, V <sub>COM</sub> = 3 V/0.3 V	Room Full	1 −10		1 10	nA
	I <sub>COM(off)</sub>		Room Full	1 −10		1 10	
Channel-On Leakage Current <sup>f</sup>	I <sub>COM(on)</sub>	V+ = 3.3 V, V <sub>NO</sub> , V <sub>NC</sub> = V <sub>COM</sub> = 0.3 V/3 V	Room Full	1 −10		1 10	
Digital Control							
Input High Voltage	V <sub>INH</sub>		Full	2			V
Input Low Voltage	V <sub>INL</sub>		Full			0.4	
Input Capacitance <sup>d</sup>	C <sub>in</sub>		Full		5		pF
Input Current <sup>d</sup>	I <sub>INL</sub> or I <sub>INH</sub>	V <sub>IN</sub> = 0 or V+	Full	−1		1	μA
Dynamic Characteristics							
Turn-On Time <sup>d</sup>	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 2.0 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF Figure 1 and 2	Room Full		47	71	ns
Turn-Off Time <sup>d</sup>	t <sub>OFF</sub>		Room Full		40	59	
Break-Before-Make Time <sup>d</sup>	t <sub>d</sub>		Room	1	6		
Charge Injection <sup>d</sup>	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω, Figure 3	Room		64		pC
Off-Isolation <sup>d</sup>	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz	Room		−70		dB
Crosstalk <sup>d</sup>	X <sub>TALK</sub>		Room		−70		
NO, NC Off Capacitance <sup>d</sup>	C <sub>NO(off)</sub> , C <sub>NC(off)</sub>	V <sub>IN</sub> = 0 or V+, f = 1 MHz	Room		100		pF
Channel-On Capacitance <sup>d</sup>	C <sub>ON</sub>		Room		340		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current <sup>d</sup>	I+	V <sub>IN</sub> = 0 or V+			0.1	1.0	μA

Notes:

- a Room = 25°C, Full = as determined by the operating suffix.
- b The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c Typical values are for design aid only, not guaranteed nor subject to production testing.
- d Guarantee by design, not subjected to production test.
- e VIN = input voltage to perform proper function.

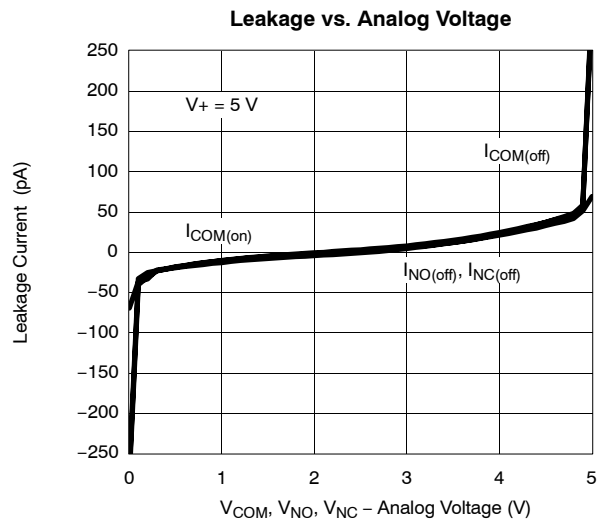
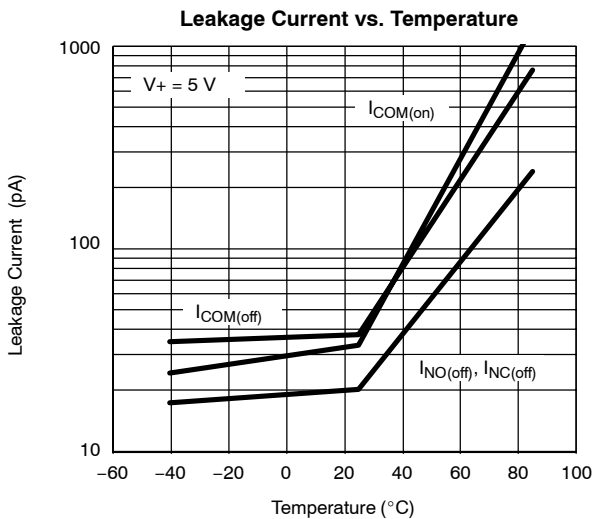
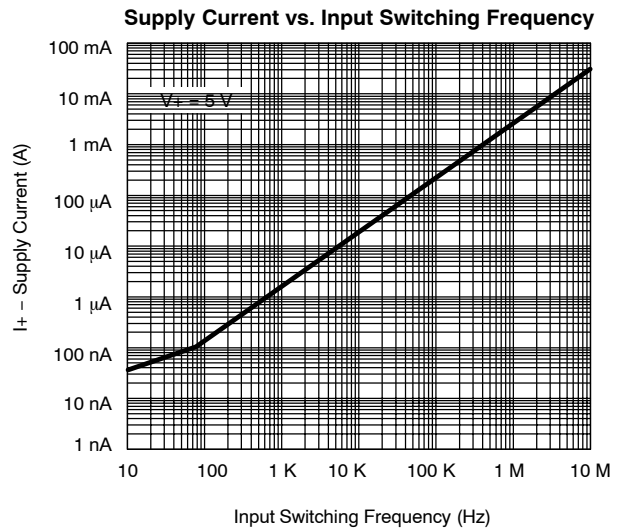
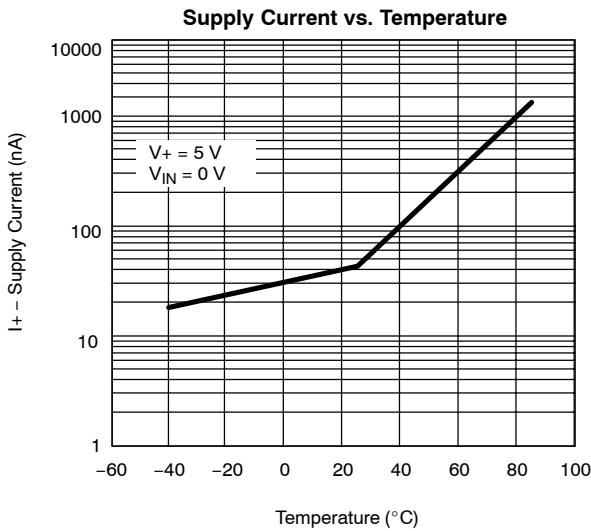
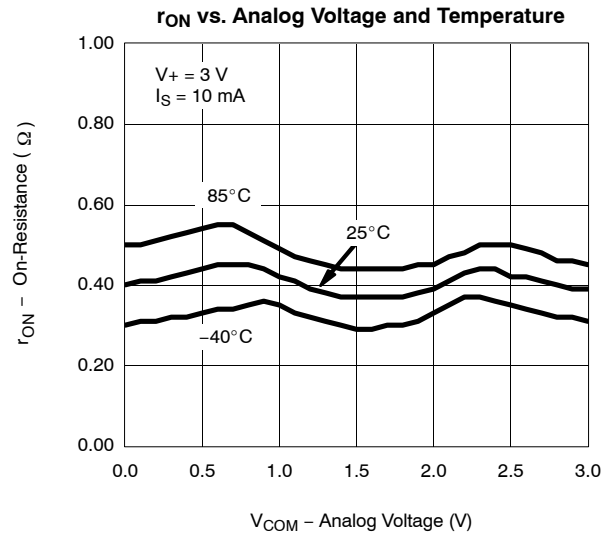
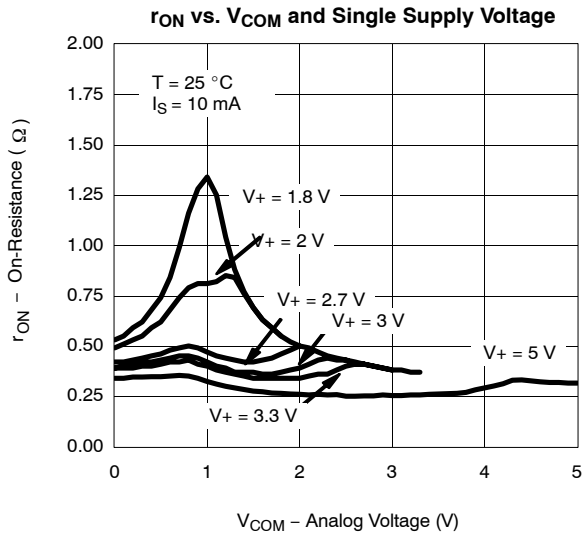


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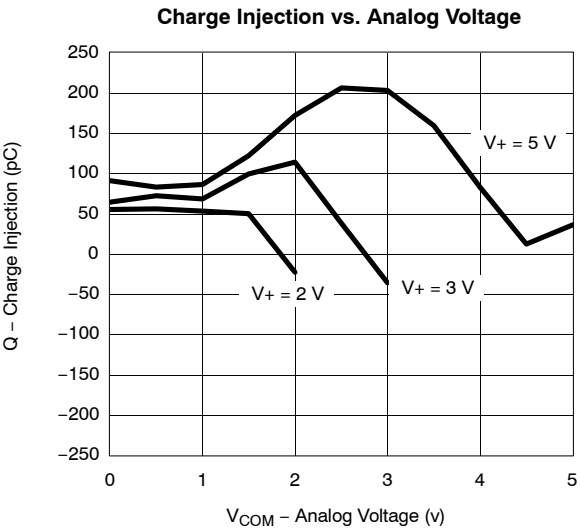
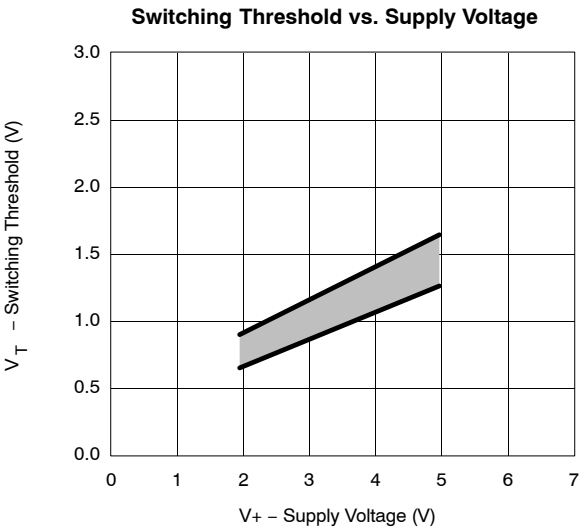
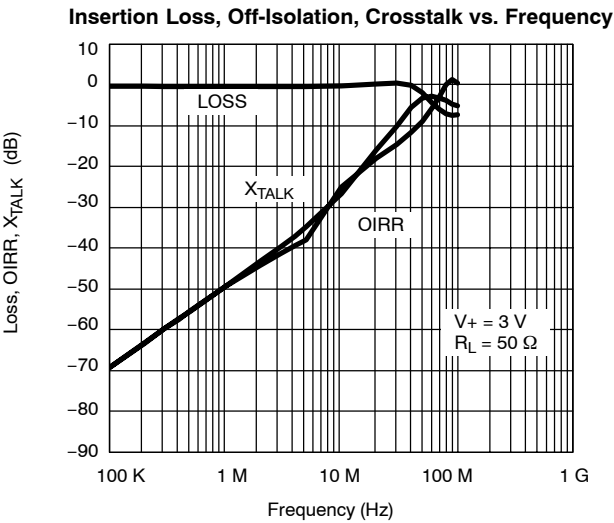
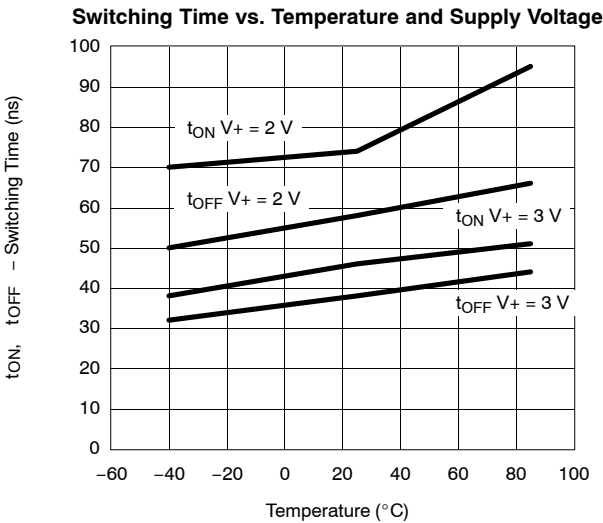
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**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



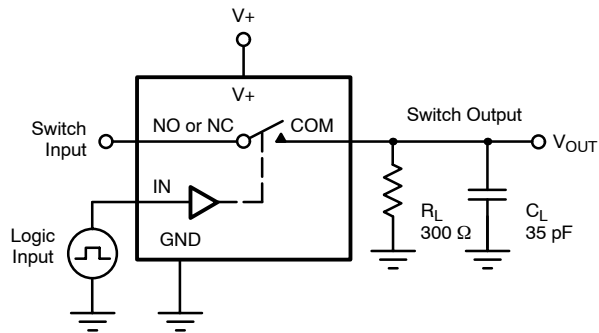


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



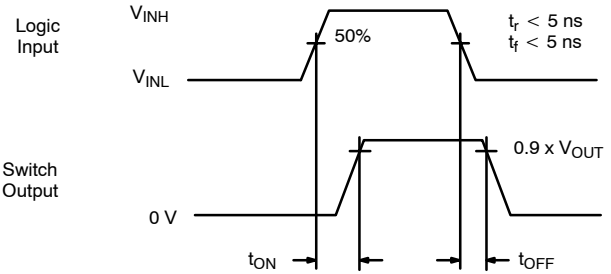


TEST CIRCUITS



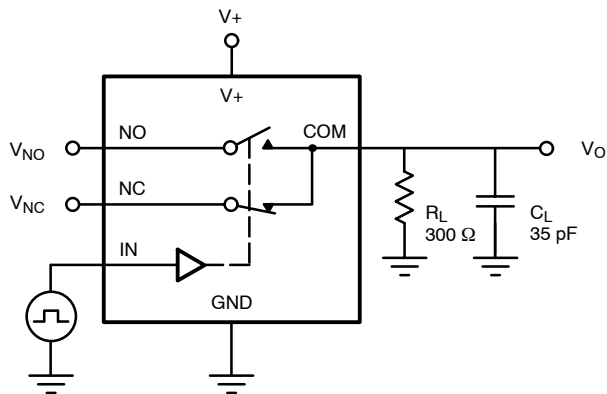
$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



$C_L$  (includes fixture and stray capacitance)

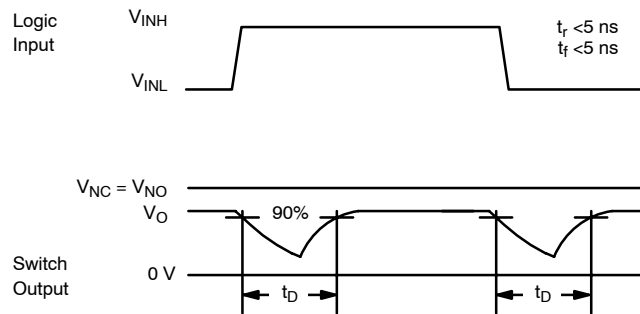
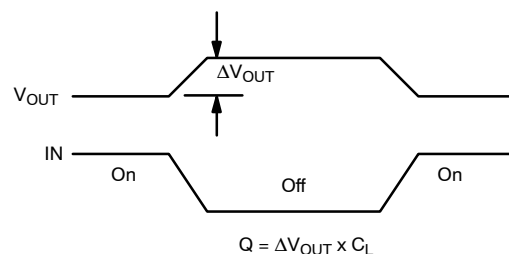
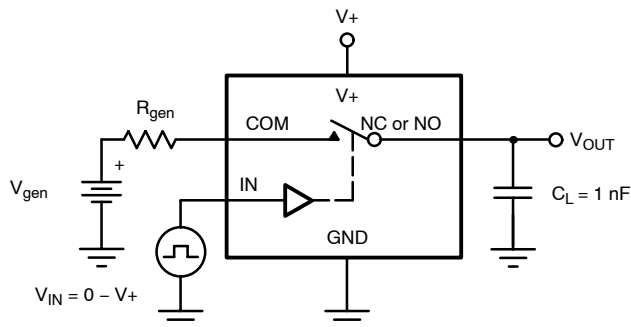


FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection



TEST CIRCUITS

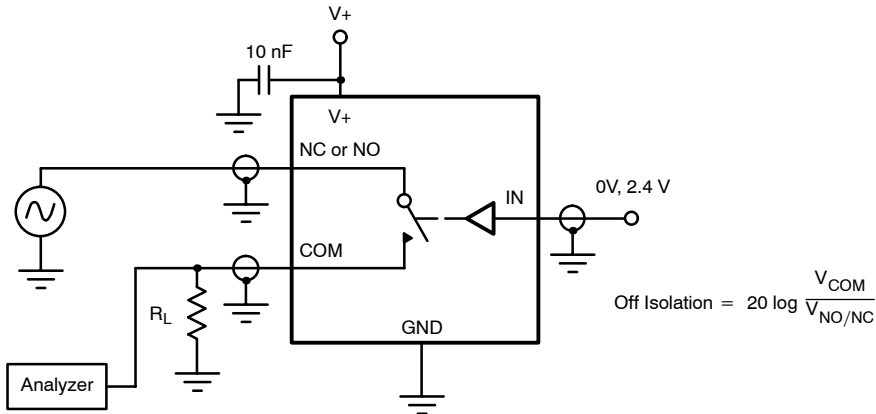


FIGURE 4. Off-Isolation

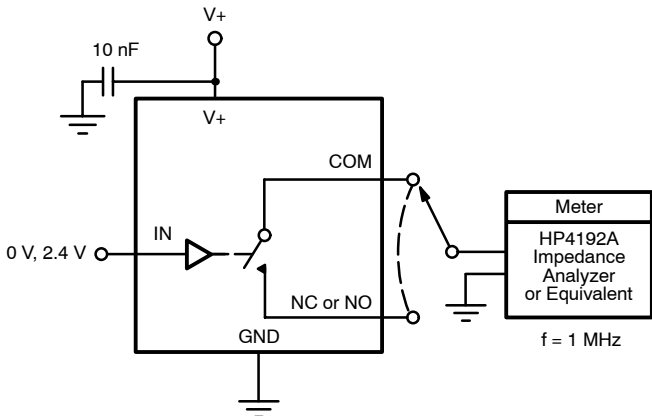


FIGURE 5. Channel Off/On Capacitance



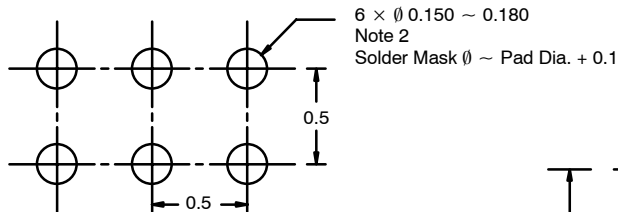
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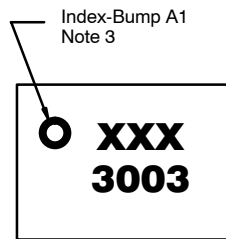
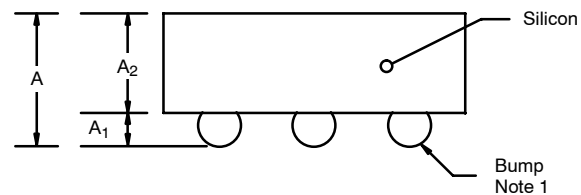
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## PACKAGE OUTLINE

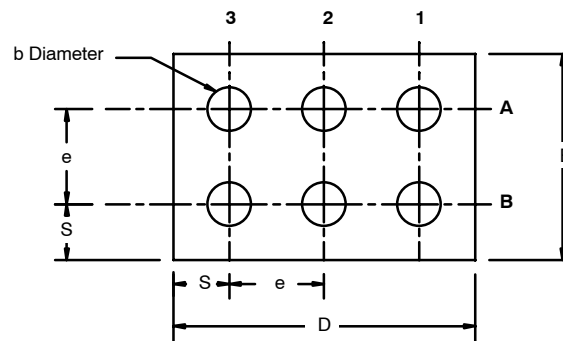
### MICRO FOOT: 6-BUMP (3 X 2, 0.5-mm PITCH, 165- $\mu$ m BUMP HEIGHT)



Recommended Land Pattern



Top Side (Die Back)



NOTES (Unless Otherwise Specified):

1. Bump is Eutectic 63/57 Sn/Pb.
2. Non-solder mask defined copper landing pad.
3. Laser Mark on silicon die back; no coating. Shown is not actual marking; sample only.

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.610	0.685	0.0240	0.0270
A <sub>1</sub>	0.140	0.190	0.0055	0.0075
A <sub>2</sub>	0.470	0.495	0.0185	0.0195
b	0.180	0.250	0.0071	0.0098
D	1.490	1.515	0.0587	0.0596
E	0.990	1.015	0.0390	0.0400
e	0.5 BASIC		0.0197 BASIC	
S	0.245	0.258	0.0096	0.0101

\* Use millimeters as the primary measurement.