

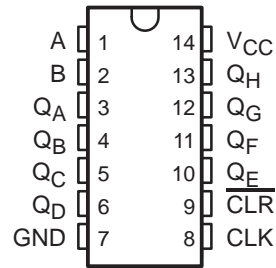
SN74ALS164A

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SDAS159D – APRIL 1982 – REVISED DECEMBER 1994

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs

D OR N PACKAGE
(TOP VIEW)



description

This 8-bit parallel-out serial shift register features AND-gated serial (A and B) inputs and an asynchronous clear ($\overline{\text{CLR}}$) input. The gated serial inputs permit control over incoming data because a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided that the minimum setup-time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input. All inputs are diode clamped to minimize transmission-line effects.

The SN74ALS164A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS† | | |
|-------------------------|-----|---|---|----------|-----------|-----|
| $\overline{\text{CLR}}$ | CLK | A | B | QA | QB ... QH | |
| L | X | X | X | L | L | L |
| H | L | X | X | QA0 | QB0 | QH0 |
| H | ↑ | H | H | H | QAn | QGn |
| H | ↑ | L | X | L | QAn | QGn |
| H | ↑ | X | L | L | QAn | QGn |

† QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

H = high level (steady state), L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

QAn, QGn = the level of QA or QG before the most recent

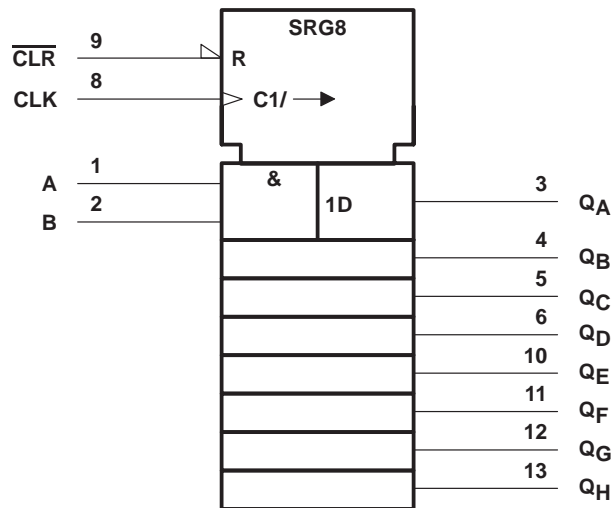
↑ transition of the clock; indicates a 1-bit shift.

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8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

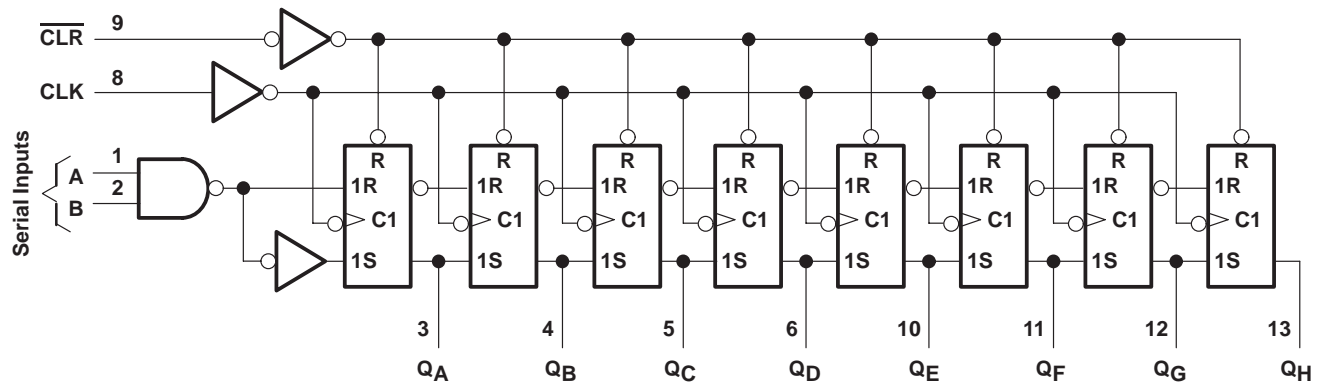
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

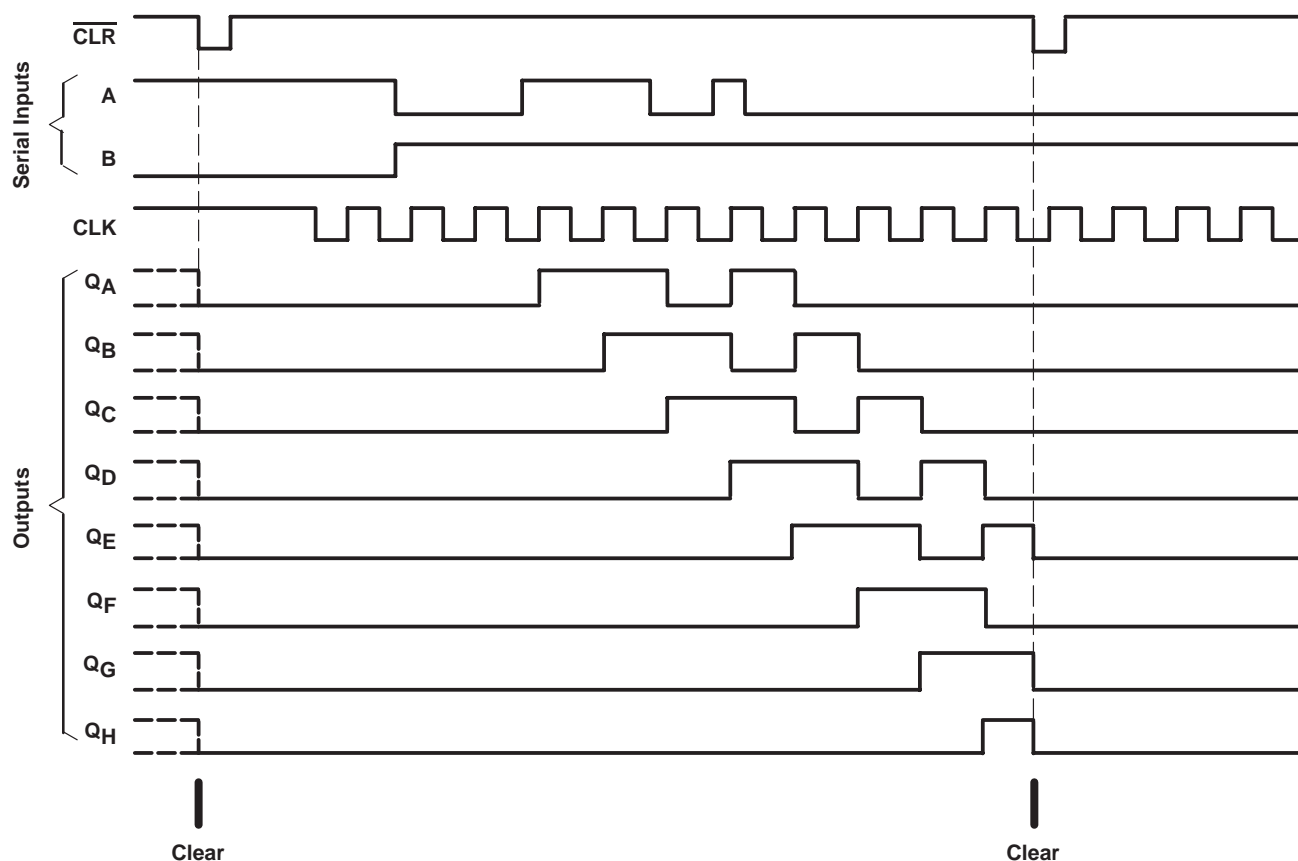


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typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

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recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-------------|--------------------------------|--------------|-----|------|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | –0.4 | mA |
| I_{OL} | Low-level output current | | | 8 | mA |
| f_{clock} | Clock frequency | | | 50 | MHz |
| t_w | Pulse duration | CLK | 10 | | ns |
| | | CLR low | 16 | | |
| t_{su} | Setup time before CLK↑ | Data | 6 | | ns |
| | | CLR inactive | 8 | | |
| t_h | Hold time, data after CLK↑ | 2 | | | ns |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--------------------|--|------------------------|------|------|------|
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | –1.5 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 4\text{ mA}$ | 0.25 | 0.4 | V |
| | | $I_{OL} = 8\text{ mA}$ | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$ | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | –0.1 | mA |
| I_{O}^{\ddagger} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | –30 | | –112 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$, See Note 1 | | 14 | 24 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: With 4.5 V applied to the serial input and all other inputs, except the CLK, grounded, I_{CC} is measured after a clock transition from 0 to 4.5 V.

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}^{\S}$ | | | UNIT |
|-----------|--------------|-------------|---|------|-----|------|
| | | | MIN | TYP† | MAX | |
| f_{max} | | | 50 | 75 | | MHz |
| t_{PHL} | CLR | Any Q | 6 | 15 | 20 | ns |
| t_{PLH} | CLK | Any Q | 4 | 9 | 16 | ns |
| t_{PHL} | | | 5 | 11 | 17 | |

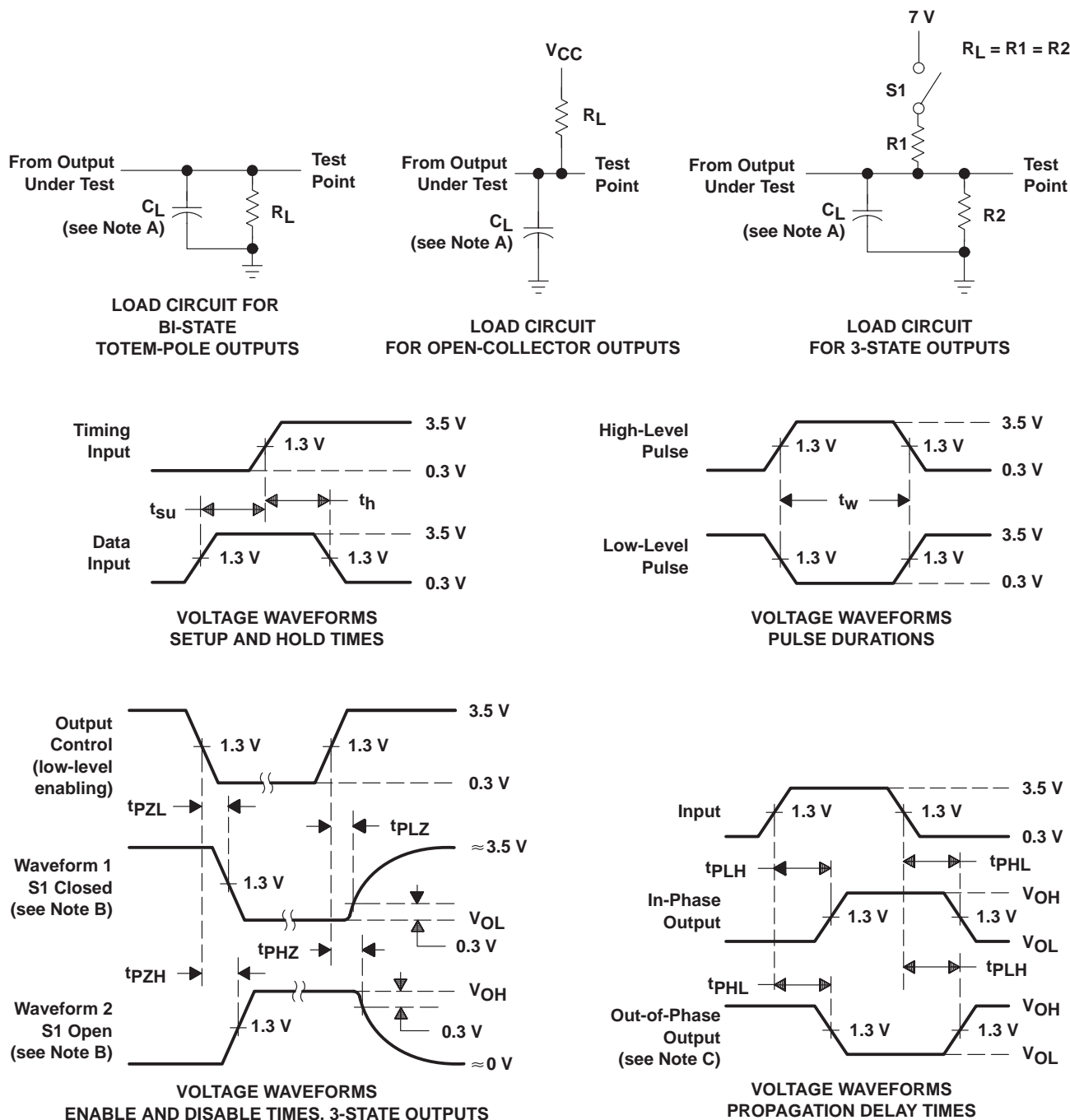
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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