19-2464; Rev 0; 4/02

MAXIM

16-Bit ADCs, 150ksps, 3.3V Single Supply

General Description

The MAX1134/MAX1135 are 150ksps, 16-bit ADCs. These serially interfaced ADCs connect directly to SPI™, QSPI™, and MICROWIRE™ devices without external logic. They combine an input scaling network, internal track/hold (T/H), clock, and three general-purpose digital output pins (for external multiplexer or PGA control) in a 20-pin SSOP package. The excellent dynamic performance (THD ≥ 90dB), high speed (150ksps in bipolar mode), and low power (8.0mA) of these ADCs make them ideal for applications such as industrial process control, instrumentation, and medical applications.

The MAX1134 accepts input signals of 0 to +6V (unipolar) or ±6V (bipolar), while the MAX1135 accepts input signals of 0 to +2.048V (unipolar) or ±2.048V (bipolar). Operating from a single 3.135V to 3.465V analog and digital supply, power-down modes reduce current consumption to 0.15mA at 10ksps and further reduce supply current to less than 20µA at slower data rates.

A serial strobe output (SSTRB) allows direct connection to the TMS320 family digital-signal processors. The MAX1134/MAX1135 user can select either the internal clock or an external serial-interface clock for the ADC to perform analog-to-digital conversions.

The MAX1134/MAX1135 feature internal calibration circuitry to correct linearity and offset errors. On-demand calibration allows the user to optimize performance. Three user-programmable logic outputs are provided for the control of an 8-channel mux or PGA.

The MAX1134/MAX1135 are available in a 20-pin SSOP package and are fully specified over the -40°C to +85°C temperature range.

Applications

Industrial Process Control

Industrial I/O Modules

Data-Acquisition Systems

Medical Instruments

Portable and Battery-Powered Equipment

Functional Diagram and Typical Application Circuit appear at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor, Corp.

Features

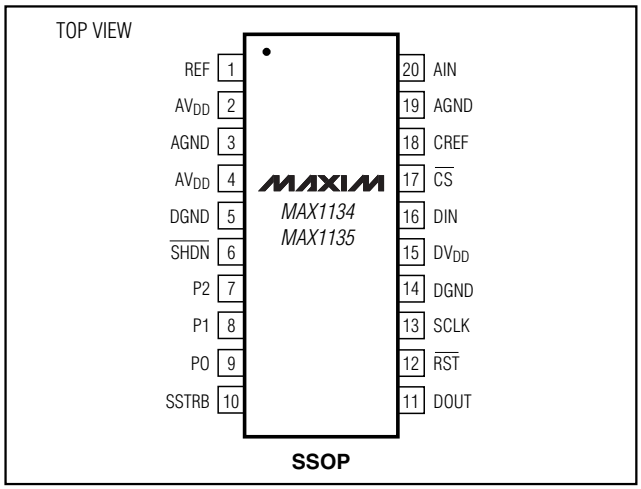
- **150ksps (Bipolar) and 125ksps (Unipolar) Sampling ADC**
- **16 Bits, No Missing Codes**
- **1LSB INL (typ) Guaranteed**
- **-100dB THD**
- **3.3V Single-Supply Operation**
- **Low-Power Operation**
  4.5mA (typ) (Unipolar Mode)
- **1.2µA Shutdown Mode**
- **Software-Configurable Unipolar and Bipolar Input Ranges**
  0 to +6V and ±6V (MAX1134)
  0 to +2.048V and ±2.048V (MAX1135)
- **Internal or External Clock**
- **SPI/QSPI/MICROWIRE TMS320-Compatible Serial Interface**
- **Three User-Programmable Logic Outputs**
- **Small 20-Pin SSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1134BCAP	0°C to +70°C	20 SSOP	±2.5
MAX1134BEAP	-40°C to +85°C	20 SSOP	±2.5

Ordering Information continued at end of data sheet.

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND, DV_{DD} to DGND .....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
AIN to AGND .....±16.5V
CREF, REF to AGND.....-0.3V to (AV_{DD} + 0.3V)
Digital Inputs to DGND.....-0.3V to +6V
Digital Outputs to DGND .....-0.3V to (DV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX113_ _CAP.....0°C to +70°C
MAX113_ _EAP.....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = 3.3V ±5%, f_{SCLK} = 3.6MHz, external clock (50% duty cycle), 24 clocks/conversion (150ksps), bipolar input, V_{REF} = 2.048V, C_{REF} = 4.7µF, C_{CREF} = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				16			Bits
Relative Accuracy	INL	Bipolar mode (Note 2)	MAX113_B		1.0	±2.5	LSB
No Missing Codes				16			Bits
Differential Nonlinearity	DNL	Bipolar mode	MAX113_B	-1		+1.75	LSB
Transition Noise					1.5		LSB_{RMS}
Offset Error		Unipolar				±4	mV
		Bipolar				±6	
Gain Error (Note 3)		Unipolar				±0.2	%FSR
		Bipolar				±0.3	
Offset Drift (Bipolar and Unipolar)		Excluding reference drift			±1		ppm/°C
Gain Drift (Bipolar and Unipolar)		Excluding reference drift			±4		ppm/°C
DYNAMIC SPECIFICATIONS (5kHz SINE-WAVE INPUT, 150ksps, 3.6MHz CLOCK, BIPOLAR INPUT MODE. MAX1134, 12V_{P-P}. MAX1135, 4.096V_{P-P}.)							
Signal-to-Noise Plus Distortion (SINAD)		f_{IN} = 5kHz		80	84		dB
		f_{IN} = 75kHz			83		
Signal-to-Noise Ratio (SNR)		f_{IN} = 5kHz		80	84		dB
		f_{IN} = 75kHz			83		
Total Harmonic Distortion (THD)		f_{IN} = 5kHz			-100	-90	dB
		f_{IN} = 75kHz			-93		
Spurious-Free Dynamic Range (SFDR)		f_{IN} = 5kHz		92	105		dB
		f_{IN} = 75kHz			97		
ANALOG INPUT							
Input Range		MAX1134	Unipolar	0		+6	V
			Bipolar	-6		+6	
		MAX1135	Unipolar	0		+2.048	
			Bipolar	-2.048		+2.048	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = 3.3V ±5%, f_{SCLK} = 3.6MHz, external clock (50% duty cycle), 24 clocks/conversion (150ksps), bipolar input, V_{REF} = 2.048V, C_{REF} = 4.7µF, C_{CREF} = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Impedance		MAX1134	Unipolar	7.5	10.5		kΩ
			Bipolar	5.9	8.4		
		MAX1135	Unipolar	100	1000		
			Bipolar	3.4	5.3		
Input Capacitance					32		pF
CONVERSION RATE							
Internal Clock Frequency					3		MHz
Aperture Delay	t_{AD}				10		ns
Aperture Jitter	t_{AJ}				50		ps
MODE 1 (24 EXTERNAL CLOCK CYCLES PER CONVERSION)							
External Clock Frequency	f_{SCLK}	Unipolar		0.1		3.0	MHz
		Bipolar		0.1		3.6	
Sample Rate	f_S = f_{SCLK} / 24	Unipolar		4.17		125	ksps
		Bipolar		4.17		150	
Conversion Time (Note 4)	$t_{CONV+ACQ}$ = 24 / f_{SCLK}	Unipolar		8		240	µs
		Bipolar		6.7		240	
MODE 2 (INTERNAL CLOCK MODE)							
External Clock Frequency (Data Transfer Only)						4	MHz
Conversion Time		(SSTRB low pulse width)			5.3	7	µs
Acquisition Time (Note 5)		Unipolar		1.67			µs
		Bipolar		1.39			
MODE 3 (32 EXTERNAL CLOCK CYCLES PER CONVERSION)							
External Clock Frequency	f_{SCLK}	Unipolar or bipolar		0.1		3.6	MHz
Sample Rate	f_S = f_{SCLK} / 32	Unipolar or bipolar		3.125		112	ksps
Conversion Time (Note 4)	$t_{CONV+ACQ}$ = 32 / f_{SCLK}	Unipolar or bipolar		8.89		320	µs
EXTERNAL REFERENCE							
Input Range		(Notes 6, 7)		1.9	2.048	2.2	V
Input Current		V_{REF} = 2.048V, f_{SCLK} = 3.6MHz			110		µA
		V_{REF} = 2.048V, f_{SCLK} = 0			100		
		In power-down, f_{SCLK} = 0			0.1		
DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage	I_{IN}	V_{IN} = 0 or DV_{DD}		-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = 3.3V ±5%, f_{SCLK} = 3.6MHz, external clock (50% duty cycle), 24 clocks/conversion (150ksps), bipolar input, V_{REF} = 2.048V, C_{REF} = 4.7µF, C_{CREF} = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis	V_{HYST}			0.2		V
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	DV_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Three-State Leakage Current	I_L	$\overline{CS}$ = DV_{DD}	-10		+10	µA
Three-State Output Capacitance		$\overline{CS}$ = DV_{DD}		10		pF
POWER SUPPLIES						
Analog Supply	AV_{DD}		3.135	3.3	3.465	V
Digital Supply	DV_{DD}		3.135	3.3	3.465	V
Analog Supply Current	I_{ANALOG}	Unipolar mode		3.9	8	mA
		Bipolar mode		7	11	
		$\overline{SHDN}$ = 0, or software power-down mode		0.1	10	µA
Digital Supply Current	$I_{DIGITAL}$	Unipolar or bipolar mode		1	2	mA
		$\overline{SHDN}$ = 0, or software power-down mode		1.1	10	µA
Power-Supply Rejection Ratio (Note 8)	PSRR	AV_{DD} = DV_{DD} = 3.135V to 3.465V		65		dB

TIMING CHARACTERISTICS (Figures 5 and 6)

(AV_{DD} = DV_{DD} = 3.3V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN to SCLK Setup	t_{DS}		50			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK to DOUT Valid	t_{DO}				70	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{LOAD} = 50pF			80	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{LOAD} = 50pF			80	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK High Pulse Width	t_{CH}		120			ns
SCLK Low Pulse Width	t_{CL}		120			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 50pF			80	ns
$\overline{CS}$ Fall to SSTRB Enable	t_{SDV}	C_{LOAD} = 50pF, external clock mode			80	ns
$\overline{CS}$ Rise to SSTRB Disable	t_{STR}	C_{LOAD} = 50pF, external clock mode			80	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode	0			ns
$\overline{RST}$ Pulse Width	t_{RS}		278	70		ns

TIMING CHARACTERISTICS (Figures 5 and 6) (continued)

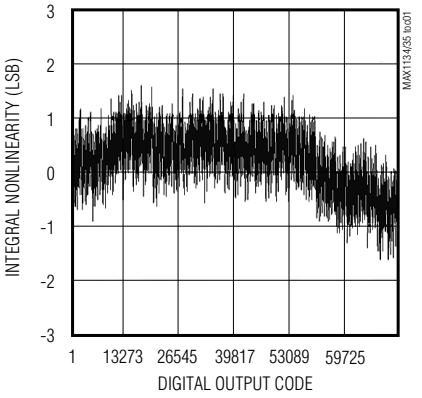
(AV_{DD} = DV_{DD} = 3.3V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Note 1: Tested at AV_{DD} = DV_{DD} = 3.3V, bipolar input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and offset error have been nullified.
Note 3: Offset nullified.
Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle. Includes the acquisition time.
Note 5: Acquisition time is 5 clock cycles in short acquisition mode and 13 clock cycles in long acquisition mode.
Note 6: Performance is limited by the converter's noise floor, typically 300μV_{P-P}.
Note 7: When an external reference has a different voltage than the specified typical value, the full scale of the ADC scales proportionally.
Note 8: Defined as the change in positive full scale caused by a ±5% variation in the nominal supply voltage.

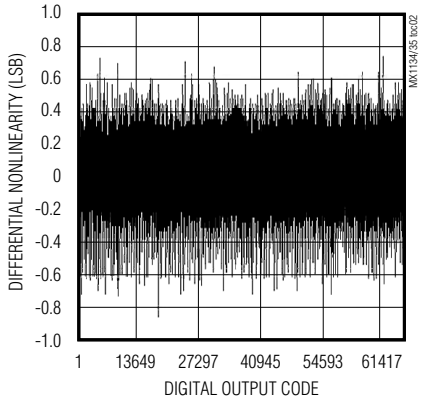
Typical Operating Characteristics

(MAX1134/MAX1135, AV_{DD} = DV_{DD} = 3.3V, f_{SCLK} = 3.6MHz, external clock (50% duty cycle), 24 clocks/conversion (150ksps), bipolar input, REF = 2.048V, 4.7µF on REF, 1µF on CREF, T_A = +25°C, unless otherwise noted.)

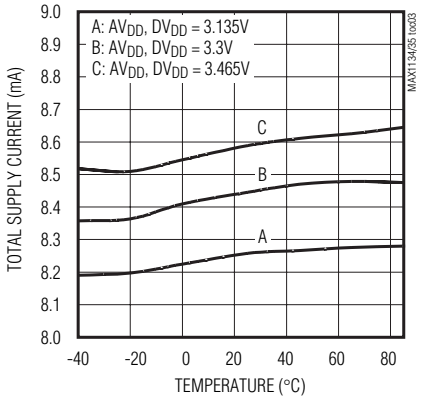
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



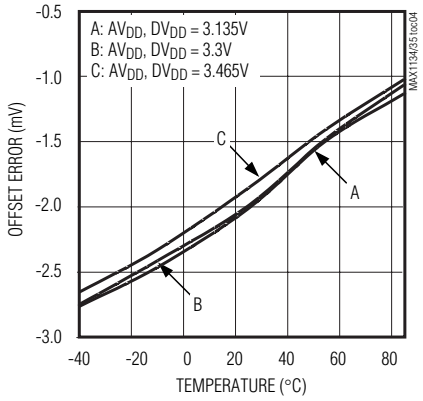
TOTAL SUPPLY CURRENT vs. TEMPERATURE



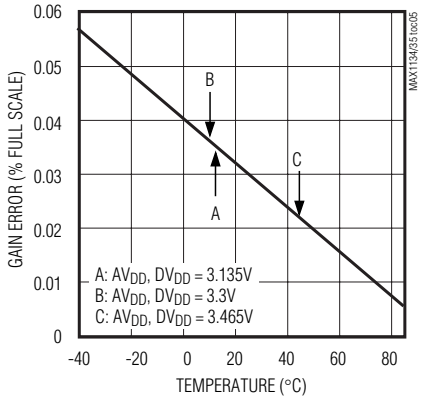
Typical Operating Characteristics (continued)

(MAX1134/MAX1135, AV_{DD} = DV_{DD} = 3.3V, f_{SCLK} = 3.6MHz, external clock (50% duty cycle), 24 clocks/conversion (150ksps), bipolar input, REF = 2.048V, 4.7µF on REF, 1µF on CREF, T_A = +25°C, unless otherwise noted.)

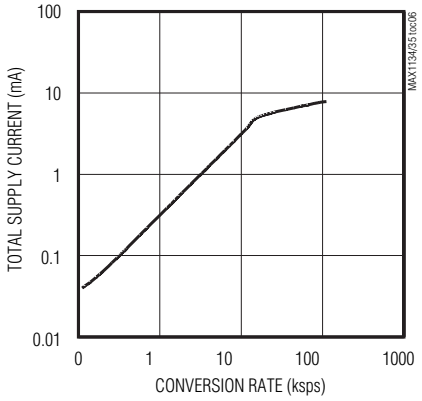
OFFSET VOLTAGE vs. TEMPERATURE



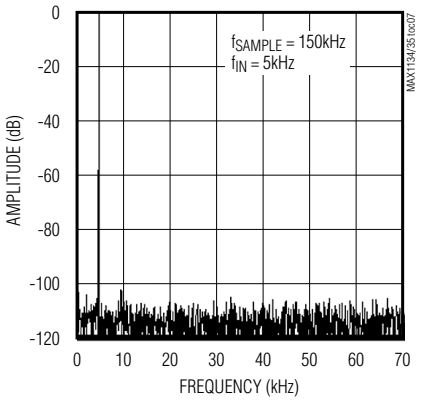
GAIN ERROR vs. TEMPERATURE



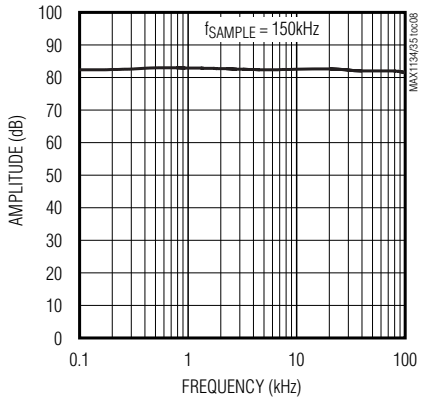
TOTAL SUPPLY CURRENT vs. CONVERSION RATE (USING SHUTDOWN)



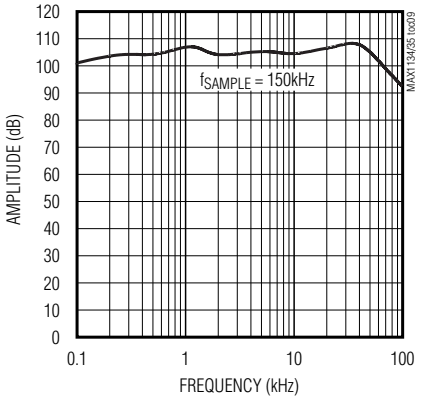
FFT PLOT



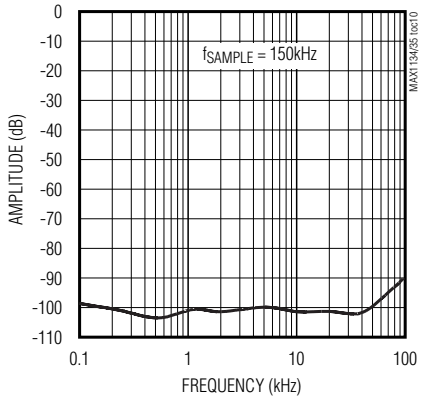
SINAD PLOT



SFDR PLOT



THD PLOT



Pin Description

PIN	NAME	FUNCTION
1	REF	ADC Reference Input. Connect a 2.048V voltage source to REF. Bypass REF to AGND with a 4.7µF capacitor.
2	AV_{DD}	Analog Supply. Connect to pin 4.
3	AGND	Analog Ground. This is the primary analog ground (star ground).
4	AV_{DD}	Analog Supply, 3.3V ±5%. Bypass AV_{DD} to AGND (pin 3) with a 0.1µF capacitor.
5	DGND	Digital Ground
6	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to put the ADC in shutdown mode.
7	P2	User-Programmable Output 2
8	P1	User-Programmable Output 1
9	P0	User-Programmable Output 0
10	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the ADC begins a conversion and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. It is high impedance when $\overline{CS}$ is high in external clock mode.
11	DOUT	Serial Data Output. MSB first, straight binary format for unipolar input, two's complement for bipolar input. Each bit is clocked out of DOUT at the falling edge of SCLK.
12	$\overline{RST}$	Reset Input. Drive $\overline{RST}$ low to put the device in the power-on default mode. See the *Power-On Reset* section.
13	SCLK	Serial Data Clock Input. Serial data on DIN is loaded on the rising edge of SCLK, and serial data is updated on DOUT on the falling edge of SCLK. In external clock mode, SCLK sets the conversion speed.
14	DGND	Digital Ground. Connect to pin 5.
15	DV_{DD}	Digital Supply, 3.3V ±5%. Bypass DV_{DD} to DGND (pin 14) with a 0.1µF capacitor.
16	DIN	Serial Data Input. Serial data on DIN is latched on the rising edge of SCLK.
17	$\overline{CS}$	Chip-Select Input. Drive $\overline{CS}$ low to enable the serial interface. When $\overline{CS}$ is high, DOUT is high impedance. In external clock mode, SSTRB is high impedance when $\overline{CS}$ is high.
18	CREF	Reference Buffer Bypass. Bypass CREF to AGND (pin 3) with a 1µF capacitor.
19	AGND	Analog Ground. Connect to pin 3.
20	AIN	Analog Input

Detailed Description

The MAX1134/MAX1135 ADCs use a successive-approximation technique and input track/hold (T/H) circuitry to convert an analog signal to a 16-bit digital output. The MAX1134/MAX1135 easily interface to microprocessors (µPs). The data bits can be read either during the conversion in external clock mode or after the conversion in internal clock mode.

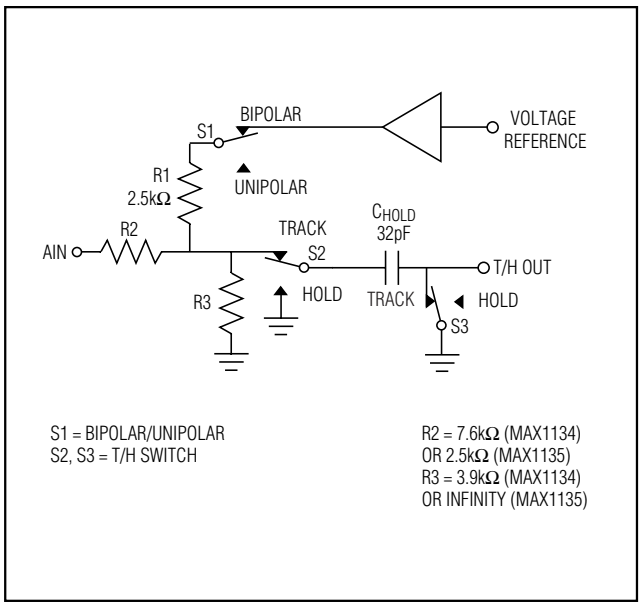


Figure 1. Equivalent Input Circuit

In addition to a 16-bit ADC, the MAX1134/MAX1135 include an input scaler, an internal digital microcontroller, calibration circuitry, and an internal clock generator.

The input scaler for the MAX1134 enables conversion of input signals ranging from 0 to +6V (unipolar input) or ±6V (bipolar input). The MAX1135 accepts 0 to +2.048V (unipolar input) or ±2.048V (bipolar input). The input range is software selectable.

Calibration

To minimize linearity, offset, and gain errors, the MAX1134/MAX1135 have on-demand software calibration. Initiate calibration by writing a control byte with bit M1 = 0 and bit M0 = 1 (Table 1). Select internal or external clock for calibration by setting the INT/$\overline{EXT}$ bit in the control byte. Calibrate the MAX1134/MAX1135 with the same clock mode used for performing conversions.

Offsets resulting from synchronous noise (such as the conversion clock) are canceled by the MAX1134/MAX1135's calibration circuitry. However, because the magnitude of the offset produced by a synchronous signal depends on the signal's shape, recalibration may be appropriate if the shape or relative timing of the clock, or other digital signals change, as may occur if more than one clock signal or frequency is used.

Input Scaler

The MAX1134/MAX1135 have an input scaler, which allows conversion of true bipolar input voltages while operating from a single 3.3V supply. The input scaler attenuates and shifts the input as necessary to map the external input range to the input range of the internal ADC. The MAX1134 analog input range is 0 to +6V (unipolar) or ±6V (bipolar). The MAX1135 analog input

Table 1. Control Byte Format

BIT	NAME	DESCRIPTION		
7 (MSB)	START	The first logic 1 bit after $\overline{CS}$ goes low defines the beginning of the control byte.		
6	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, analog input signals from 0 to +6V (MAX1134) or 0 to +V_{REF} (MAX1135) can be converted. In bipolar mode, analog input signals from -6V to +6V (MAX1134) or -V_{REF} to +V_{REF} (MAX1135) can be converted.		
5	INT/$\overline{EXT}$	Selects the internal or external conversion clock. 1 = internal, 0 = external.		
4	M1	M1	M0	Mode
		0	0	24 external clocks per conversion (short acquisition mode)
		0	1	Start calibration: starts internal calibration
3	M0	1	0	Software power-down mode
		1	1	32 external clocks per conversion (long acquisition mode)
2	P2	These 3 bits are stored in a port register and output to pins P2, P1, and P0 for use in addressing a mux or PGA. These 3 bits are updated in the port register simultaneously when a new control byte is written.		
1	P1			
0 (LSB)	P0			

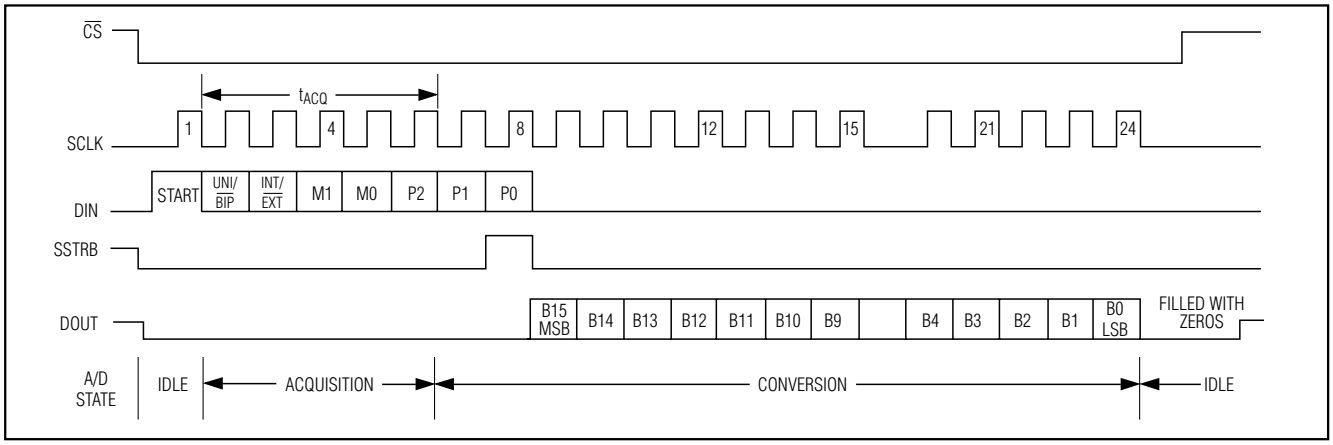


Figure 2. Short Acquisition Mode (24 Clock Cycles) External Clock

Table 2. User-Programmable Outputs

OUTPUT PIN	PROGRAMMED THROUGH CONTROL BYTE	POWER-ON OR $\overline{RST}$ DEFAULT	DESCRIPTION
P2	Bit 2	0	User-programmable outputs follow the state of the control byte's 3 LSBs, and are updated simultaneously when a new control byte is written. Outputs are push-pull. In hardware and software shutdown, these outputs are unchanged and remain low impedance.
P1	Bit 1	0	
P0	Bit 0	0	

range is 0 to +2.048V (unipolar) or ±2.048V (bipolar). Unipolar and bipolar mode selection is configured with bit 6 of the serial control byte (Table 1).

Figure 1 shows the equivalent input circuit of the MAX1134/MAX1135. The resistor network on the analog input provides ±16.5V fault protection. This circuit limits the current going into or out of the pin to less than 2mA. The overvoltage protection is active even if the device is in a power-down mode, or if AV_{DD} = 0.

Digital Interface

The digital interface pins consist of $\overline{SHDN}$, $\overline{RST}$, SSTRB, DOUT, SCLK, DIN, and $\overline{CS}$. Bringing $\overline{SHDN}$ low places the MAX1134/MAX1135 in its 1.2µA shutdown mode. A logic low on $\overline{RST}$ halts the MAX1134/MAX1135 operation and returns the part to its power-on-reset state.

In external clock mode, SSTRB is low and pulses high for one clock cycle at the start of conversion. In internal clock mode, SSTRB goes low at the start of the conversion, and goes high to indicate that the conversion is finished.

The DIN input accepts control byte data, which is clocked in on each rising edge of SCLK. After $\overline{CS}$ goes low or after a conversion or calibration completes, the first logic 1 clocked into DIN is interpreted as the START bit, the MSB of the 8-bit control byte.

The SCLK input is the serial-data-transfer clock, which clocks data in and out of the MAX1134/MAX1135. SCLK also drives the ADC conversion steps in external clock mode (see the *Internal and External Clock Modes* section).

DOUT is the serial output of the conversion result. DOUT is updated on the falling edge of SCLK. DOUT is high impedance when $\overline{CS}$ is high.

$\overline{CS}$ must be low for the MAX1134/MAX1135 to accept a control byte. The serial interface is disabled when $\overline{CS}$ is high.

User-Programmable Outputs

The MAX1134/MAX1135 have three user-programmable outputs: P0, P1, and P2. The power-on default state for the programmable outputs is zero. These are push-pull CMOS outputs suitable for driving a multiplexer, a PGA, or other signal preconditioning circuitry. Bits 0, 1, and 2 of the control byte control the user-programmable outputs (Tables 1, 2).

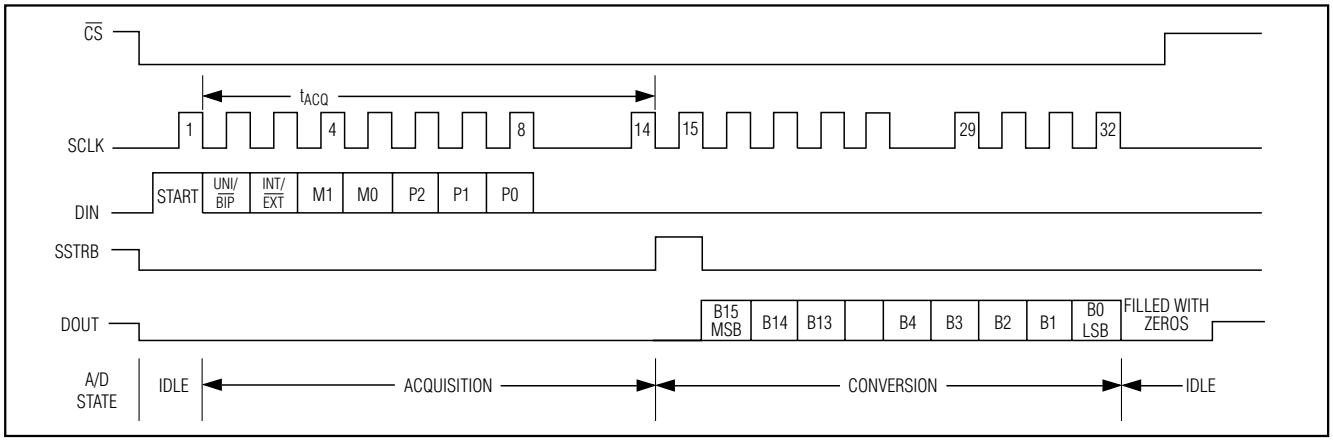


Figure 3. Long Acquisition Mode (32 Clock Cycles) External Clock

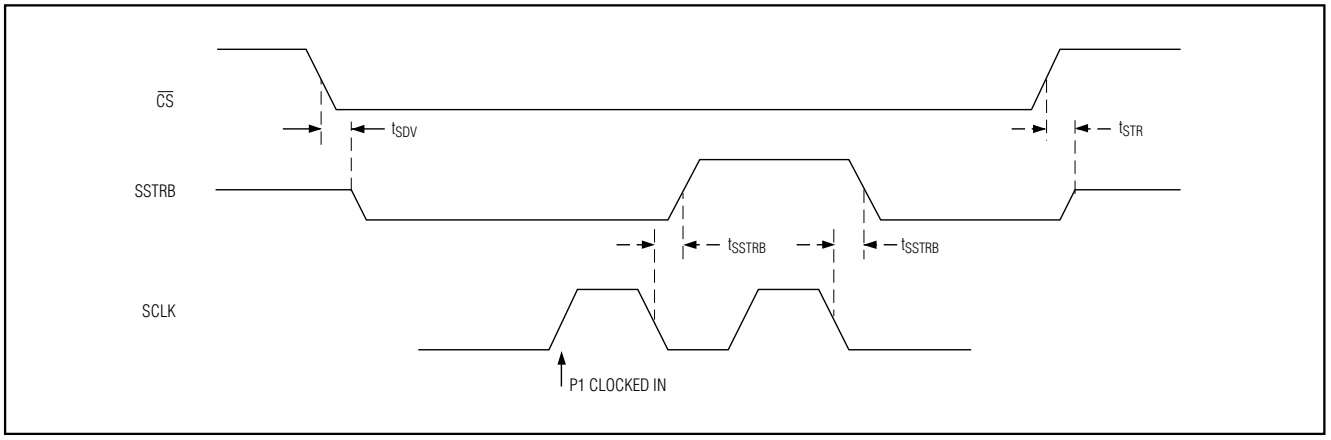


Figure 4. External Clock Mode SSTRB Detailed Timing

The user-programmable outputs are set to zero during power-on reset or when $\overline{RST}$ goes low. During hardware or software shutdown, P0, P1, and P2 are unchanged and remain low impedance.

Starting a Conversion

Start a conversion by clocking a control byte into the device's internal shift register. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1134/MAX1135s' internal shift register. After $\overline{CS}$ goes low or after a conversion or calibration completes, the first arriving logic 1 is defined as the start bit of the control byte. Until this first start bit arrives, any number of logic 0 bits can be clocked into DIN with no effect. If at any time during acquisition or conversion $\overline{CS}$ is brought high and then low again, the part is placed into a state where it can recognize a new start bit. If a new start bit occurs before the current conversion is complete, the conversion is aborted and a new acquisition is initiated.

Internal and External Clock Modes

The MAX1134/MAX1135 use either the external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1134/MAX1135. Bit 5 (INT/$\overline{EXT}$) of the control byte programs the clock mode.

External Clock

In external clock mode, the external clock not only shifts data in and out, but also drives the ADC conversion steps.

In short acquisition mode, SSTRB pulses high for one clock period after the seventh falling edge of SCLK following the start bit. The MSB of the conversion is available at DOUT on the eighth falling edge of SCLK (Figure 2).

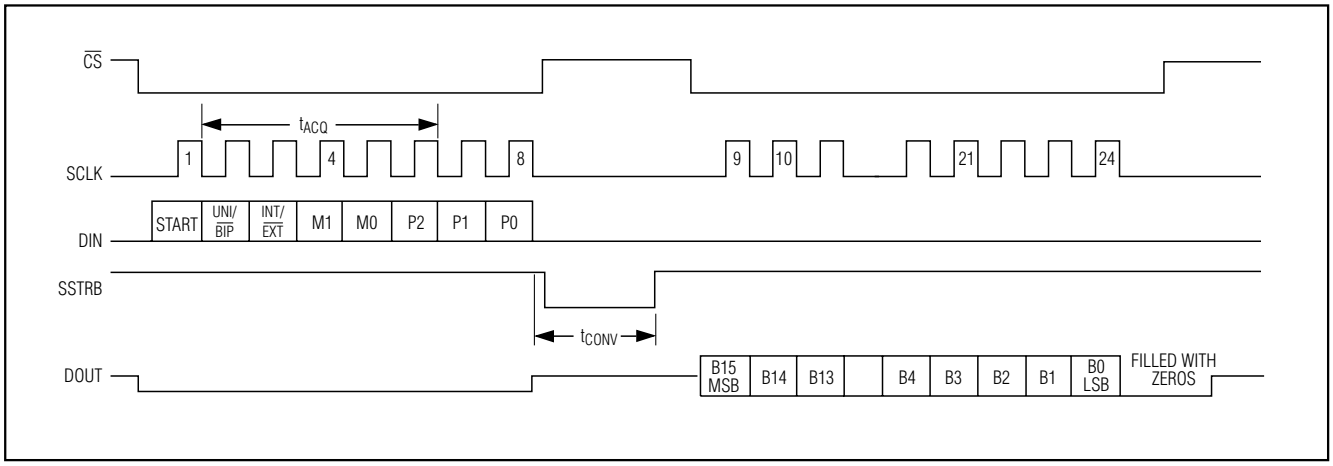


Figure 5. Internal Clock Mode Timing, Short Acquisition

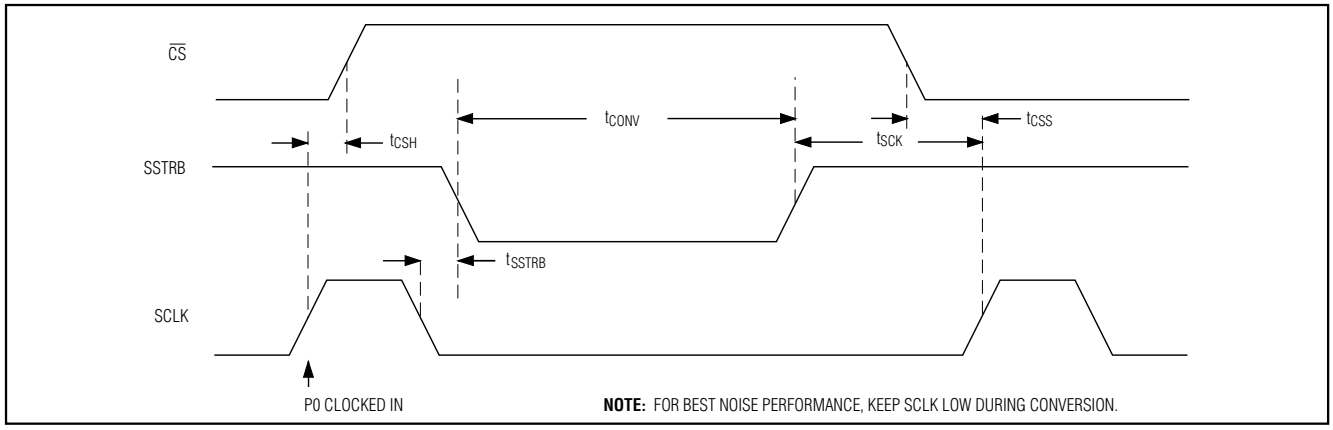


Figure 6. Internal Clock Mode SSTRB Detailed Timing

In long acquisition mode, when using external clock, SSTRB pulses high for one clock period after the 15th falling edge of SCLK following the start bit. The MSB of the conversion is available at DOUT on the 16th falling edge of SCLK (Figure 3).

In external clock mode, SSTRB is high impedance when $\overline{CS}$ is high (Figure 4). $\overline{CS}$ is normally held low during the entire conversion. If $\overline{CS}$ goes high during the conversion, SCLK is ignored until $\overline{CS}$ goes low. This allows external clock mode to be used with 8-bit bytes.

Internal Clock

In internal clock mode, the MAX1134/MAX1135 generate their own conversion clock. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate up to 4MHz.

SSTRB goes low at the start of the conversion and goes high when the conversion is complete. SSTRB is low for a maximum of 7µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out of the internal storage register at any time after the conversion is complete.

The MSB of the conversion is available at DOUT when SSTRB goes high. The subsequent 15 falling edges on SCLK shift the remaining bits out of the internal storage register (Figure 5). $\overline{CS}$ does not need to be held low once a conversion is started.

When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high. Figure 6 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted into the MAX1134/MAX1135 at clock rates up to 4MHz, pro-

Table 3. Unipolar Full Scale and Zero Scale

PART	ZERO SCALE	FULL SCALE
MAX1134	0	+6 (V_{REF}/2.048)
MAX1135	0	+V_{REF}

vided the minimum acquisition time, t_{ACQ}, is kept above 1.39µs in bipolar mode and 1.67µs in unipolar mode. Data can be clocked out at 4MHz.

Output Data

The output data format is straight binary for unipolar conversions and two's complement in bipolar mode. The MSB is shifted out of the MAX1134/MAX1135 first in both modes.

Data Framing

The falling edge of $\overline{CS}$ does not start a conversion on the MAX1134/MAX1135. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the seventh bit of the control byte (the P1 bit) is clocked into DIN. The start bit is defined as:

- The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle, e.g., after AV_{DD} is applied.
- The first high bit clocked into DIN after $\overline{CS}$ is pulsed high then low.

If a falling edge on $\overline{CS}$ forces a start bit before the conversion or calibration is complete, then the current operation terminates and a new one starts.

Applications Information

Power-On Reset

When power is first applied to the MAX1134/MAX1135, or if $\overline{RST}$ is pulsed low, the internal calibration registers are set to their default values. The user-programmable registers (P0, P1, and P2) are low, and the device is configured for bipolar mode with internal clocking.

Calibration

Periodically calibrate the MAX1134/MAX1135 to compensate for temperature drift and other variations. After any change in ambient temperature of more than +10°C, the device should be recalibrated. A 100mV change in supply voltage or any change in the reference voltage should be followed by a calibration. Calibration corrects for errors in gain, offset, integral nonlinearity, and differential nonlinearity.

The MAX1134/MAX1135 should be calibrated after power-up or after the assertion of reset. Make sure the power supplies and the reference voltage have fully settled prior to initiating the calibration sequence.

Table 4. Bipolar Full Scale, Zero Scale, and Negative Full Scale

PART	NEGATIVE FULL SCALE	ZERO SCALE	FULL SCALE
MAX1134	-6 (V_{REF}/2.048)	0	+6 (V_{REF}/2.048)
MAX1135	-V_{REF}	0	+V_{REF}

Initiate calibration by setting M1 = 0 and M0 = 1 in the control byte. In internal clock mode, SSTRB goes low at the beginning of calibration and goes high to signal the end of calibration, approximately 80,000 clock cycles later. In external clock mode, SSTRB goes high at the beginning of calibration and goes low to signal the end of calibration. Calibration should be performed in the same clock mode that is used for conversions.

Reference

The MAX1134/MAX1135 require a 2.048V reference. The reference must be bypassed with a 4.7µF capacitor. The input impedance at REF is a minimum of 16kΩ for DC currents. During conversion, the external reference at REF must deliver up to 150µA DC load current and have an output impedance of 10Ω or less.

Analog Input

The MAX1134/MAX1135 use a capacitive DAC that provides an inherent track/hold function. Drive AIN with a source impedance less than 10Ω. Any signal conditioning circuitry must settle with 16-bit accuracy in less than 500ns. Limit the input bandwidth to less than half the sampling frequency to eliminate aliasing. The MAX1134/MAX1135 have a complex input impedance that varies from unipolar to bipolar mode (Figure 1).

Input Range

The analog input range in unipolar mode is 0 to +6V for the MAX1134, and 0 to +2.048V for the MAX1135. In bipolar mode, the analog input can be -6V to +6V for the MAX1134, or -2.048V to +2.048V for the MAX1135. Unipolar or bipolar mode is programmed with the UNI/$\overline{BIP}$ bit of the control byte. When using a reference other than the suggested 2.048V, the full-scale input range varies accordingly. The full-scale input range depends on the voltage at REF and the sampling mode selected (Tables 3 and 4).

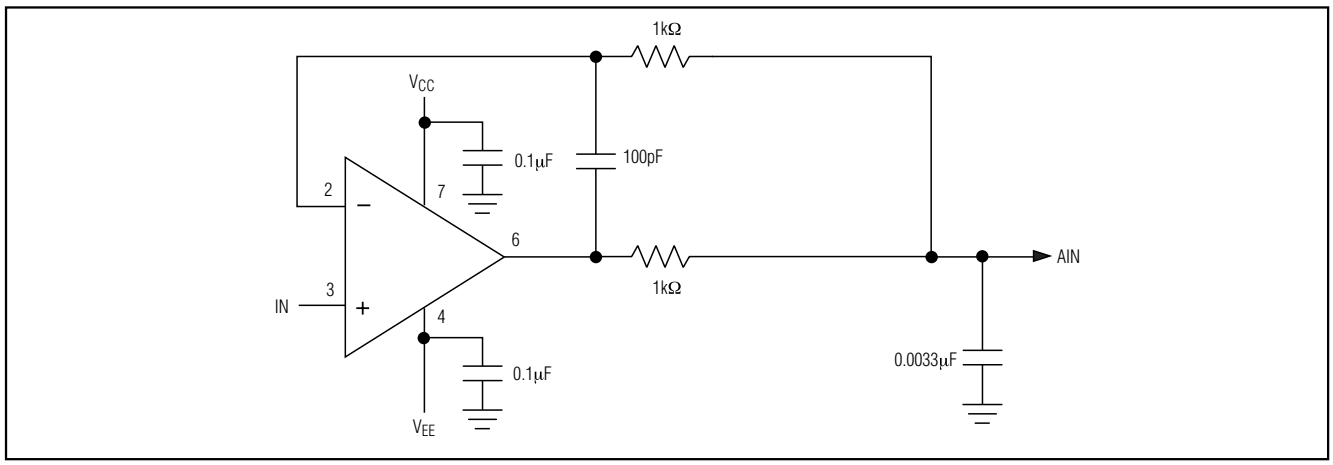


Figure 7. AIN Buffer for AC/DC Use

Input Acquisition and Settling

Clocking in a control byte starts input acquisition. The main capacitor array starts acquiring the input as soon as a start bit is recognized, using the same input range as the previous conversion. If the opposite input range is selected by the second DIN bit, the part immediately switches to the new sampling mode. Acquisition time is one-and-a-half clock cycles shorter when switching from unipolar to bipolar or bipolar to unipolar modes than when continuously converting in the same mode.

Acquisition can be extended by eight clock cycles by setting M1 = 1 and M0 = 1 (long acquisition mode). The sampling instant in short acquisition completes on the falling edge of the sixth clock cycle after the start bit (Figure 2). Acquisition is five clock cycles in short acquisition mode and 13 clock cycles in long acquisition mode. Short acquisition mode is 24 clock cycles per conversion. Using the external clock to run the conversion process limits unipolar conversion speed to 125ksps instead of 150ksps as in bipolar mode. The input resistance in unipolar mode is larger than that of bipolar mode (Figure 1). The RC time constant in unipolar mode is larger than that of bipolar mode, reducing the maximum conversion rate in 24 external clock mode. Long acquisition mode with external clock allows both unipolar and bipolar sampling of 112ksps (3.6MHz / 32 clock cycles) by adding eight extra clock cycles to the conversion.

Most applications require an input buffer amplifier. If the input signal is multiplexed, the input channel should be switched immediately after acquisition, rather than near the end of or after a conversion. This allows more time for the input buffer amplifier to respond to a large step change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change before the beginning of the acquisition time.

At the beginning of acquisition, the capacitive DAC is connected to the amplifier output, causing some output disturbance. Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the capacitive DAC with very little change in voltage. However, for AC use, AIN must be driven by a wideband buffer (at least 10MHz), which must be stable with the DAC's capacitive load (in parallel with any AIN bypass capacitor used) and also must settle quickly (Figure 7).

Digital Noise

Digital noise can couple to AIN and REF. The conversion clock (SCLK) and other digital signals that are active during input acquisition contribute noise to the conversion result. If the noise signal is synchronous to the sampling interval, an effective input offset is produced.

Asynchronous signals produce random noise on the input, whose high-frequency components may be aliased into the frequency band of interest. Minimize noise by presenting a low impedance (at the frequencies contained in the noise signal) at the inputs. This requires bypassing AIN to AGND, or buffering the input with an amplifier that has a small-signal bandwidth of several MHz, or preferably both. AIN has a bandwidth of about 4MHz.

Offsets resulting from synchronous noise (such as the conversion clock) are canceled by the MAX1134/MAX1135s' calibration scheme. However, because the magnitude of the offset produced by a synchronous signal depends on the signal's shape, recalibration may be appropriate if the shape or relative timing of the clock or other digital signals change, which can occur if more than one clock signal or frequency is used.

Distortion

Avoid degrading dynamic performance by choosing an amplifier with distortion much less than the MAX1134/MAX1135s' THD (-90dB) at frequencies of interest. If the chosen amplifier has insufficient common-mode rejection, which results in degraded THD performance, use the inverting configuration to eliminate errors from common-mode voltage. Low-temperature-coefficient resistors reduce linearity errors caused by resistance changes due to self-heating. To reduce linearity errors due to finite amplifier gain, use an amplifier circuit with sufficient loop gain at the frequencies of interest.

DC Accuracy

If DC accuracy is important, choose a buffer with an offset much less than the MAX1134/MAX1135s' maximum offset (±6mV), or whose offset can be trimmed while maintaining good stability over the required temperature range.

Operating Modes and Serial Interfaces

The MAX1134/MAX1135 are fully compatible with MICROWIRE and SPI/QSPI devices. MICROWIRE and SPI/QSPI both transmit a byte and receive a byte at the same time. The simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 16-bit conversion result).

Short Acquisition Mode (24 SCLK)

Configure short acquisition by setting M1 = 0 and M0 = 0. In short acquisition mode, the acquisition time is 5 clock cycles. The total period is 24 clock cycles per conversion.

Long Acquisition Mode (32 SCLK)

Configure long acquisition by setting M1 = 1 and M0 = 1. In long acquisition mode, the acquisition time is 13 clock cycles. The total period is 32 clock cycles per conversion.

Calibration Mode

A calibration is initiated through the serial interface by setting M1 = 0 and M0 = 1. Calibration can be done in either internal or external clock mode, though it is desirable that the part be calibrated in the same mode in which it will be used to do conversions. The part remains in calibration mode for approximately 80,000 clock cycles unless the calibration is aborted. Calibration is halted if $\overline{RST}$ or $\overline{SHDN}$ goes low, or if a valid start condition occurs.

Software Shutdown

A software power-down is initiated by setting M1 = 1 and M0 = 0. After the conversion completes, the part shuts down. It reawakens upon receiving a new start bit. Conversions initiated with M1 = 1 and M0 = 0 (shutdown) use the acquisition mode selected for the previous conversion.

Shutdown Mode

The MAX1134/MAX1135 may be shut down by pulling $\overline{SHDN}$ low or by asserting software shutdown. In addition to lowering power dissipation to 4.0µW, considerable power can be saved by shutting down the converter for short periods between conversions. There is no need to perform a calibration after the converter has been shut down unless the time in shutdown is long enough that the supply voltage or ambient temperature has changed.

Supplies, Layout, Grounding, and Bypassing

For best system performance, use separate analog and digital ground planes. The two ground planes should be tied together at the MAX1134/MAX1135. Use pin 3 and pin 14 as the primary AGND and DGND, respectively. If the analog and digital supplies come from the same source, isolate the digital supply from the analog with a low-value resistor (10Ω).

The MAX1134/MAX1135 are not sensitive to the order of AV_{DD} and DV_{DD} sequencing. Either supply can be present in the absence of the other. Do not apply an external reference voltage until after both AV_{DD} and DV_{DD} are present.

Be sure that digital return currents do not pass through the analog ground. All return-current paths must be low impedance. A 5mA current flowing through a PC board ground trace impedance of only 0.05Ω creates an error voltage of about 250µV, or about 2LSBs error with a ±4V full-scale system. The board layout should ensure that digital and analog signal lines are kept separate. Do not run analog and digital lines parallel to one another. If you must cross one with the other, do so at right angles.

The ADC is sensitive to high-frequency noise on the AV_{DD} power supply. Bypass this supply to the analog ground plane with 0.1µF. If the main supply is not adequately bypassed, add an additional 1µF or 10µF low-ESR capacitor in parallel with the primary bypass capacitor.

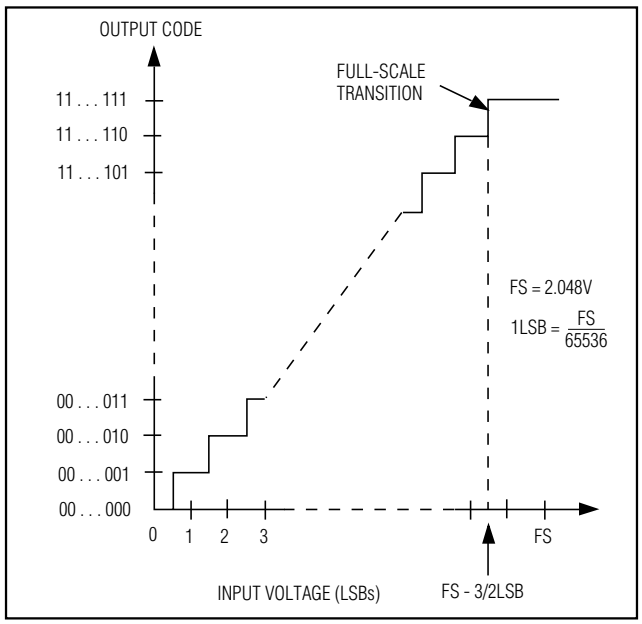


Figure 8. MAX1135 Unipolar Transfer Function, 2.048V = Full Scale

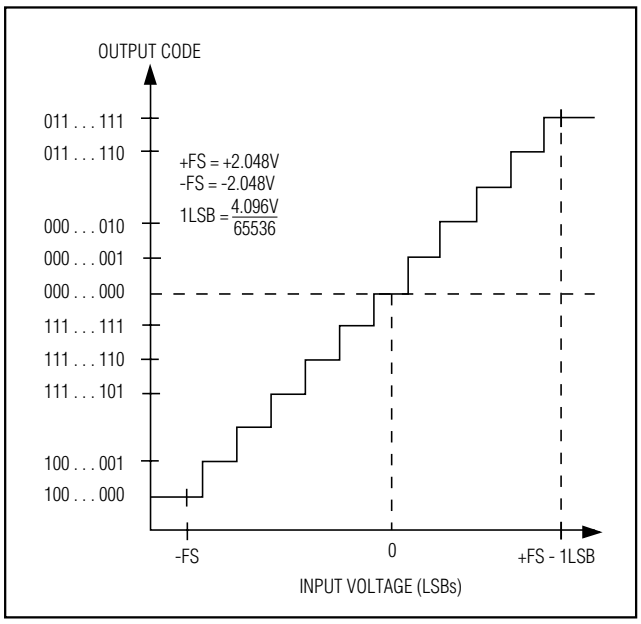


Figure 9. MAX1135 Bipolar Transfer Function, 4.096V = Full Scale

Transfer Function

Figures 8 and 9 show the MAX1135s' transfer functions. In unipolar mode, the output data is in binary format and in bipolar mode it is in two's complement format.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1134/MAX1135 is measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N-bits):

$$SNR = (6.02 \times N + 1.76)\ dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals:

$$SINAD\ (dB) = 20 \times \log (Signal_{RMS} / Noise_{RMS})$$

16-Bit ADCs, 150ksps, 3.3V Single Supply

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

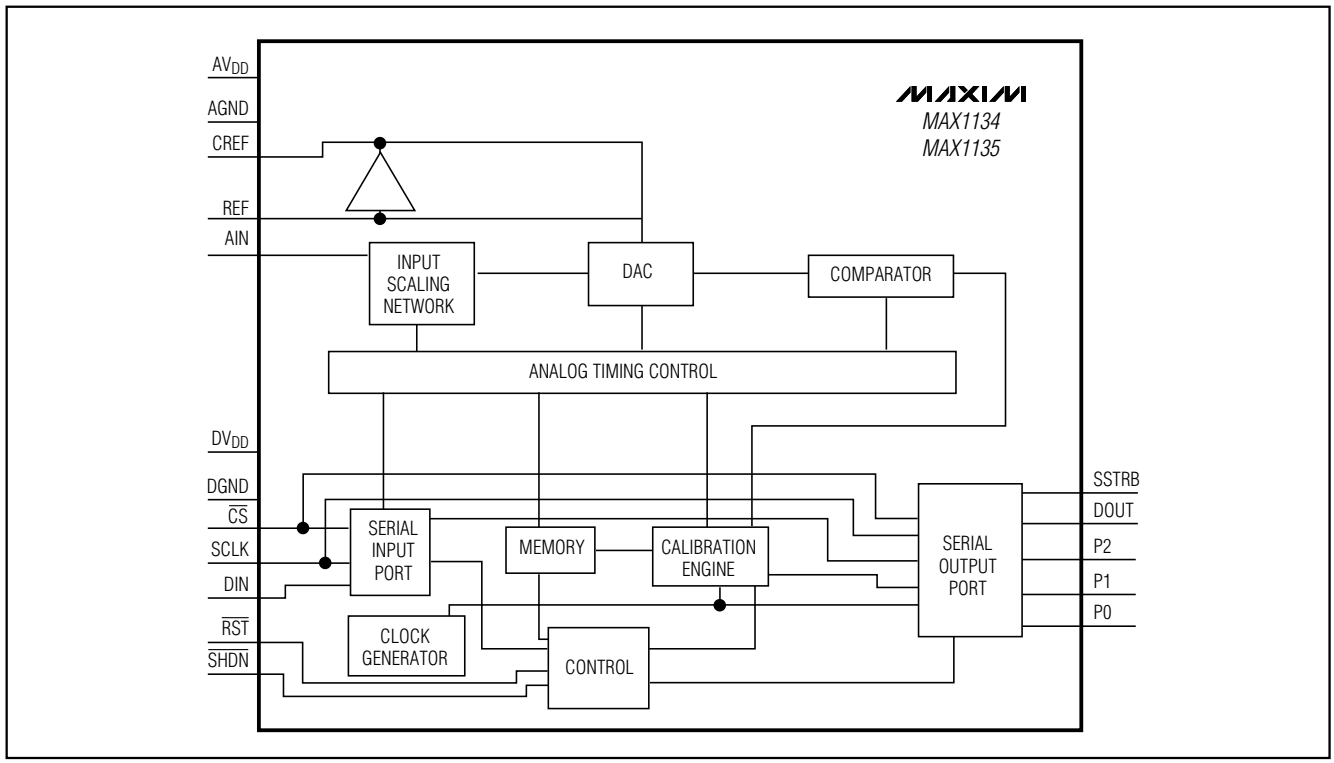
$$THD = 20 \times \log\left[\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}\right]$$

where V1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

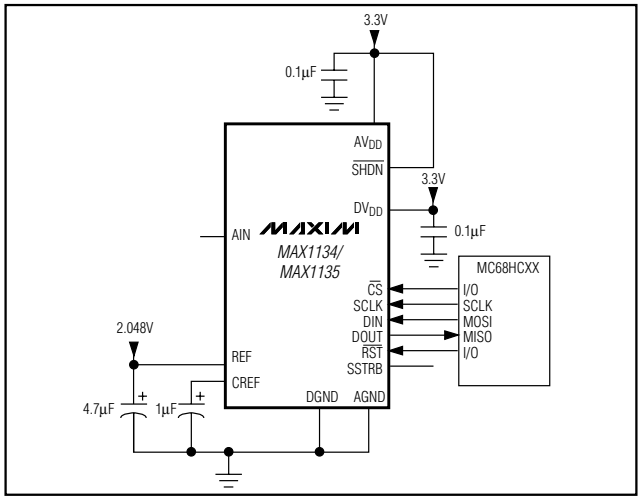
Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest distortion component.

Functional Diagram



Typical Application Circuit



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1135BCAP	0°C to +70°C	20 SSOP	±2.5
MAX1135BEAP	-40°C to +85°C	20 SSOP	±2.5

Chip Information

TRANSISTOR COUNT: 21,807

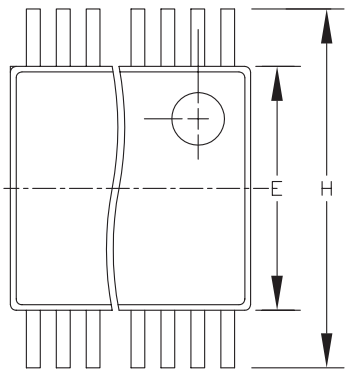
PROCESS: BiCMOS

16-Bit ADCs, 150ksps, 3.3V Single Supply

Package Information

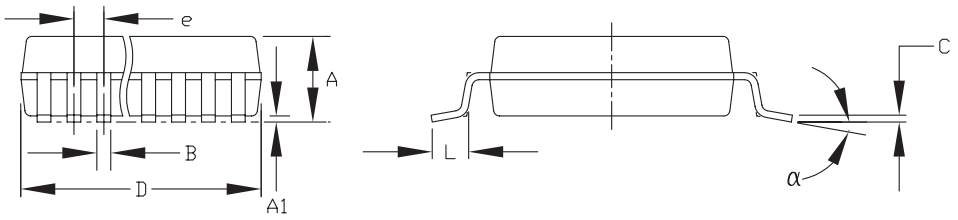
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3x.65mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0056	REV B	1/1