PRELIMINARY

T-49-19-16

80C196KA
16-BIT HIGH PERFORMANCE CHMOS MICROCONTROLLER

- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 2.3 μs 16 x 16 Multiply
- 4.0 μs 32/16 Divide
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Full Duplex Serial Port
- Dedicated Baud Rate Generator
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with S/H
- Dynamically Configurable 8-Bit or 16-Bit Buswidth

The 80C196KA is the CHMOS upgrade for the 8096. It is pin-for-pin compatible and uses a true superset of the 8096 instructions. At the same oscillator frequency the 80C196KA state time generator operates 1.5 times as fast as the 8096. In addition, many instruction execution times have been reduced providing up to twice the performance of a 12 MHz 8096 with a 12 MHz 80C196KA. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

Bit, byte, word and some 32-bit operations are available on the 80C196KA. With a 12 MHz oscillator a 16-bit addition takes 0.66 μs, and the instruction times average 0.5 μs to 1.5 μs in typical applications.

Four high-speed capture inputs are provided to record times which events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

Also provided on-chip are an A/D converter, serial port, watchdog timer, and a pulse-width-modulated output signal.

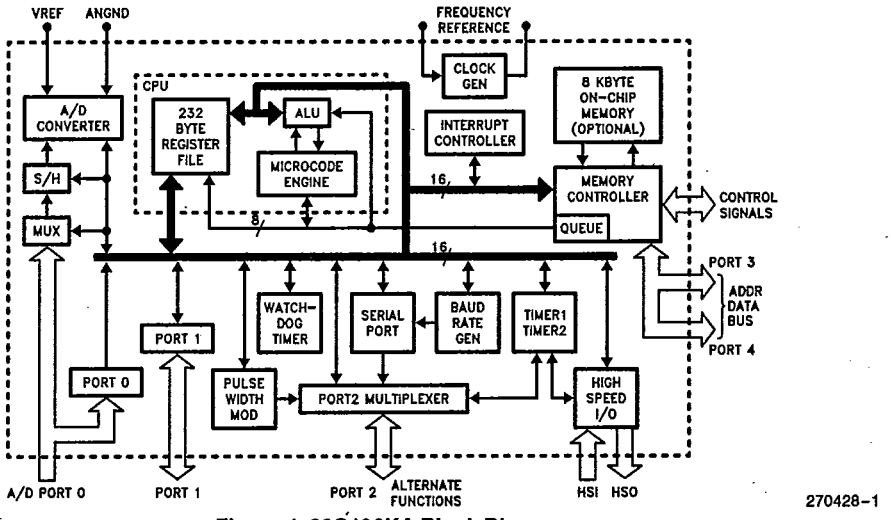


Figure 1. 80C196KA Block Diagram

ARCHITECTURE

The 80C196KA is a member of the MCS®-96 family, and as such has the same architecture and uses the same instruction set as the 8096. Many new features have been added on the 80C196KA including:

CPU FEATURES

Divide by 2 instead of divide by 3 clock for 1.5X performance

Faster instructions, especially indexed/indirect data operations

2.33 μs 16 $\times$ 16 multiply with 12 MHz clock (was 6.25 μs)

Faster interrupt response (almost twice as fast)

Powerdown and Idle Modes

Clock Failure Detect

6 new instructions including Compare Long and Block Move

8 new interrupt vectors/6 new interrupt sources

PERIPHERAL FEATURES

SFR Window switching allows read-only registers to be written and vice-versa

Timer2 can count up and down by external selection

Timer2 has an independent capture register

HSO line events are stored in a register

HSO has CAM Lock and CAM Clear commands

New Baud Rate values are needed for serial port, higher speeds possible in all modes

Double buffered serial port transmit register

Serial Port Receive Overrun and Framing Error Detection

PWM has a Divide-by-2 Prescaler

NEW INSTRUCTIONS

PUSHA — PUSHes the PSW, IMASK, IMASK1, and WSR

(Used instead of PUSHF when new interrupts and registers are used.)

assembly language format: PUSHA

object code format: <11110100>

bytes: 1

states: on-chip stack: 12
off-chip stack: 18

POPA — POPs the PSW, IMASK, IMASK1, and WSR
(Used instead of POPF when new interrupts and registers are used.)

assembly language format: POPA
object code format: <11110101>
bytes: 1
states: on-chip stack: 12
off-chip stack:18

IDLPD — Sets the part into Idle or Powerdown Mode

assembly language format: IDLPD #key (key=1 for Idle, key=2 for Powerdown.)
object code format: <11110110> <key>
bytes: 2
states: legal key: 8
illegal key: 25

DJNZW — Decrement Jump Not Zero using a Word counter

assembly language format: DJNZW wreg, cadd
object code format: <11100001> <wreg> <disp>
bytes: 3
states: jump not taken: 5
jump taken: 9

CMPL — Compare 2 long direct values
assembly language format:

```
                          DST  SRC
CMPL                      Lreg, Lreg
```

object code format: <11000101> <src Lreg> <dst Lreg>
bytes: 3
states: 7

BMOV — Block move using 2 auto-incrementing pointers and a counter

assembly language format:

```
                          PTRS  CNTREG
BMOV                      Lreg, wreg
```

object code format: <11000001> <wreg> <Lreg>
bytes: 3
states:
internal/internal: 8 per transfer + 6
external/internal: 11 per transfer + 6
external/external: 14 per transfer + 6

SFR OPERATION

All of the registers that were present on the 8096 work the same way as they did, except that the baud rate value is different. The new registers shown in the memory map control new functions. The most important new register is the Window Select Register (WSR) which allows reading of the formerly write-only registers and vice-versa. Using the WSR is described later in this data sheet.

PACKAGING

The 80C196KA is available in 68-pin PLCC and LCC packages. Contact your local sales office to determine the exact ordering code for the part desired.

LCC	PLCC	Description	LCC	PLCC	Description	LCC	PLCC	Description
1	9	ACH7/P0.7	24	54	AD6/P3.6	47	31	P1.6
2	8	ACH6/P0.6	25	53	AD7/P3.7	48	30	P1.5
3	7	ACH2/P0.2	26	52	AD8/P4.0	49	29	HSO.1
4	6	ACH0/P0.0	27	51	AD9/P4.1	50	28	HSO.0
5	5	ACH1/P0.1	28	50	AD10/P4.2	51	27	HSO.5/HSI.3
6	4	ACH3/P0.3	29	49	AD11/P4.3	52	26	HSO.4/HSI.2
7	3	NMI	30	48	AD12/P4.4	53	25	HSI.1
8	2	$\overline{EA}$	31	47	AD13/P4.5	54	24	HSI.0
9	1	V_{CC}	32	46	AD14/P4.6	55	23	P1.4
10	68	V_{SS}	33	45	AD15/P4.7	56	22	P1.3
11	67	XTAL1	34	44	T2CLK/P2.3	57	21	P1.2
12	66	XTAL2	35	43	READY	58	20	P1.1
13	65	CLKOUT	36	42	T2RST/P2.4	59	19	P1.0
14	64	BUSWIDTH	37	41	$\overline{BHE}/\overline{WRH}$	60	18	TXD/P2.0
15	63	INST	38	40	$\overline{WR}/\overline{WRL}$	61	17	RXD/P2.1
16	62	ALE/$\overline{ADV}$	39	39	PWM/P2.5	62	16	$\overline{RESET}$
17	61	$\overline{RD}$	40	38	P2.7/T2CAPTURE	63	15	EXTINT/P2.2
18	60	AD0/P3.0	41	37	V_{PP}	64	14	CDE
19	59	AD1/P3.1	42	36	V_{SS}	65	13	V_{REF}
20	58	AD2/P3.2	43	35	HSO.3	66	12	ANGND
21	57	AD3/P3.3	44	34	HSO.2	67	11	ACH4/P0.4
22	56	AD4/P3.4	45	33	P2.6/T2UP/DN	68	10	ACH5/P0.5
23	55	AD5/P3.5	46	32	P1.7			

Figure 2. Pin Definitions

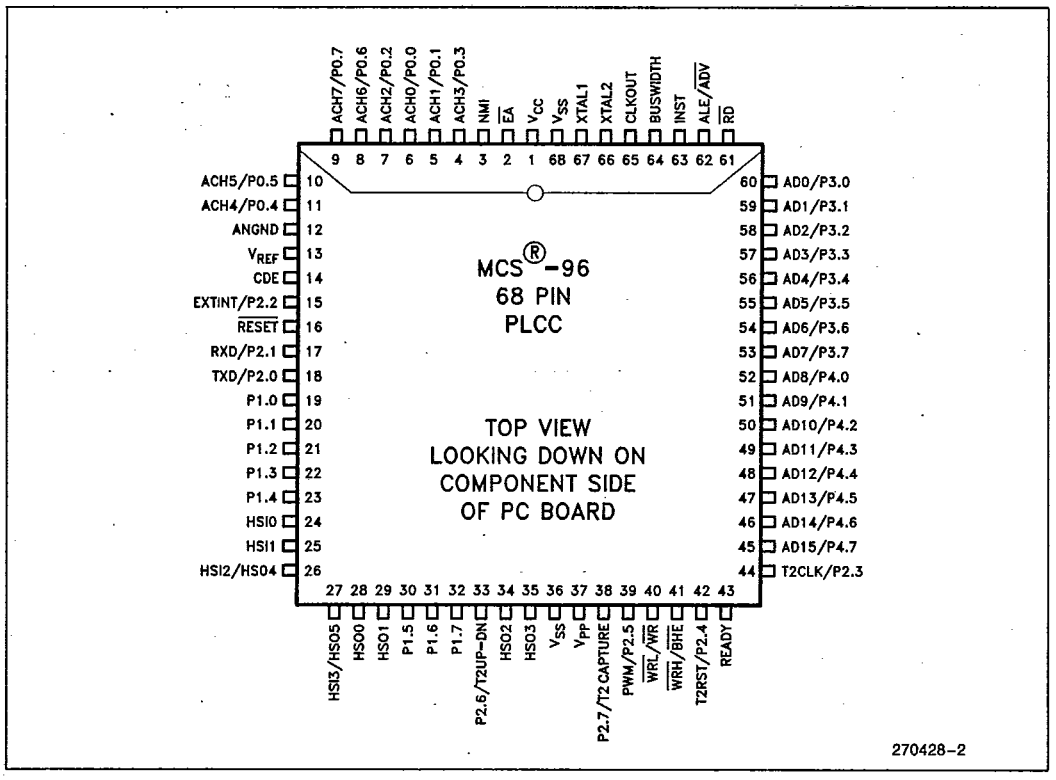


Figure 3. 68-Pin Package (PLCC—Top View)

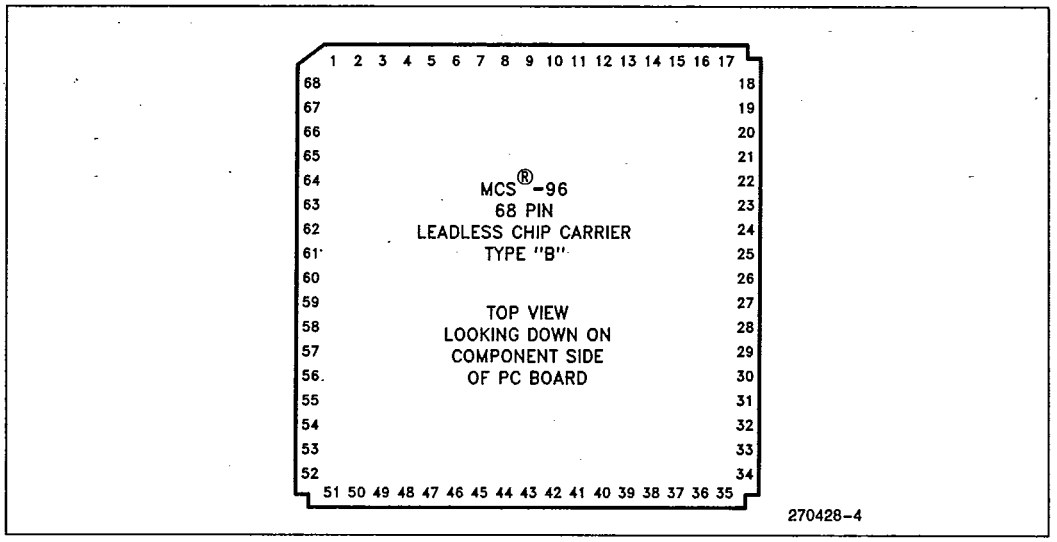


Figure 4. 68-Pin Package (LCC—Top View)

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are two V_{SS} pins, both of which must be connected.
CDE	Clock Detect Enable - When pulled high enables the clock failure detection circuit. If the XTAL1 frequency falls below a specified limit the $\overline{\text{RESET}}$ pin will be pulled low.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used V_{PP} may be tied to V_{CC}. This pin was V_{BB} on the 8X9X-90 parts and will be the programming voltage on future EPROM parts.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input to the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re- synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. This pin is the $\overline{\text{TEST}}$ pin on 8X9X-90 parts. Systems with $\overline{\text{TEST}}$ tied to V_{CC} do not need to change.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes acccesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2, and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit. The HSI pins are also used as inputs by future EPROM parts in Programming Mode.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4, and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also a mode input to future EPROM parts in the Programming Mode.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KA.
Ports 3 and 4	8-bit bi-directional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Available only on future ROM and EPROM parts.

Instruction Summary

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D ← D + A	✓	✓	✓	✓	↑	–	
ADD/ADDB	3	D ← B + A	✓	✓	✓	✓	↑	–	
ADDC/ADDCB	2	D ← D + A + C	↓	✓	✓	✓	↑	–	
SUB/SUBB	2	D ← D − A	✓	✓	✓	✓	↑	–	
SUB/SUBB	3	D ← B − A	✓	✓	✓	✓	↑	–	
SUBC/SUBCB	2	D ← D − A + C − 1	↓	✓	✓	✓	↑	–	
CMP/CMPB	2	D − A	✓	✓	✓	✓	↑	–	
MUL/MULU	2	D,D + 2 ← D × A	–	–	–	–	–	–	2
MUL/MULU	3	D,D + 2 ← B × A	–	–	–	–	–	–	2
MULB/MULUB	2	D,D + 1 ← D × A	–	–	–	–	–	–	3
MULB/MULUB	3	D,D + 1 ← B × A	–	–	–	–	–	–	3
DIVU	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	✓	↑	–	2
DIVUB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	✓	↑	–	3
DIV	2	D ← (D,D + 2) /A,D + 2 ← remainder	–	–	–	✓	↑	–	
DIVB	2	D ← (D,D + 1) /A,D + 1 ← remainder	–	–	–	✓	↑	–	
AND/ANDB	2	D ← D AND A	✓	✓	0	0	–	–	
AND/ANDB	3	D ← B AND A	✓	✓	0	0	–	–	
OR/ORB	2	D ← D OR A	✓	✓	0	0	–	–	
XOR/XORB	2	D ← D (ecxl. or) A	✓	✓	0	0	–	–	
LD/LDB	2	D ← A	–	–	–	–	–	–	
ST/STB	2	A ← D	–	–	–	–	–	–	
LDBSE	2	D ← A; D + 1 ← SIGN(A)	–	–	–	–	–	–	3,4
LDBZE	2	D ← A; D + 1 ← 0	–	–	–	–	–	–	3,4
PUSH	1	SP ← SP − 2; (SP) ← A	–	–	–	–	–	–	
POP	1	A ← (SP); SP + 2	–	–	–	–	–	–	
PUSHF	0	SP ← SP − 2; (SP) ← PSW; PSW ← 0000H; I ← 0	0	0	0	0	0	0	
POPF	0	PSW ← (SP); SP ← SP + 2; I ← ✓	✓	✓	✓	✓	✓	✓	
SJMP	1	PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LJMP	1	PC ← PC + 16-bit offset	–	–	–	–	–	–	5
BR[indirect]	1	PC ← (A)	–	–	–	–	–	–	
SCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 11-bit offset	–	–	–	–	–	–	5
LCALL	1	SP ← SP − 2; (SP) ← PC; PC ← PC + 16-bit offset	–	–	–	–	–	–	5

Instruction Summary (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
RET	0	PC ← (SP); SP ← SP + 2	–	–	–	–	–	–	
J (conditional)	1	PC ← PC + 8-bit offset (if taken)	–	–	–	–	–	–	5
JC	1	Jump if C = 1	–	–	–	–	–	–	5
JNC	1	jump if C = 0	–	–	–	–	–	–	5
JE	1	jump if Z = 1	–	–	–	–	–	–	5
JNE	1	Jump if Z = 0	–	–	–	–	–	–	5
JGE	1	Jump if N = 0	–	–	–	–	–	–	5
JLT	1	Jump if N = 1	–	–	–	–	–	–	5
JGT	1	Jump if N = 0 and Z = 0	–	–	–	–	–	–	5
JLE	1	Jump if N = 1 or Z = 1	–	–	–	–	–	–	5
JH	1	Jump if C = 1 and Z = 0	–	–	–	–	–	–	5
JNH	1	Jump if C = 0 or Z = 1	–	–	–	–	–	–	5
JV	1	Jump if V = 0	–	–	–	–	–	–	5
JNV	1	Jump if V = 1	–	–	–	–	–	–	5
JVT	1	Jump if VT = 1; Clear VT	–	–	–	–	0	–	5
JNVT	1	Jump if VT = 0; Clear VT	–	–	–	–	0	–	5
JST	1	Jump if ST = 1	–	–	–	–	–	–	5
JNST	1	Jump if ST = 0	–	–	–	–	–	–	5
JBS	3	Jump if Specified Bit = 1	–	–	–	–	–	–	5,6
JBC	3	Jump if Specified Bit = 0	–	–	–	–	–	–	5,6
DJNZ/ DJNZW	1	D ← D − 1; If D ≠ 0 then PC ← PC + 8-bit offset	–	–	–	–	–	–	5
DEC/DECB	1	D ← D − 1	↕	↕	↕	↕	↑	–	
NEG/NEGB	1	D ← 0 − D	↕	↕	↕	↕	↑	–	
INC/INCB	1	D ← D + 1	↕	↕	↕	↕	↑	–	
EXT	1	D ← D; D + 2 ← Sign (D)	↕	↕	0	0	–	–	2
EXTB	1	D ← D; D + 1 ← Sign (D)	↕	↕	0	0	–	–	3
NOT/NOTB	1	D ← Logical Not (D)	↕	↕	0	0	–	–	
CLR/CLRB	1	D ← 0	1	0	0	0	–	–	
SHL/SHLB/SHLL	2	C ← msb - - - - - lsb ← 0	↕	↕	↕	↕	↑	–	7
SHR/SHRB/SHRL	2	0 → msb - - - - - lsb → C	↕	↕	↕	0	–	↕	7
SHRA/SHRAB/SHRAL	2	msb → msb - - - - - lsb → C	↕	↕	↕	0	–	↕	7
SETC	0	C ← 1	–	–	1	–	–	–	
CLRC	0	C ← 0	–	–	0	–	–	–	

Instruction Summary (Continued)

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
CLRVT	0	VT ← 0	–	–	–	–	0	–	
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable All Interupts (I ← 0)	–	–	–	–	–	–	
EI	0	Enable All Interupts (I ← 1)	–	–	–	–	–	–	
NOP	0	PC ← PC + 1	–	–	–	–	–	–	
SKIP	0	PC ← PC + 2	–	–	–	–	–	–	
NORML	2	Left shift till msb = 1;D ← shift count	✓	✓	0	–	–	–	7
TRAP	0	SP ← SP – 2; (SP) ← PC; PC ← (2010H)	–	–	–	–	–	–	9
PUSHA	1	SP ← SP-2; (SP) ← PSW; PSW ← 0000H; SP ← SP-2; (SP) ← IMASK1/WSR; IMASK1 ← 00H	0	0	0	0	0	0	
POPA	1	IMASK1/WSR ← (SP); SP ← SP+2 PSW ← (SP); SP ← SP+2	✓	✓	✓	✓	✓	✓	
IDLPD	1	IDLE MODE IF KEY=1; POWERDOWN MODE IF KEY =2; CHIP RESET OTHERWISE	–	–	–	–	–	–	
CMPL	2	D-A	✓	✓	✓	✓	↑	–	
BMOV	2	[PTR_HI]+ ← [PTR_LOW]+ ; UNTIL COUNT=0	–	–	–	–	–	–	

NOTES:
1. If the mnemonic ends in "B" a byte operation is performed, otherwise a word operation is done. Operands is done. Operands D, B, and A must conform to the alignment rules for the required operand type. D and B are locations in the Register File; A can be located anywhere in memory.
2. D,D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D,D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (Long) suffix indicates double-word operation.
8. Initiates a Reset by pulling $\overline{\text{RESET}}$ low. Software should re-initialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept this mnemonic.

Instruction Execution State Times

MNEMONIC	DIRECT	IMMED	INDIRECT		INDEXED	
			NORMAL*	A-INC*	SHORT*	LONG*
ADD (3-op)	5	6	7/9	8/10	7/9	8/10
SUB (3-op)	5	6	7/9	8/10	7/9	8/10
ADD (2-op)	4	5	6/8	7/9	6/8	7/9
SUB (2-op)	4	5	6/8	7/9	6/8	7/9
ADDC	4	5	6/8	7/9	6/8	7/9
SUBC	4	5	6/8	7/9	6/8	7/9
CMP	4	5	6/8	7/9	6/8	7/9
ADDB (3-op)	5	5	7/9	8/10	7/9	8/10
SUBB (3-op)	5	5	7/9	8/10	7/9	8/10
ADDB (2-op)	4	4	6/8	7/9	6/8	7/9
SUBB (2-op)	4	4	6/8	7/9	6/8	7/9
ADDCB	4	4	6/8	7/9	6/8	7/9
SUBCB	4	4	6/8	7/9	6/8	7/9
CMPB	4	4	6/8	7/9	6/8	7/9
MUL (3-op)	16	17	18/21	19/22	19/22	20/23
MULU (3-op)	14	15	16/19	17/20	17/20	18/21
MUL (2-op)	16	17	18/21	19/22	19/22	20/23
MULU (2-op)	14	15	16/19	17/20	17/20	18/21
DIV	26	27	28/31	29/32	29/32	30/33
DIVU	24	25	26/29	27/30	27/30	28/31
MULB (3-op)	12	12	14/17	15/18	15/18	16/19
MULUB (3-op)	10	10	12/15	12/16	12/16	14/17
MULB (2-op)	12	12	14/17	15/18	15/18	16/19
MULUB (2-op)	10	10	12/15	12/16	12/16	14/17
DIVB	18	18	20/23	21/24	21/24	22/25
DIVUB	16	16	18/21	19/22	19/22	20/23
AND (3-op)	5	6	7/9	8/10	7/9	8/10
AND (2-op)	4	5	6/8	7/9	6/8	7/9
OR (2-op)	4	5	6/8	7/9	6/8	7/9
XOR	4	5	6/8	7/9	6/8	7/9
ANDB (3-op)	5	5	7/9	8/10	7/9	8/10
ANDB (2-op)	4	4	6/8	7/9	6/8	7/9
ORB (2-op)	4	4	6/8	7/9	6/8	7/9
XORB	4	4	6/8	7/9	6/8	7/9
LD/LDB	4	5	5/7	6/8	6/8	7/9
ST/STB	4	5	5/7	6/8	6/8	7/9
LDBSE	4	4	5/7	6/8	6/8	7/9
LDBZE	4	4	5/7	6/8	6/8	7/9
BMOV	6+8 per word			6 + 11/14 per word		
PUSH (int stack)	6	7	9/12	10/13	10/13	11/14
POP (int stack)	8	–	10/12	11/13	11/13	12/14
PUSH (ext stack)	8	9	11/14	12/15	12/15	13/16
POP (ext stack)	11	–	13/15	14/16	14/16	15/17

*Times for (Internal/External) Operands

Instruction Execution State Times (Continued)

MNEMONIC		MNEMONIC	
PUSHF (int stack)	6	PUSHF (ext stack)	8
POPF (int stack)	7	POPF (ext stack)	10
PUSHA (int stack)	12	PUSHA (ext stack)	18
POPA (int stack)	12	POPA (ext stack)	18
TRAP (int stack)	16	TRAP (ext stack)	18
LCALL (int stack)	11	LCALL (ext stack)	13
SCALL (int stack)	11	SCALL (ext stack)	13
RET (int stack)	11	RET (ext stack)	14
CMPL	7	DEC/DECB	3
CLR/CLRB	3	EXT/EXTB	4
NOT/NOTB	3	INC/INCB	3
NEG/NEGB	3		
LJMP	7		
SJMP	7		
BR [indirect]	7		
JNST, JST	4/8 jump not taken/jump taken		
JNH, JH	4/8 jump not taken/jump taken		
JGT, JLE	4/8 jump not taken/jump taken		
JNC, JC	4/8 jump not taken/jump taken		
JNVT, JVT	4/8 jump not taken/jump taken		
JNV, JV	4/8 jump not taken/jump taken		
JGE, JLT	4/8 jump not taken/jump taken		
JNE, JE	4/8 jump not taken/jump taken		
JBC, JBS	5/9 jump not taken/jump taken		
DJNZ	5/9 jump not taken/jump taken		
DJNZW	5/9 jump not taken/jump taken		
NORML	8 + 1 per shift (9 for 0 shift)		
SHRL	7+ 1 per shift (8 for 0 shift)		
SHLL	7 + 1 per shift (8 for 0 shift)		
SHRAL	7 + 1 per shift (8 for 0 shift)		
SHR/SHRB	6 + 1 per shift (7 for 0 shift)		
SHL/SHLB	6 + 1 per shift (7 for 0 shift)		
SHRA/SHRAB	6 + 1 per shift (7 for 0 shift)		
CLRC	2		
SETC	2		
DI	2		
EI	2		
CLRVT	2		
NOP	2		
RST	15 (includes fetch of configuration byte)		
SKIP	3		
IDLPD	8/25 (proper key/improper key)		

intel

80C196KA

PRELIMINARY

T-49-19-16

MEMORY MAP

	0FFFFH
EXTERNAL MEMORY OR I/O	
	4000H
INTERNAL ROM/EPROM OR EXTERNAL MEMORY*	
	2080H
RESERVED	
	2040H
UPPER 8 INTERRUPT VECTORS (NEW ON 80C196KA)	
	2030H
ROM/EPROM SECURITY KEY*	
	2020H
RESERVED	
	2019H
CHIP CONFIGURATION BYTE	
	2018H
RESERVED	
	2014H
LOWER 8 INTERRUPT VECTORS PLUS 2 SPECIAL INTERRUPTS	
	2000H
PORT 3 AND PORT 4	
	1FFEH
EXTERNAL MEMORY OR I/O	
	0100H
INTERNAL DATA MEMORY - REGISTER FILE (STACK POINTER, RAM AND SFRS) EXTERNAL PROGRAM CODE MEMORY	
	0000H

*ROM/EPROM will be available on future versions of 80C196.

80C196KA INTERRUPTS

Number	Source	Vector Location	Priority
INT15	NMI	203EH	15
INT14	HSI FIFO Full	203CH	14
INT13	EXTINT Pin	203AH	13
INT12	TIMER2 Overflow	2038H	12
INT11	TIMER2 Capture	2036H	11
INT10	4th Entry into HSI FIFO	2034H	10
INT09	RI	2032H	9
INT08	TI	2030H	8
SPECIAL	Unimplemented Opcode	2012H	N/A
SPECIAL	Trap	2010H	N/A
INT07	EXTINT	200EH	7
INT06	Serial Port	200CH	6
INT05	Software Timer	200AH	5
INT04	HSI.0 Pin	2008H	4
INT03	High Speed Outputs	2006H	3
INT02	HSI Data Available	2004H	2
INT01	A/D Conversion Complete	2002H	1
INT00	Timer Overflow	2000H	0

	WHEN READ	WHEN WRITTEN
19H	STACK POINTER	STACK POINTER
18H		
17H	*IOS2	PWM_CONTROL
16H	IOS1	IOC1
15H	IOS0	IOC0
14H	*WSR	*WSR
13H	*INT_MASK 1	*INT_MASK 1
12H	*INT_PEND 1	*INT_PEND 1
11H	*SP_STAT	*SP_CON
10H	PORT2	PORT2
0FH	PORT1	PORT1
0EH	PORT0	BAUD RATE
0DH	TIMER2 (HI)	TIMER2 (HI)
0CH	TIMER2 (LO)	TIMER2 (LO)
0BH	TIMER1 (HI)	*IOC2
0AH	TIMER1 (LO)	WATCHDOG
09H	INT_PENDING	INT_PENDING
08H	INT_MASK	INT_MASK
07H	SBUF(RX)	SBUF(TX)
06H	HSI_STATUS	HSO_COMMAND
05H	HSI_TIME (HI)	HSO_TIME (HI)
04H	HSI_TIME (LO)	HSO_TIME (LO)
03H	AD_RESULT (HI)	HSI_MODE
02H	AD_RESULT (LO)	AD_COMMAND
01H	ZERO REG (HI)	ZERO REG (HI)
00H	ZERO REG (LO)	ZERO REG (LO)

WSR = 0

	WSR = 15
0DH	*T2 CAPTURE (HI)
0CH	*T2 CAPTURE (LO)

OTHER SFRS IN WSR 15 BECOME READABLE IF THEY WERE WRITABLE IN WSR = 0 AND WRITABLE IF THEY WERE READABLE IN WSR = 0

*NEW OR CHANGED REGISTER FUNCTION

USING THE ALTERNATE REGISTER WINDOW (WSR = 15)

I/O register expansion on the new CHMOS members of the MCS-96 family has been provided by making two register windows available. Switching between these windows is done using the Window Select Register (WSR). The PUSHA and POPA instructions can be used to push and pop the WSR and second interrupt mask when entering or leaving interrupts, so it is easy to change between windows.

On the 80C196KA only Window 0 and Window 15 are active. Window 0 is a true superset of the standard 8096 SFR space, while Window 15 allows the read-only registers to be written and write-only registers to be read. The only major exception to this is the Timer2 register which is the Timer2 capture register in Window 15. The writeable register for Timer2 is in Window 0. There are also some minor changes and cautions. The descriptions of the registers which have different functions in Window 15 than in Window 0 are listed below:

AD_COMMAND (02H) — Read the last written command

AD_RESULT (02H, 03H) — Write a value into the result register

HSI_MODE (03H) — Read the value in HSI_MODE

HSI_TIME (04H,05H) — Write to FIFO Holding register

HSO_TIME (04H,05H) — Read the last value placed in the holding register

HSI_STATUS (06H) — Write to status bits but not to HSI pin bits. (Pin bits are 1,3,5,7).

HSO_COMMAND (06H) — Read the last value placed in the holding register

SBUF(RX) (07H) — Write a value into the receive buffer

SBUF(TX) (07H) — Read the last value written to the transmit buffer

WATCHDOG(0AH) — Read the value in the upper byte of the WDT

TIMER1 (0AH,0BH) — Write a value to Timer1

TIMER2 (0CH,0DH) — Read/Write the Timer2 capture register.
Note that Timer2 read/write is done with WSR = 0.

IOC2 (0BH) — Last written value is readable, except bit 7 (note 1)

BAUD_RATE (0EH) — No function, cannot be read

PORT0 (0EH) — No function, no output drivers on the pins

SP_STAT (11H) — Set the status bits, TI and RI can be set, but it will not cause an interrupt

SP_CON (11H) — Read the current control byte

IOS0 (15H) — Writing to this register controls the HSO pins. Bits 6 and 7 are inactive for writes.

IOC0 (15H) — Last written value is readable, except bit 1 (note 1)

IOS1 (16H) — Writing to this register will set the status bits, but not cause interrupts. Bits 6 and 7 are not functional

IOC1 (16H) — Last written value is readable

IOS2 (17H) — Writing to this register will set the status bits, but not cause interrupts.

PWM_CONTROL (17H) — Read the duty cycle value written to PWM_CONTROL

NOTE:

1. IOC2.7 (CAM CLEAR) and IOC0.1 (T2RST) are not latched and will read as a 1 (precharged bus) .

Being able to write to the read-only registers and vice-versa provides a lot of flexibility. One of the most useful advantages is the ability to set the timers and HSO lines for initial conditions other than zero.

SFR BIT SUMMARY

A summary of the SFRs which control I/O functions has been included in this section. The summary is separated into a list of those SFRs which have changed on the 80C196 and a list of those which have remained the same.

The following 80C196 SFRs are different than those on the 8096BH:

(The Read and Write comments indicate the register's function in Window 0 unless otherwise specified.)

SBUF(TX):
07h
write

Now double buffered

BAUD RATE:
0Eh
write

Uses new Baud Rate Values

SP_STAT:

7	6	5	4	3	2	1	0
RB8/ RPE	RI	TI	FE	TXE	OE	X	X

11h
read

RPE : Receive Parity Error
RI : Receive Indicator
TI : Transmit Indicator
FE : Framing Error
TXE : Transmitter Empty
OE : Receive Overrun Error

IPEND1:
IMASK1:

7	6	5	4	3	2	1	0
NMI	FIFO FULL	EXT INT	T2 OVF	T2 CAP	HSI4	RI	TI

12h,13h
read/write

NMI : Non-Maskable Interrupt
FIFO FULL : HSIO FIFO full
EXTINT : External Interrupt Pin
T2OVF : Timer2 Overflow
T2CAP : Timer2 Capture
HSI4 : HSI has 4 or more entries in FIFO
RI : Receive Interrupt
TI : Transmit Interrupt

WSR:

7	6	5	4	3	2	1	0
X	X	X	X	W	W	W	W

14h
read/write

WWWW = 0 : SFRs function like a superset of 8096 SFRs

WWWW = 15
: Exchange read/write registers

WWWW = OTHER : Undefined, do not use

XXXX = 0000B : These bits must always be written as zeros to provide compatibility with future products.

IOS2:

7	6	5	4	3	2	1	0
START A2D	T2 RESET	HSO.5	HSO.4	HSO.3	HSO.2	HSO.1	HSO.0

17h
read

Indicates which HSO event occured

START A2D : HSO__CMD 15, start A to D

T2RESET : HSO__CMD 14, Timer 2 reset

HSO.0-5 : Output pins HSO.0 through HSO.5

IOC2:

7	6	5	4	3	2	1	0
CLEAR CAM	ENA LOCK	T2ALT INT	A2D CPD	NOSH	SLOW PWM	T2UD ENA	FAST T2EN

0Bh
write

CLEAR__CAM : Clear Entire CAM

ENA__LOCK : Enable lockable CAM entry feature

T2ALT INT : Enable T2 Alternate Interrupt at 8000H

A2D__CPD : Clock Prescale Disable for low XTAL frequency (A to D conversion in fewer state times)

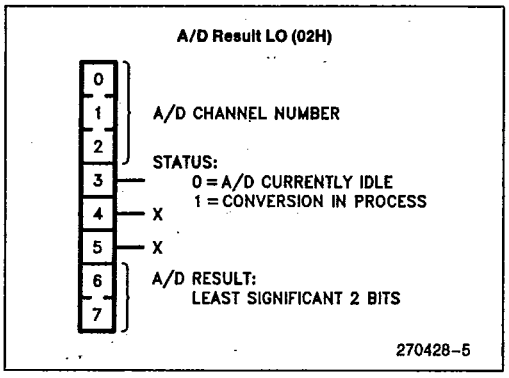
NOSH : Disable A/D Sample and Hold

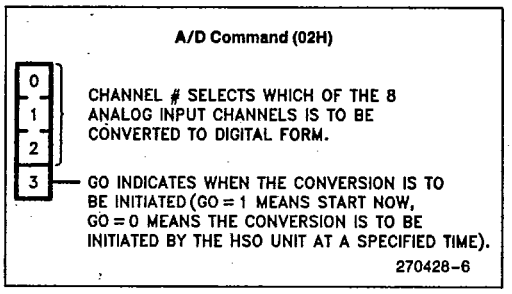
SLOW__PWM : Turn on divide by 2 Prescaler on PWM

T2UD ENA : Enable Timer 2 as up/down counter

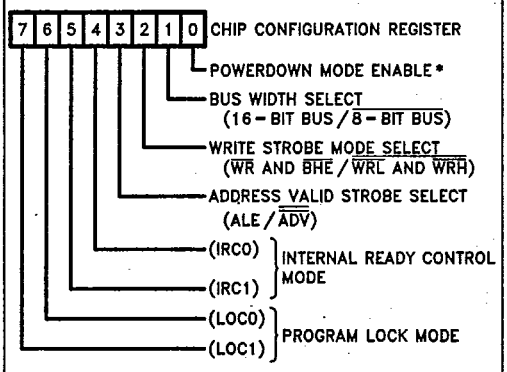
FAST__T2EN : Enable Fast increment of T2; once per state time.

The following registers are the same on the 80C196 as they were on the 8096BH:





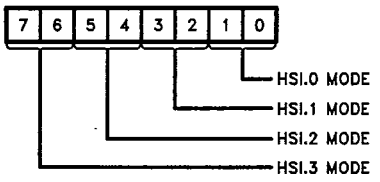
Chip Configuration (2108H)



270428-7

*Minor Change

HSI_Mode (03H)

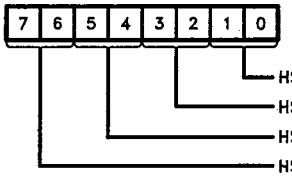


WHERE EACH 2-BIT MODE CONTROL FIELD DEFINES ONE OF 4 POSSIBLE MODES:

00 8 POSITIVE TRANSITIONS
01 EACH POSITIVE TRANSITION
10 EACH NEGATIVE TRANSITION
11 EVERY TRANSITION (POSITIVE AND NEGATIVE)

270428-8

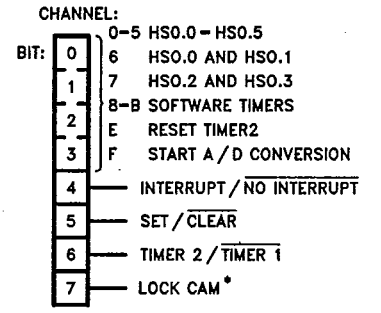
HSI_Status (06H)



WHERE FOR EACH 2-BIT STATUS FIELD THE LOWER BIT INDICATES WHETHER OR NOT AN EVENT HAS OCCURED ON THIS PIN AND THE UPPER BIT INDICATES THE CURRENT STATUS OF THE PIN.

270428-9

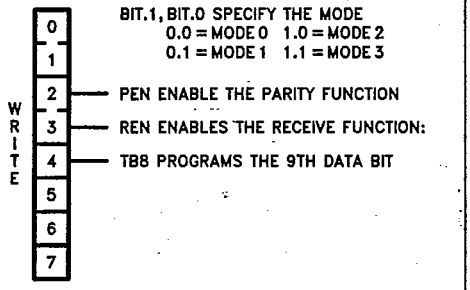
HSO Command (06H)



270428-10

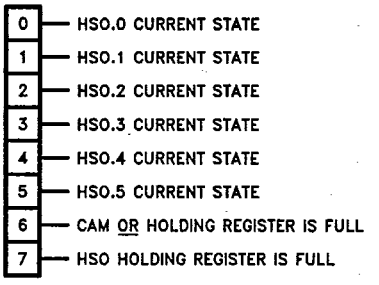
*Minor Change

SPCON (11H)



270428-11

IOS0 (15H)



270428-12

IOC0 (15H)

0	HSI.0 INPUT ENABLE / $\overline{\text{DISABLE}}$
1	TIMER 2 RESET EACH WRITE
2	HSI.1 INPUT ENABLE / $\overline{\text{DISABLE}}$
3	TIMER 2 EXTERNAL RESET ENABLE / $\overline{\text{DISABLE}}$
4	HSI.2 INPUT ENABLE / $\overline{\text{DISABLE}}$
5	TIMER 2 RESET SOURCE HSI.0 / $\overline{\text{T2RST}}$
6	HSI.3 INPUT ENABLE / $\overline{\text{DISABLE}}$
7	TIMER 2 CLOCK SOURCE HSI.1 / $\overline{\text{T2CLK}}$

270428-13

IOS1 (16H)

0	SOFTWARE TIMER 0 EXPIRED
1	SOFTWARE TIMER 1 EXPIRED
2	SOFTWARE TIMER 2 EXPIRED
3	SOFTWARE TIMER 3 EXPIRED
4	TIMER 2 HAS OVERFLOW
5	TIMER 1 HAS OVERFLOW
6	HSI FIFO IS FULL
7	HSI HOLDING REGISTER DATA AVAILABLE

270428-14

IOC1 (16H)

0	SELECT PWM / $\overline{\text{SELECT P2.5}}$
1	EXTERNAL INTERRUPT ACH7 / $\overline{\text{EXTINT}}$
2	TIMER 1 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$
3	TIMER 2 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$
4	HSO.4 OUTPUT ENABLE / $\overline{\text{DISABLE}}$
5	SELECT TXD / $\overline{\text{SELECT P2.0}}$
6	HSO.5 OUTPUT ENABLE / $\overline{\text{DISABLE}}$
7	HSI INTERRUPT FIFO FULL / $\overline{\text{HOLDING REGISTER LOADED}}$

270428-15

Port 2 Multiple Functions

Pin	Func.	Alternative Function	Control Reg.
2.0	Output	TXD (Serial Port Transmit)	IOC1.5
2.1	Input	RXD (Serial Port Receive)	SPCON.3
2.3	Input	T2CLK (Timer2 Clock & Baud)	IOC0.7
2.4	Input	T2RST (Timer2 Reset)	IOC0.5
2.5	Output	PWM Output	IOC1.0
2.6	QBD*	Timer2 up/ down select	IOC2.1
2.7	QBD*	Timer2 Capture	N/A

*QBD = Quasi-bidirectional

Baud Rate Calculations

Asynchronous Modes 1, 2 and 3:

$$\text{Baud\_Reg} = \frac{\text{XTAL1}}{\text{Baud Rate} \times 16} - 1 \text{ OR } \frac{\text{T2CLK}}{\text{Baud Rate} \times 8}$$

Synchronous Mode 0:

$$\text{Baud\_Reg} = \frac{\text{XTAL1}}{\text{Baud Rate} \times 2} - 1 \text{ OR } \frac{\text{T2CLK}}{\text{Baud Rate}}$$

Baud Rates and Baud Register Values

Baud Rate	XTAL Frequency		
	8.0 MHz	10.0 MHz	12.0 MHz
300	1666/−0.02	2082/0.02	2499/0.00
1200	416/−0.08	520/−0.03	624/0.00
2400	207/0.16	259/0.16	312/−0.16
4800	103/−0.16	129/0.16	155/0.16
9600	51/−0.16	64/0.16	77/0.16
19.2K	25/0.16	32/1.40	38/0.16

Baud Register Value/% Error

A maximum baud rate of 750 Kbaud is available in the asynchronous modes with 12 MHz on XTAL1. The synchronous mode has a maximum rate of 3.0 Mbaud with a 12 MHz clock. Location 0EH is the Baud Register. It is loaded sequentially in two bytes, with the low byte being loaded first. This register may not be loaded with zero in serial port Mode 0.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V
Power Dissipation 1.5W

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

Operating Conditions

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.5	5.50	V
T_{REF}	Analog Supply Voltage	4.5	5.50	V
f_{OSC}	Oscillator Frequency	3.5	12	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

D.C. Characteristics (Over specified operating conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (except XTAL 1)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.0	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	µA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		±3	µA	0 < V_{IN} < V_{REF}
I_{TL}	1 to 0 Transition Current (QBD Pins)		−650	µA	V_{IN} = 2.0V
I_{IL}	Logical 0 Input Current (QBD Pins)		−50	µA	V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current in Reset (ALE, RD, WR, BHE, INST, P2.0)		−500	µA	V_{IN} = 0.45 V

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D.C. Characteristics (Over specified operating conditions) (Continued)

Symbol	Description	Min	Max	Units	Test Conditions
I_{CC}	Active Mode Current in Reset		60	mA	XTAL1 = 12 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		5	mA	
I_{idle}	Idle Mode Current		22	mA	
I_{CC1}	Active Mode Current (Typical)		15	mA	XTAL1 = 3.5 MHz
I_{PD}	Powerdown Mode Current		TBD	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K	50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	f_{TEST} = 1.0 MHz

NOTES:
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include all bus pins (data and control), HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0, and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs, which will be available on future ROM and EPROM parts.
3. Standard Inputs include HSI pins, CDE, EA, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3, and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply to each group of pins:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{\text{RESET}}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.7, P2.5, $\overline{\text{WR}}$, $\overline{\text{BHE}}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{\text{RD}}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

A.C. Characteristics (Over specified operating conditions)

These are ADVANCED specifications, the parameters may change before Intel releases the product for sale.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} = 12 MHz

The system must meet these specifications to work with the 80C196:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 55$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 55$	ns	
T_{YLYH}	NonREADY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 2)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC}+5$	$2T_{OSC}-40$	ns	(Note 2)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 55$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 55$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 60$	ns	
T_{RLDV}	RD# Active to Input Data Valid		$T_{OSC} - 25$	ns	
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 55$	ns	
T_{RHDZ}	End of RD# to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after RD# Inactive	0		ns	

NOTES:
1. Typical specification, not guaranteed.
2. If max is exceeded, additional wait states will occur.

A.C. Characteristics (Over specified operating conditions) (Continued)

These are ADVANCED specifications, the parameters may change before Intel releases the product for sale.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} = 12 MHz

The 80C196KA will meet these specifications:

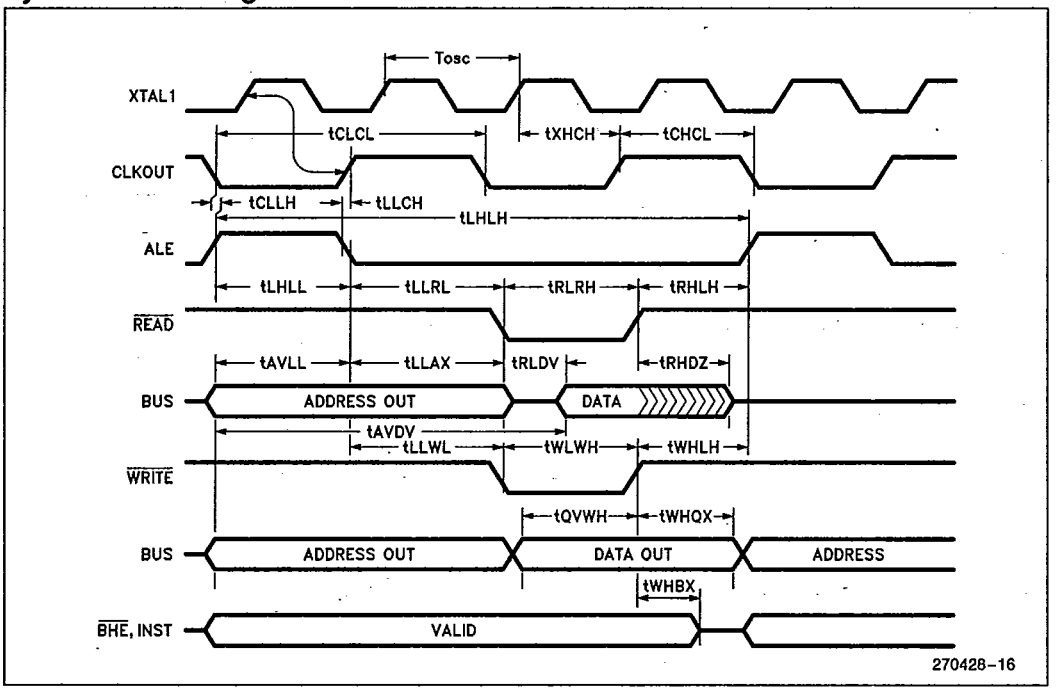
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1	3.5	12.0	MHz	
T_{OSC}	$1/F_{XTAL}$	83	286	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	40	110	ns	(Note 1)
T_{CLCL}	CLKOUT Cycle Time	$2T_{OSC}$		ns	
T_{CHCL}	CLKOUT High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−10	10	ns	
T_{LHLH}	ALE Cycle Time	$4T_{OSC}$		ns	
T_{LHLL}	ALE High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	$T_{OSC}-25$		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	$T_{OSC}-15$		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC}-25$		ns	
T_{RLCL}	$\overline{RD}$ Falling Edge to CLKOUT Falling Edge	0	20	ns	
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC}-5$		ns	
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	$T_{OSC}-15$	$T_{OSC}+15$	ns	(Note 2)
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC}-10$		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	−5	15	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC}-20$		ns	
T_{CHWH}	CLKOUT Rising Edge to $\overline{WR}$ Rising Edge	−10	10	ns	
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC}-20$		ns	
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-20$		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	$T_{OSC}-20$	$T_{OSC}+20$	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST HOLD after $\overline{WR}$ Rising Edge	$T_{OSC}-30$		ns	

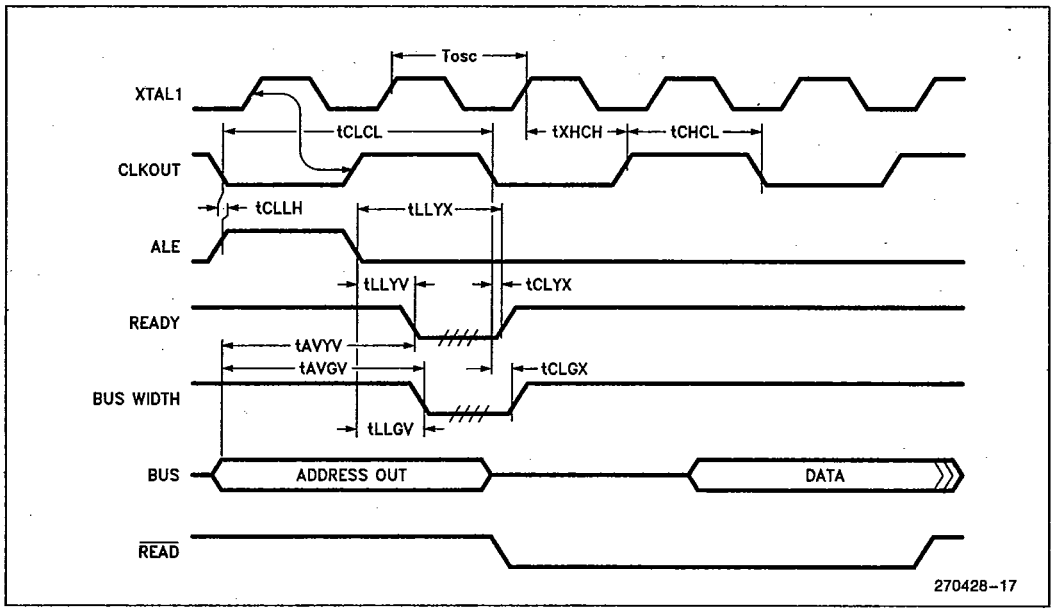
NOTES:

T_{OSC} = 83.3 ns at 12 MHz; T_{OSC} = 125 ns at 8 MHz.

1. Typical specification, not guaranteed.
2. Assuming back-to-back bus cycles.

System Bus Timings

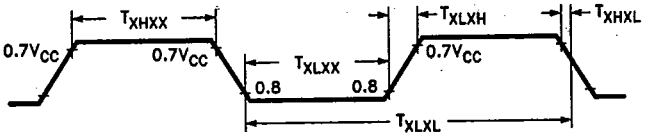




EXTERNAL CLOCK DRIVE

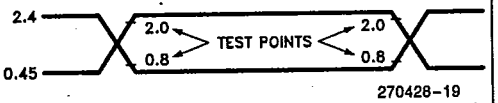
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	3.5	12	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	83	286	ns
T_{XHXX}	High Time	32		ns
T_{XLXX}	Low Time	32		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



270428-18

A.C. TESTING INPUT, OUTPUT WAVEFORM



270428-19

A.C. Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORM

270428-20

For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H - High
L - Low
V - Valid
X - No Longer Valid
Z - Floating

Signals:

A - Address
B - $\overline{BHE}$
C - CLKOUT
D - DATA
G - Buswidth
L - ALE/$\overline{ADV}$
R - $\overline{RD}$
W - $\overline{WR}/\overline{WRH}/\overline{WRL}$
X - XTAL1
Y - READY

A TO D CHARACTERISTICS

There are four modes of A/D operation.

In Modes 2 and 3 the maximum XTAL1 frequency is 10.0 MHz. Accuracy will degrade at higher frequencies.

	Clock Prescaler On IOC2.4 = 0	Clock Prescaler Off IOC2.4 = 1	
IOC2.3 = 0 with S&H	Mode 0–158 States 26.33 μs @ 12 MHz	Mode 2–91 States 22.75 μs @ 8 MHz	91 States 18.2 μs @ 10 MHz
IOC2.3 = 1 without S&H	Mode 1–293 States 48.83 μs @ 12 MHz	Mode 3–163 States 40.75 μs @ 8 MHz	163 States 32.6 μs @ 10 MHz

A/D CONVERTER SPECIFICATIONS

The absolute conversion accuracy is dependent on the accuracy of V_{REF}. The specifications given below assume adherence to the Operating Conditions section of these data sheets. Testing is done at V_{REF} = 5.120V, 10.0 MHz, A/D Mode 2.

Parameter	Typical*(1)	Minimum	Maximum	Units**	Notes
Resolution		256(5)	1024 10	Levels Bits	5
Absolute Error		0	±4	LSBs	
Full Scale Error	−0.5 ±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±4	LSBs	
Differential Non-Linearity		0	±2	LSBs	5
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	1
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	 1 1 1
Off Isolation		−60		dB	1,2,4
Feedthrough	−60			dB	1,2
V_{CC} Power Supply Rejection	−60			dB	1,2
Input Resistance		1K	5K	Ω	1
D.C. Input Leakage		0	3.0	μA	

NOTES:
* These values are expected for most parts at 25°C.
**An "LSB", as used here, has a value of approximately 5 mV.
1. These values are not tested in production and are based on theoretical estimates and laboratory tests.
2. DC to 100 KHz.
3. For starting the A/D with an HSO Command.
4. Multiplexer Break-Before-Make Guaranteed.
5. See functional deviations list.

A/D GLOSSARY OF TERMS

ABSOLUTE ERROR—The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

ACTUAL CHARACTERISTIC—The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An actual characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversions under the same conditions.

BREAK-BEFORE-MAKE—The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected. (e.g. the converter will not short inputs together.)

CHANNEL-TO-CHANNEL MATCHING—The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

CHARACTERISTIC—A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

CODE—The digital value output by the converter.

CODE CENTER—The voltage corresponding to the midpoint between two adjacent code transitions.

CODE TRANSITION—The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

CODE WIDTH—The voltage corresponding to the difference between two adjacent code transitions.

CROSSTALK—See "Off-Isolation".

D.C. INPUT LEAKAGE—Leakage current to ground from an analog input pin.

DIFFERENTIAL NON-LINEARITY—The difference between the ideal and actual code widths of the terminal based characteristic.

FEEDTHROUGH—Attenuation of a voltage applied on the selected channel of the A/D Converter after the sample window closes.

FULL SCALE ERROR—The difference between the expected and actual input voltage corresponding to the full scale code transition.

IDEAL CHARACTERISTIC—A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

INPUT RESISTANCE—The effective series resistance from the analog input pin to the sample capacitor.

LSB—Least Significant Bit: The voltage corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For an 8-bit converter with a reference voltage of 5.12V, one LSB is 20 mV. Note that this is different than digital LSBs, since an uncertainty of two LSB, when referring to an A/D converter, equals 40 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 80 mV.)

MONOTONIC—The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

NO MISSED CODES—For each and every output code, there exists a unique input voltage range which produces that code only.

NON-LINEARITY—The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristic.

OFF-ISOLATION—Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

REPEATABILITY—The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

RESOLUTION—The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

SAMPLE DELAY—The delay from receiving the start conversion signal to when the sample window opens.

SAMPLE DELAY UNCERTAINTY—The variation in the sample delay.

SAMPLE TIME—The time that the sample window is open.

SAMPLE TIME UNCERTAINTY—The variation in the sample time.

SAMPLE WINDOW—Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

SUCCESSIVE APPROXIMATION—An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

TEMPERATURE COEFFICIENTS—Change in the stated variable per degree centigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of temperature drift.

TERMINAL BASED CHARACTERISTIC—An actual characteristic which has been rotated and translated to remove zero offset and full scale error.

V_{CC} REJECTION—Attenuation of noise on the V_{CC} line to the A/D converter.

ZERO OFFSET—The difference between the expected and actual input voltage corresponding to the first code transition.

80C196KA FUNCTIONAL DEVIATIONS

The 80C196KA has the following problems. We are working on, or have already defined, silicon fixes for all these problems.

1. Byte shifts on odd addresses do not work properly (SHRB and SHLB). Byte shifts can be done on even addresses, and word and long shifts work correctly.
2. The Unsigned Divide operations (Byte and Word), may result in a quotient that is one count larger than the correct value (DIVU and DIVUB). This can only occur if the most significant bit of the divisor is a one. The problem will not always occur if the MSB is one, and determining if the problem will occur or not is very difficult.
3. The current in the power down mode is on the order of 1 milliamp.
4. The PUSHA instruction works properly with internal stack. When external stack is used, the PUSHA instruction will cause the data to be written into the location pointed to by the lower byte of the stack pointer. Since the PUSHA instruction is simply a fast way of doing a PUSHF, and pushing WSR/IMASK1 and clearing IMASK1, a macro can be written to work around this problem.
5. The A/D converter differential non-linearity error becomes larger as V_{in} approaches V_{ref}. This results in the potential for missed codes at 10-bit resolution.
6. The reset pin must have a rise time less than 4 state times. An External Schmitt trigger reset circuit is recommended. A capacitor only or RC circuit directly connected to the pin will not work reliably. If a bad reset occurs, the chip will lock-up. A good reset will cause the part to work correctly; the chip does not have to be powered on and off.

NOTE:

Instruction bugs 1, 2, and 4 may prevent high level language compilers from generating code which works correctly. If a problem is suspected, generate an assembler code output of the high level language and examine the listing for the above instructions. If any of the instructions are present, the code may have to be rewritten.

DIFFERENCES BETWEEN THE 80C196KA AND THE 8096BH

CONVERTING FROM OTHER MCS®-96 PRODUCTS TO THE 80C196KA

The following list of suggestions for designing an 8X9XBH system will yield a design that is easily converted to the 80C196KA.

1. Do not base critical timing loops on instruction or peripheral execution times.
2. Use equate statements to set all timing parameters, including the baud rate.
3. Do not base hardware timings on CLKOUT or XTAL1. The timings of the 80C196KA are different than those of the 8X9XBH, but they will function with standard ROM/EPROM/Peripheral type memory systems.
4. Make sure all inputs are tied high or low and not left floating.
5. On the 8X9XBH, the $\overline{WRL}/\overline{WR}$ and $\overline{WRH}/\overline{BHE}$ signals both go low for byte writes to odd addresses in 8-bit write strobe mode. On the 80C196KA, only the $\overline{WRH}/\overline{BHE}$ signal goes low for this type of operation.
6. Indexed and indirect operations relative to the stack pointer (SP) work differently on the 80C196KA than on the 8096. On the 8096, the address is calculated based on the un-updated version of the stack pointer. The 80C196KA uses the updated version. The offset for PUSH[SP], POP[SP], PUSH nn[SP] and POP nn[SP] instructions may need to be changed by a count of 2.

NEW FEATURE SUMMARY

CPU FEATURES

Divide by 2 instead of divide by 3 clock for 1.5X performance

Faster instructions, especially indexed/indirect data operations

2.33 μs 16 $\times$ 16 multiply with 12 MHz clock (was 6.25 μs)

Faster interrupt response (almost twice as fast)

Different Reset Sequence

Powerdown and Idle Modes

Clock Failure Detect

6 new instructions including Compare Long and Block Move

8 new interrupt vectors

PERIPHERAL FEATURES

SFR Window switching allows read-only registers to be written and vice-versa

Timer2 can count up and down by external selection

Timer2 has an independent capture register

HSO lines which transitioned are saved

HSO lines can be written directly

HSO has CAM Lock and CAM Clear commands

A to D has a selectable sample and hold and speed control

New Baud Rate values are needed for serial port, higher speeds possible in all modes

Double buffered serial port transmit register

Serial Port Receive Overrun and Framing Error Detection

PWM has a Divide-by-2 Prescaler