LTC1346

10Mbps DCE/DTE V.35 Transceiver

June 1995

FEATURES

- **Single Chip Provides Complete Differential Signal Interface for V.35 Port**
- **Drivers and Receivers Will Withstand Repeated ±10kV ESD Pulses**
- 10MBaud Transmission Rate
- Meets CCITT V.35 Specification
- **Operates from ±5V Supplies**
- Shutdown Mode Reduces I_{CC} to Below 1µA
- Selectable Transmitter and Receiver Configurations
- Transmitter Maintains High Impedance When Disabled, Shutdown or with Power Off
- Transmitters Are Short-Circuit Protected

APPLICATIONS

- Modems
- Telecommunications
- Data Routers

DESCRIPTION

The LTC®1346 is a single chip transceiver that provides the differential clock and data signals for a V.35 interface from ±5V supplies. Combined with an external resistor termination network and an LT®1134A RS232 transceiver for the control signals, the LTC1346 forms a complete low power DTE or DCE V.35 interface port.

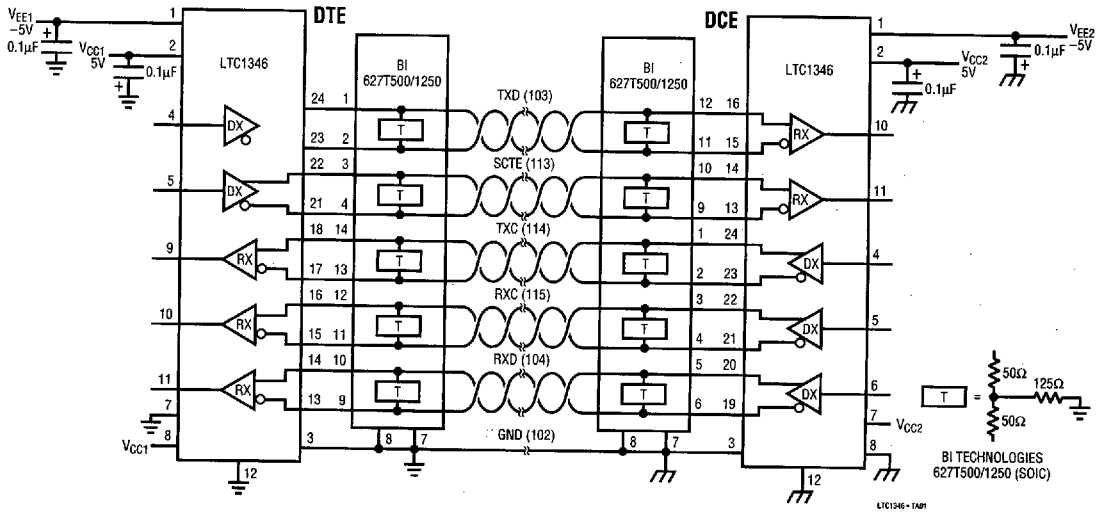
The LTC1346 features three current output differential transmitters and three differential receivers. The transceiver can be configured for DTE or DCE operation or Shutdown using two Select pins. In the Shutdown mode, the supply current is reduced to below 1µA.

The LTC1346 transceiver operates up to 10MBaud. All transmitters feature short-circuit protection and a Receiver Output Enable pin that allows the receiver outputs to be forced into a high impedance state. Both transmitter outputs and receiver inputs feature ±10kV ESD protection.

For single 5V applications that do not have –5V available, the LTC1345 provides the same functionality as the LTC1346 and includes an on-board –5V generator.

TYPICAL APPLICATION

Clock and Data Signals for V.35 Interface



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} 6.5V
- V_{EE} ..... −6.5V

Input Voltage
- Transmitters ..... −0.3V to (V_{CC} + 0.3V)
- Receivers ..... −18V to 18V
- S1, S2, $\overline{OE}$ ..... −0.3V to (V_{CC} + 0.3V)

Output Voltage
- Transmitters ..... −18V to 18V
- Receivers ..... −0.3V to (V_{CC} + 0.3V)

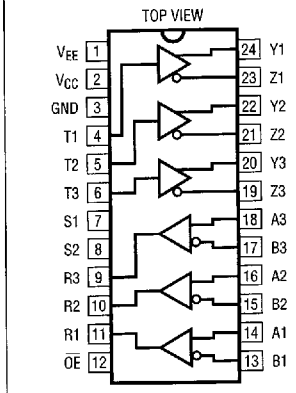
Short-Circuit Duration
- Transmitter Output ..... Indefinite
- Receiver Output ..... Indefinite

Operating Temperature Range
- Commercial ..... 0°C to 70°C
- Industrial ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



SW PACKAGE
24-LEAD PLASTIC SO WIDE

THREE V.35 TRANSMITTERS AND THREE RECEIVERS

T_{JMAX} = 150°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1346CSW
LTC1346ISW

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, V_{EE} = −5V ±5% (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD}	Transmitter Differential Output Voltage	−4V ≤ V_{OS} ≤ 4V (Figure 1)	●	0.44	0.55	0.66	V
V_{OC}	Transmitter Common-Mode Output Voltage	V_{OS} = 0V (Figure 1)	●	−0.6	0	0.6	V
I_{OH}	Transmitter Output High Current	$V_{Y, Z}$ = 0V	●	−12.6	−11	−9.4	mA
I_{OL}	Transmitter Output Low Current	$V_{Y, Z}$ = 0V	●	9.4	11	12.6	mA
I_{OZ}	Transmitter Output Leakage Current	−5V ≤ $V_{Y, Z}$ ≤ 5V, S1 = S2 = 0V	 ●		 ±1	±20 ±100	µA µA
R_O	Transmitter Output Impedance	−2V ≤ $V_{Y, Z}$ ≤ 2V			100		kΩ
V_{TH}	Differential Receiver Input Threshold Voltage	−7V ≤ (V_A + V_B)/2 ≤ 7V	●		25	200	mV
ΔV_{TH}	Receiver Input Hysterisis	−7V ≤ (V_A + V_B)/2 ≤ 7V			50		mV
I_{IN}	Receiver Input Current (A, B)	−7V ≤ $V_{A, B}$ ≤ 7V	●			0.4	mA
R_{IN}	Receiver Input Impedance	−7V ≤ $V_{A, B}$ ≤ 7V	●	17.5	30		kΩ
V_{OH}	Receiver Output High Voltage	I_O = 4mA, $V_{A, B}$ = 0.2V	●	3	4.5		V
V_{OL}	Receiver Output Low Voltage	I_O = 4mA, $V_{A, B}$ = −0.2V	●		0.2	0.4	V
I_{OSR}	Receiver Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	7	40	85	mA
I_{OZR}	Receiver Three-State Output Current	$\overline{OE}$ = V_{CC}, 0V ≤ V_O ≤ V_{CC}	●			±10	µA
V_{IH}	Logic Input High Voltage	T, S1, S2, $\overline{OE}$	●	2			V
V_{IL}	Logic Input Low Voltage	T, S1, S2, $\overline{OE}$	●			0.8	V
I_{IN}	Logic Input Current	T, S1, S2, $\overline{OE}$	●			±10	µA
I_{CC}	V_{CC} Supply Current	V_{OS} = 0V, S1 = S2 = HIGH (Figure 1) No Load, S1 = S2 = HIGH Shutdown, S1 = S2 = 0V, $\overline{OE}$ = V_{CC}			40 6 0.1		mA mA µA
I_{EE}	V_{EE} Supply Current	V_{OS} = 0V, S1 = S2 = HIGH (Figure 1) No Load, S1 = S2 = HIGH Shutdown, S1 = S2 = 0V, $\overline{OE}$ = V_{CC}			−40 −6 −0.1		mA mA µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, V_{EE} = −5V ±5% (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_R, t_F	Transmitter Rise or Fall Time	V_{OS} = 0V (Figures 1, 3)	●		7	40	ns
t_{PLH}	Transmitter Input to Output ↓	V_{OS} = 0V (Figures 1, 3)	●		25	70	ns
t_{PHL}	Transmitter Input to Output ↑	V_{OS} = 0V (Figures 1, 3)	●		30	70	ns
t_{SKEW}	Transmitter Output to Output	V_{OS} = 0V (Figures 1, 3)			5		ns
t_{PLH}	Receiver Input to Output ↓	V_{OS} = 0V (Figures 1, 4)	●		60	100	ns
t_{PHL}	Receiver Input to Output ↑	V_{OS} = 0V (Figures 1, 4)	●		65	100	ns
t_{SKEW}	Differential Receiver Skew, $\lvert t_{PLH} - t_{PHL} \rvert$	V_{OS} = 0V (Figures 1, 4)			5		ns
t_{ZL}	Receiver Enable to Output LOW	C_L = 15pF, SW1 Closed (Figures 2, 5)	●		40	70	ns
t_{ZH}	Receiver Enable to Output HIGH	C_L = 15pF, SW2 Closed (Figures 2, 5)	●		35	70	ns
t_{LZ}	Receiver Disable From LOW	C_L = 15pF, SW1 Closed (Figures 2, 5)	●		30	70	ns
t_{HZ}	Receiver Disable From HIGH	C_L = 15pF, SW2 Closed (Figures 2, 5)	●		35	70	ns
BR_{MAX}	Maximum Data Rate (Note 3)		●	10	15		MBaud

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are termed positive; all currents out of device pins are termed negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: Maximum data rate is specified for NRZ data encoding scheme. The maximum data rate may be different for other data encoding schemes. Data rate is guaranteed by a propagation delay test.

PIN FUNCTIONS

V_{EE} (Pin 1): Negative Supply, $-4.75V \geq V_{EE} \geq -5.25V$.

V_{CC} (Pin 2): Positive Supply, $4.75V \leq V_{CC} \leq 5.25V$.

GND (Pin 3): Ground.

T1 (Pin 4): Transmitter 1 Input.

T2 (Pin 5): Transmitter 2 Input.

T3 (Pin 6): Transmitter 3 Input.

S1 (Pin 7): Select Input 1.

S2 (Pin 8): Select Input 2.

R3 (Pin 9): Receiver 3 Output.

R2 (Pin 10): Receiver 2 Output.

R1 (Pin 11): Receiver 1 Output.

$\overline{OE}$ (Pin 12): Receiver Output Enable. To ensure shutdown mode, both S1 and S2 should be LOW and $\overline{OE}$ should be HIGH.

B1 (Pin 13): Receiver 1 Inverting Input.

A1 (Pin 14): Receiver 1 Noninverting Input.

B2 (Pin 15): Receiver 2 Inverting Input.

A2 (Pin 16): Receiver 2 Noninverting Input.

B3 (Pin 17): Receiver 3 Inverting Input.

A3 (Pin 18): Receiver 3 Noninverting Input.

Z3 (Pin 19): Transmitter 3 Inverting Output.

Y3 (Pin 20): Transmitter 3 Noninverting Output.

Z2 (Pin 21): Transmitter 2 Inverting Output.

Y2 (Pin 22): Transmitter 2 Noninverting Output

Z1 (Pin 23): Transmitter 1 Inverting Output.

Y1 (Pin 24): Transmitter 1 Noninverting Output.

13

FUNCTION TABLES

Transmitter and Receiver Configuration

S1	S2	TX#	RX#	REMARKS
0	0	—	—	All Shut Down*
1	0	1, 2, 3	1, 2	DCE Mode, RX3 Shut Down
0	1	1, 2	1, 2, 3	DTE Mode, TX3 Shut Down
1	1	1, 2, 3	1, 2, 3	All Active

Transmitter

	INPUTS				OUTPUTS			
CONFIGURATION	S1	S2	$\overline{OE}$	T	Y1 AND Y2	Z1 AND Z2	Y3	Z3
DTE	0	1	X	0	0	1	Z	Z
DTE	0	1	X	1	1	0	Z	Z
DCE or All ON	1	X	X	0	0	1	0	1
DCE or All ON	1	X	X	1	1	0	1	0
Shutdown*	0	0	1	X	Z	Z	Z	Z

Receiver

	INPUTS				OUTPUTS	
CONFIGURATION	S1	S2	$\overline{OE}$	A – B	R1 AND R2	R3
DTE or All ON	X	1	0	≥0.2V	1	1
DTE or All ON	X	1	0	≤–0.2V	0	0
DCE	1	0	0	≥0.2V	1	Z
DCE	1	0	0	≤–0.2V	0	Z
Disabled	X	X	1	X	Z	Z
Shutdown*	0	0	1	X	Z	Z

*To ensure shutdown mode, both S1 and S2 should be LOW and $\overline{OE}$ should be HIGH

TEST CIRCUITS

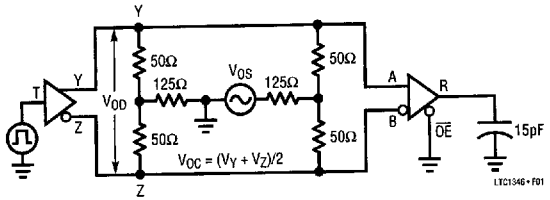


Figure 1. V.35 Transmitter/Receiver Test Circuit

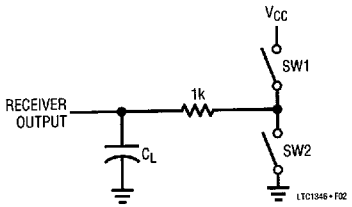


Figure 2. Receiver Output Enable and Disable Timing Test Load

SWITCHING TIME WAVEFORMS

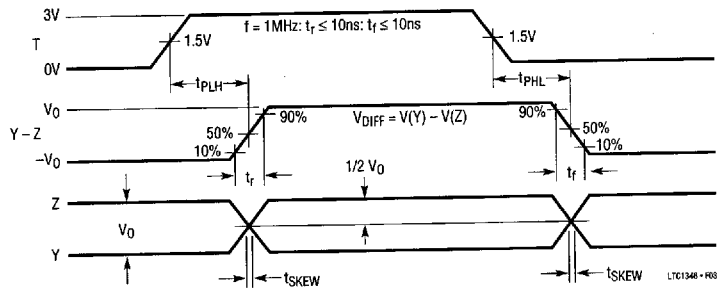


Figure 3. V.35 Transmitter Propagation Delays

SWITCHING TIME WAVEFORMS

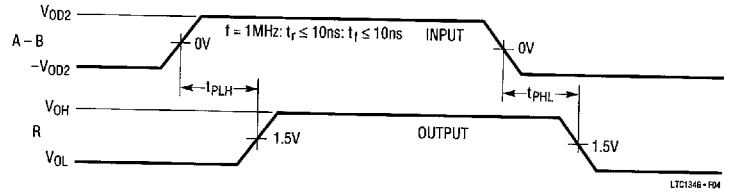


Figure 4. V.35 Receiver Propagation Delays

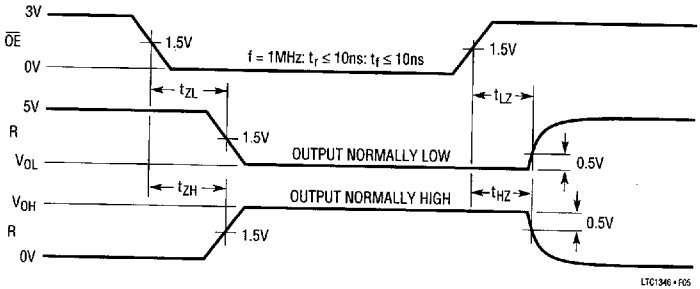


Figure 5. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Review of CCITT Recommendation V.35 Electrical Specifications

V.35 is a CCITT recommendation for synchronous data transmission via modems. Appendix 2 of the recommendation describes the electrical specifications which are summarized below:

1. The interface cable is a balanced twisted-pair with 80Ω to 120Ω impedance.
2. The transmitter's source impedance is between 50Ω and 150Ω.
3. The transmitter's resistance between shorted terminals and ground is 150Ω ±15Ω.
4. When terminated by a 100Ω resistive load, the terminal-to-terminal voltage should be 0.55V ±20%.
5. The transmitter's rise time should be less than 1% of the signal pulse or 40ns, whichever is greater.
6. The common-mode voltage at the transmitter output should not exceed 0.6V.
7. The receiver impedance is 100Ω ±10Ω.
8. The receiver impedance to ground is 150Ω ±15Ω.
9. The transmitter or receiver should not be damaged by connection to earth ground, short-circuiting, or cross connection to other lines.
10. No data errors should occur with ±2V common-mode change at either the transmitter or receiver, or ±4V ground potential difference between transmitter and receiver.

Cable Termination

Each end of the cable connected to an LTC1346 must be terminated by an external Y or Δ resistor network for proper operation. The Y-termination has two series connected 50Ω resistors and a 125Ω resistor connected between ground and the center tap of the two 50Ω resistors as shown in Figure 6.

13

APPLICATIONS INFORMATION

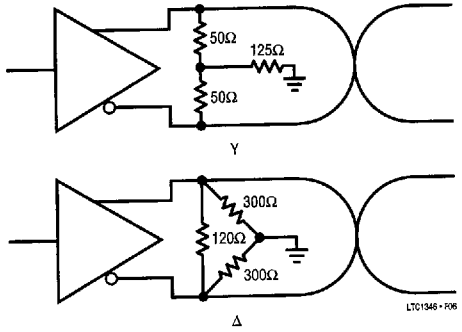


Figure 6. Y and Δ Termination Networks

The alternative Δ-termination has a 120Ω resistor across the twisted wires and two 300Ω resistors between each wire and ground. Standard 1/8W, 5% surface mount resistors can be used for the termination network. To maintain the proper differential output swing, the resistor tolerance must be 5% or less. A termination network that combines all the resistors into an 14-pin SO package is available from:

BI Technologies (Formerly Beckman Industrial)
Resistor Networks
4200 Bonita Place
Fullerton, CA 92635
Phone: (714) 447-2357
FAX: (714) 447-2500
Part #: BI Technologies 627T500/1250 (SO)
899TR50/125 (DIP)

Theory of Operation

The transmitter output consists of complementary switched-current sources as shown in Figure 7.

With a logic zero at the transmitter input, the inverting output Z sources 11mA and the noninverting output Y sinks 11mA. The differential transmitter output voltage is then set by the termination resistors. With two differential 50Ω resistors at each end of the cable, the voltage is set to (50Ω × 11mA) = 0.55V. With a logic 1 at the transmitter input, output Z sinks 11mA and Y sources 11mA. The common-mode voltage of Y and Z is 0V when both current sources are matched and there is no ground potential

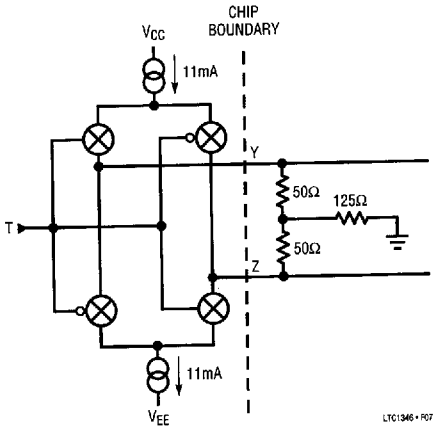


Figure 7. Simplified Transmitter Schematic

difference between the cable terminations. The transmitter current sources have a common-mode range of ±2V, which allows for a ground difference between cable terminations of ±4V.

Each receiver input has a 30k resistance to ground and requires external termination to meet the V.35 input impedance specification. The receivers have an input hysteresis of 50mV to improve noise immunity. The receiver output may be forced into a high impedance state by pulling the output enable ($\overline{OE}$) pin HIGH. For normal operation $\overline{OE}$ should be pulled LOW.

Two Select pins, S1 and S2, configure the chip for DTE, DCE, all transmitter and receivers ON, or Shutdown. To ensure shutdown mode, both S1 and S2 should be LOW and $\overline{OE}$ should be HIGH. In Shutdown mode, I_{CC} drops to 1μA. The outputs of the transmitters and receivers are in high impedance states.

Complete V.35 Port

Figure 8 shows the schematic of a complete surface mounted, single 5V DTE and DCE V.35 port using only three ICs and six capacitors per port. The LTC1346 is used to transmit the clock and data signals, and the LT1134A to transmit the control signals. If test signals 140, 141, and 142 are not used, the transmitter inputs should be tied to V_{CC}.

APPLICATIONS INFORMATION

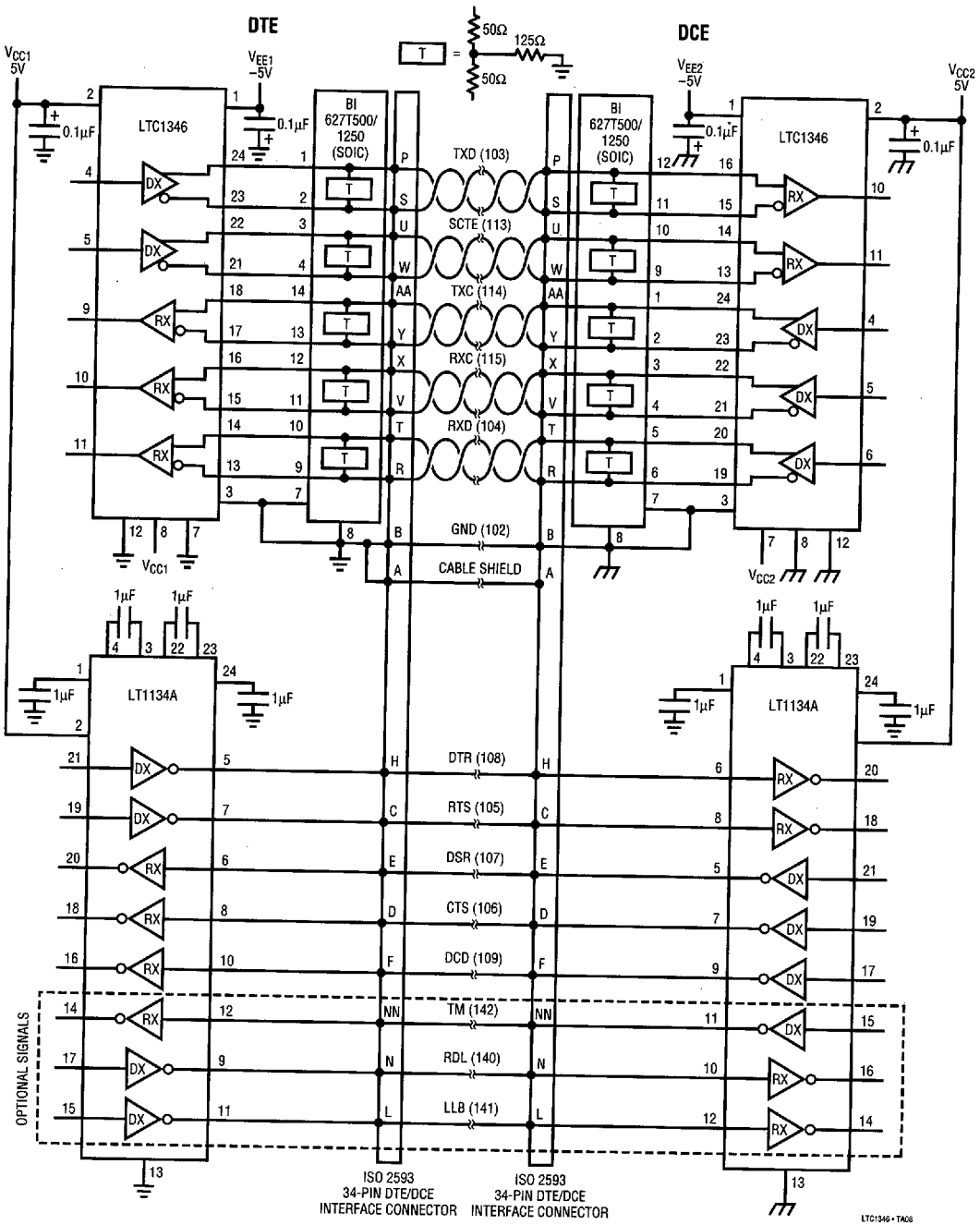


Figure 8. Complete ±5V V.35 Interface

APPLICATIONS INFORMATION

RS422/RS485 Applications

The receivers on the LTC1346 are ideal for RS422 and RS485 applications. Using the test circuit in Figure 9, the LTC1346 receivers are able to successfully reconstruct the data stream with the common-mode voltage meeting RS422 and RS485 requirements (12V to –7V).

Figures 10 and 11 show that the LTC1346 receivers are very capable of reconstructing data at frequencies up to 10MHz.

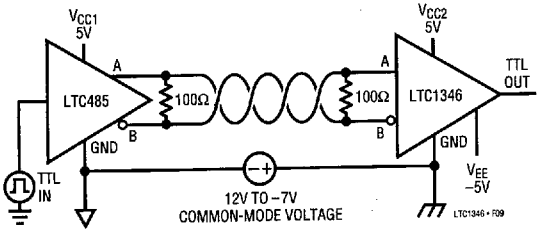


Figure 9 RS422/RS485 Receiver Interface

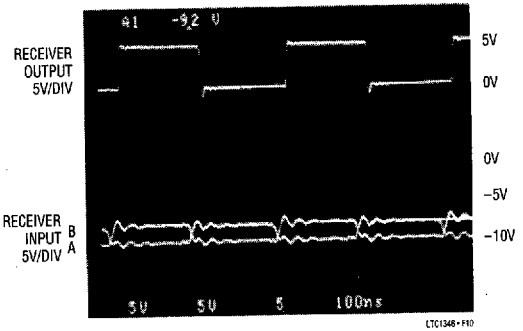


Figure 10. –7V Common Mode

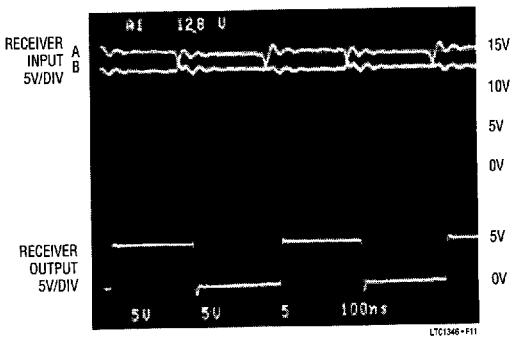


Figure 11. 12V Common Mode

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1345	Single Supply V.35 Transceiver	Requires Only Single 5V Power