T-47-13

Standard-Performance TTL Delay Modules

Available as 5- or 10-tap standard-DIP or 5-tap half-DIP modules, these LTTLDL low-profile delay modules offer good performance *not* commensurate with their low cost. All are available as surface-DIP.

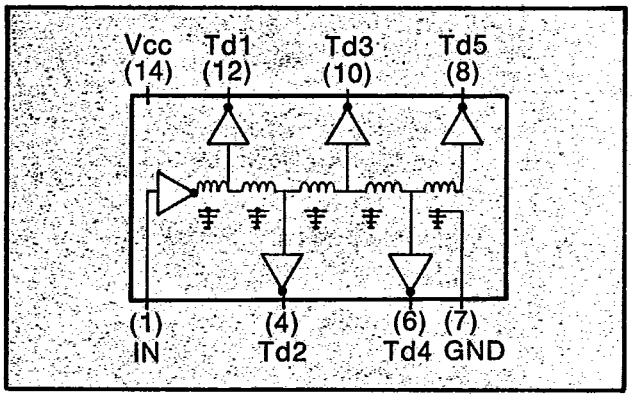
- **±2 ns or ±5% delay tolerance (whichever is greater) @ 25 °C.**
- **Temperature coefficient ±2 ns or ±4% (whichever is greater) at maximum delay, 0 to 70 °C.**
- **Minimum input-pulse width 40% of total delay.**
- **5 to 500 ns delays available.**
- **For Schottky TTL, TTL, LSTTL, AS, ALS and FAST logic circuits.**
- **Transfer-molded—reliable.**
- **Pin compatible to 74/54 series 14-pin DIP.**
- **Auto-insertable.**
- **Trailing-edge timing available.**
- **Fanout: Logic 1—20 loads; logic 0—10 loads.**

STANDARD-PERFORMANCE 5-TAP TTL DELAY MODULES

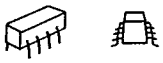
- Standard size (excluding leads)— 0.8″ L × 0.3″ W × 0.25″ H.
- Five equal taps in 20% increments of total delay.

Part No.	NANOSECONDS					All Taps (Max.)	
	T_D1	T_D2	T_D3	T_D4	T_D5	T_R+	T_R-
LTTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
LTTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
LTTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
LTTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	5.0
LTTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	6.0
LTTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	7.0
LTTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	8.0
LTTLDL250	50.0	100.0	150.0	200.0	250.0	2.0	9.0
LTTLDL500	100.0	200.0	300.0	400.0	500.0	2.0	9.0

Delay Characteristics measured at V_{cc} = 5.0V, 25°C no load.
Delay Tolerance ±2 ns or 5% whichever is greater.



Available in these packages:



For dimensions, see drawings 2 and 2A, on page 22.

Available in these logics:

TTL · FAST CMOS · FAST · ALSTTL · Schottky TTL · LSTTL · ASTTL

STANDARD-PERFORMANCE 10-TAP TTL DELAY MODULES

- Ten equal taps in 10% increments of total delay.

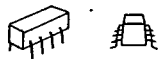
Part No.	NANOSECONDS										All Taps (Max.)	
[1]	T_D1	T_D2	T_D3	T_D4	T_D5	T_D6	T_D7	T_D8	T_D9	T_D10	T_R+	T_R-
LTTLDD050	5.0	10.0	15.0	20.0	25.0	30.0	35.0	40.0	45.0	50.0	2.0	2.0
LTTLDD075	7.5	15.0	22.5	30.0	37.5	45.0	52.5	60.0	67.5	75.0	2.0	2.0
LTTLDD100	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0	2.0	2.0
LTTLDD125	12.5	25.0	37.5	50.0	62.5	75.0	87.5	100.0	112.5	125.0	2.0	2.0
LTTLDD150	15.0	30.0	45.0	60.0	75.0	90.0	105.0	120.0	135.0	150.0	2.0	5.0
LTTLDD200	20.0	40.0	60.0	80.0	100.0	120.0	140.0	160.0	180.0	200.0	2.0	5.0
LTTLDD250	25.0	50.0	75.0	100.0	125.0	150.0	175.0	200.0	225.0	250.0	2.0	5.0
LTTLDD500	50.0	100.0	150.0	200.0	250.0	300.0	350.0	400.0	450.0	500.0	2.0	9.0

Delay Characteristics @ V_{cc} = 5.0 V., 25°C. no load
Delay Tolerance ±2.0 ns or 5% whichever is greater
[1] Add Suffix "A" for Non-Standard Pinout per Schematic

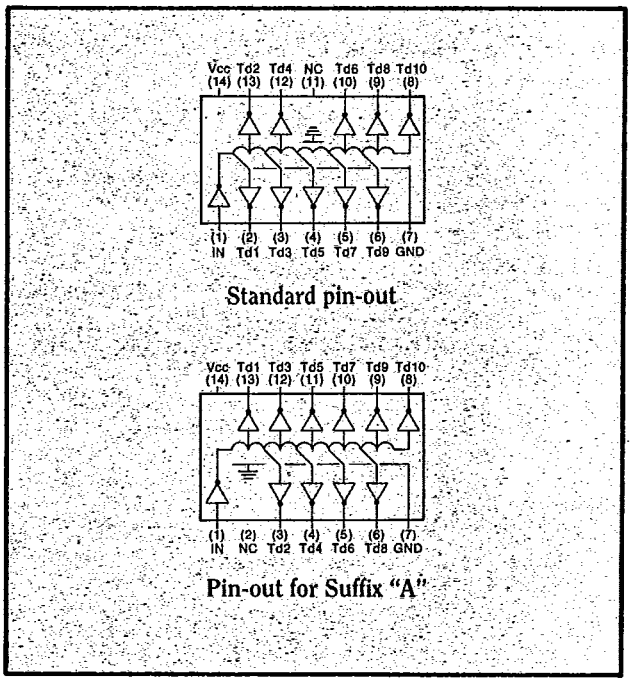
Higher performance characteristics than those noted in general specifications (page 10) available in the following areas:

- temperature coefficient of total delay (2%)
- minimum input-pulse width to total delay (20%)

Available in these packages:



For dimensions, see drawings 2 and 2A, page 22.



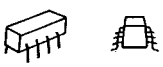
STANDARD-PERFORMANCE COMPACT TTL DELAY MODULES

- Compact size (excluding leads)—
  0.5" L × 0.3" W × 0.25" H.
- Five equal taps in 20% increments of total delay.

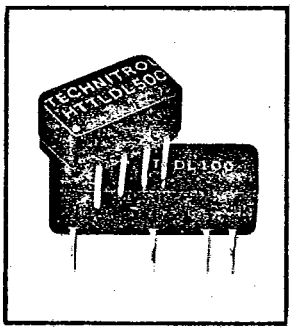
Part No.	NANOSECONDS					All Taps (Max.)	
	T_D1	T_D2	T_D3	T_D4	T_D5	T_R+	T_R-
HTTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
HTTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
HTTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
HTTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	5.0
HTTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	6.0
HTTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	7.0
HTTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	8.0
HTTLDL250	50.0	100.0	150.0	200.0	250.0	2.0	9.0
HTTLDL500	100.0	200.0	300.0	400.0	500.0	2.0	9.0

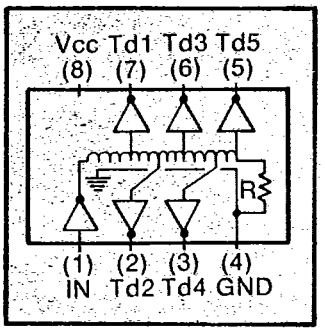
Delay Characteristics measured at V_{cc} = 5.0V, 25°C no load.
Delay Tolerance ±2 ns or 5% whichever is greater.

Available in these packages:



For dimensions, see drawings 3 and 3A, on page 22.





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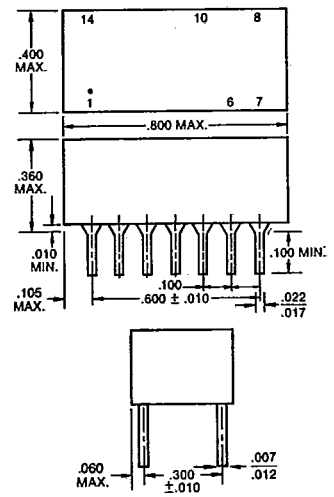
Dimensions

Numbers of the drawings below are referenced in the catalog at the locations describing specific modules. One drawing may be referenced by two, three, or more modules. Only the pins specified in the applicable schematic are provided with each package.

Pin numbers shown are for identification only, and are not necessarily marked on unit.

T-50-23

1



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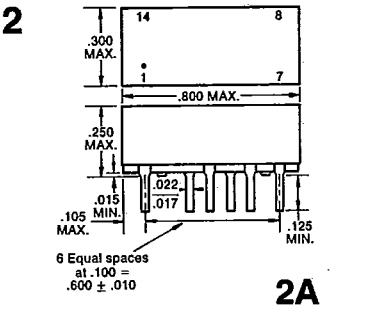
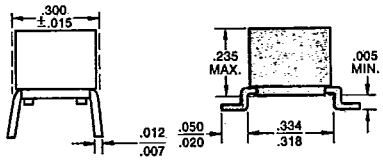


2A



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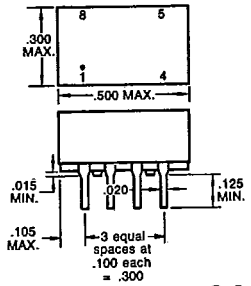
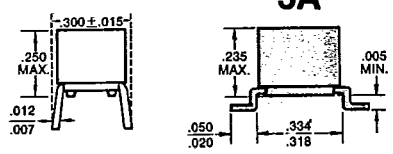


3A



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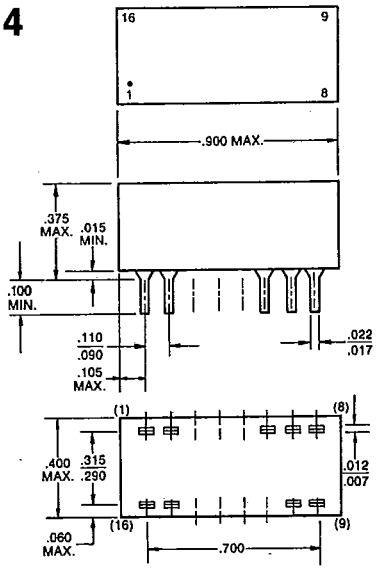

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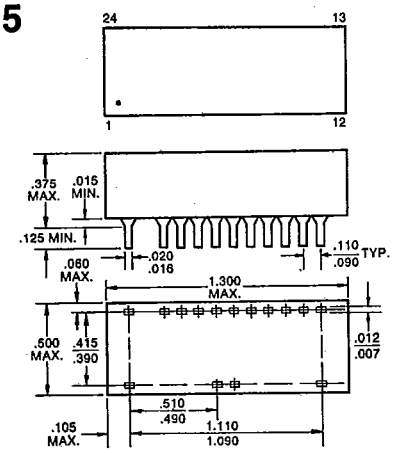
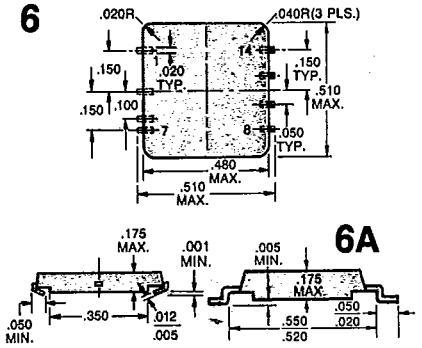
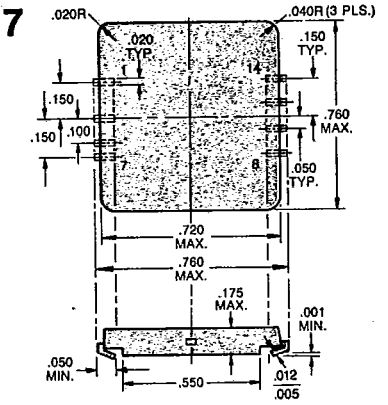


6

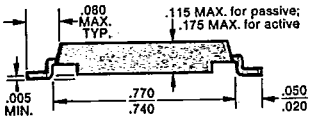


6A

7



7A



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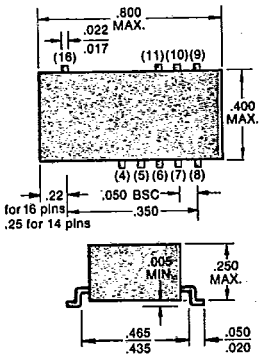

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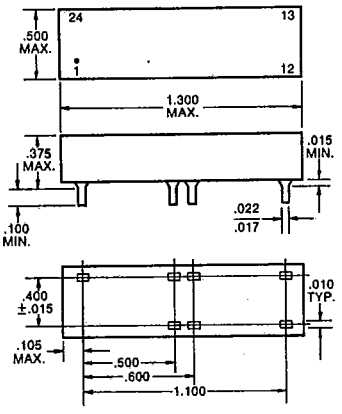
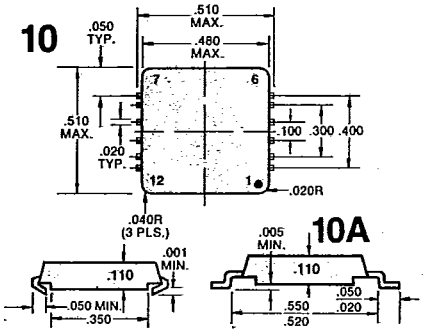


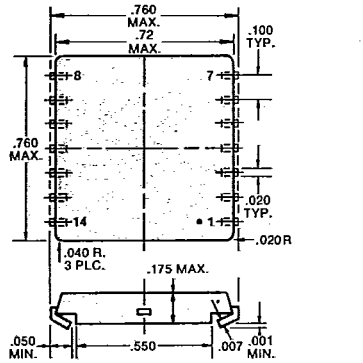
Surface-mount models are shown in shaded color.

10

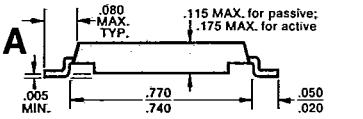


10A

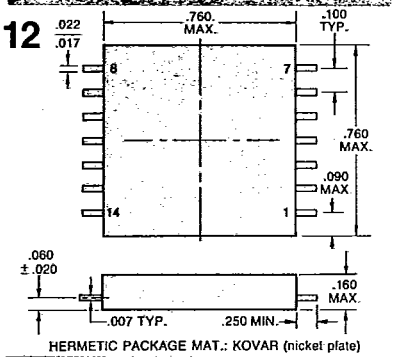
11



11A

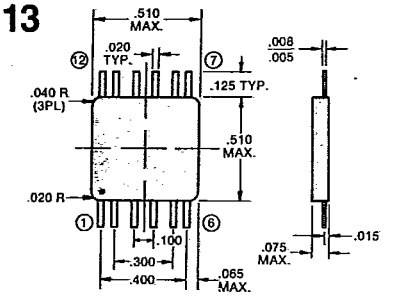


12



HERMETIC PACKAGE MAT.: KOVAR (nickel plate)

13



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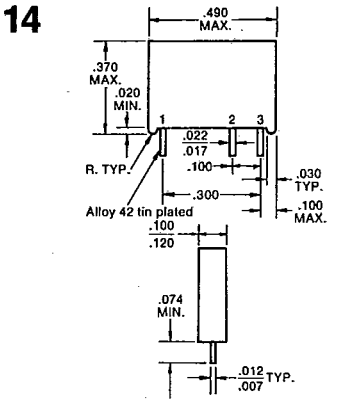

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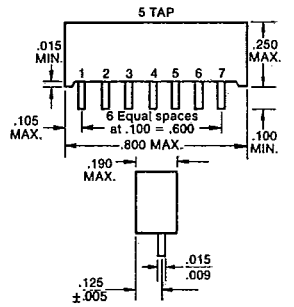
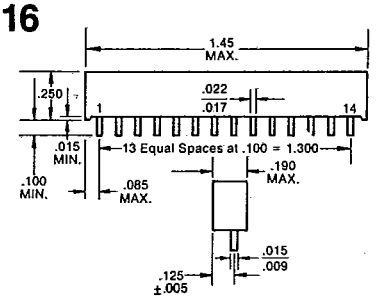


16



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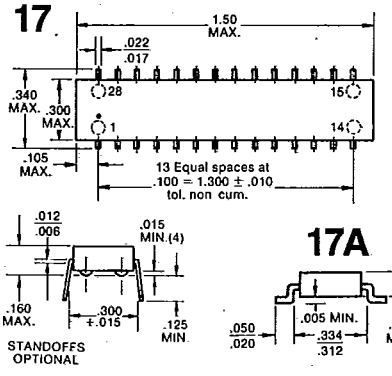
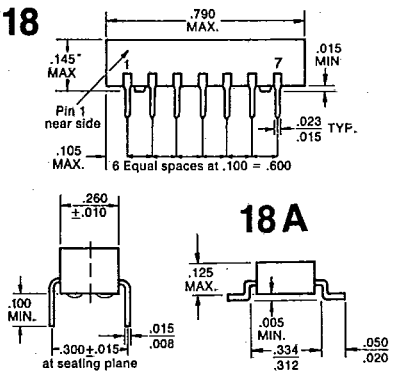


17A

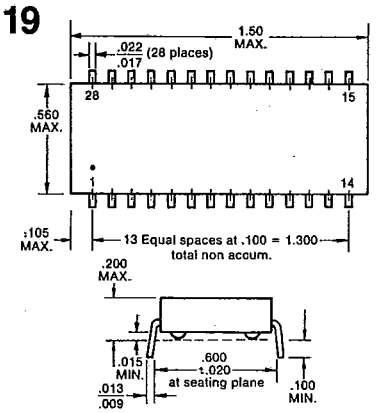
18



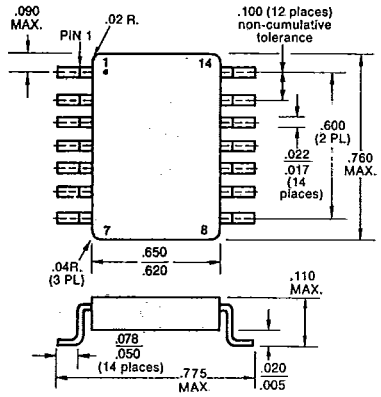
18A

*For delays above 200 ns, height is .200 MAX.

19



20



Can be used for ceramic-substrate applications.

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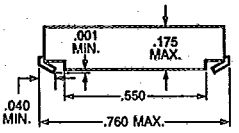
High-Performance 5-Tap TTL Delay Modules—¾" Sq.

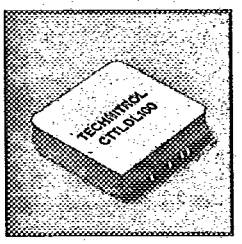
High-Performance Surface-Mount TTL Delay Modules

Part No.	NANOSECONDS					All Taps (Max.)	
	T_D1	T_D2	T_D3	T_D4	T_D5	T_R+	T_R-
CTTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
CTTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
CTTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
CTTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	5.0
CTTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	5.0
CTTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	6.0
CTTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	7.0

Delay Characteristics measured @ V_{CC} = 5.0V, 25°C no load.
Delay Tolerance ±2 ns or 5% (whichever is greater).
Minimum Input-pulse width 20% of total delay.

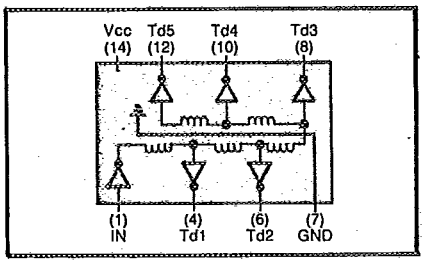
C-Lead CTTLDL

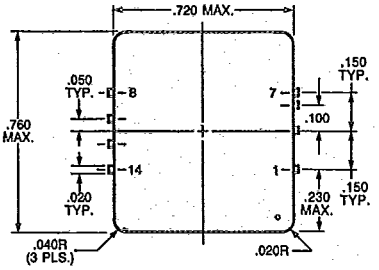




Actual Size

Schematic and Pin-Out for CTTLDL



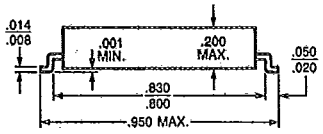


High-Performance Hermetic 5-Tap TTL Delay Modules—¾" Sq.

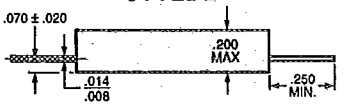
Part No.	Part No.	NANOSECONDS					All Taps (Max.)	
		T_D1	T_D2	T_D3	T_D4	T_D5	T_R+	T_R-
GJTTLDL025	JTTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
GJTTLDL050	JTTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
GJTTLDL075	JTTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
GJTTLDL100	JTTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	5.0
GJTTLDL125	JTTLDL125	25.0	50.0	75.0	100.0	125 0	2.0	6.0
GJTTLDL150	JTTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	7.0
GJTTLDL200	JTTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	8.0

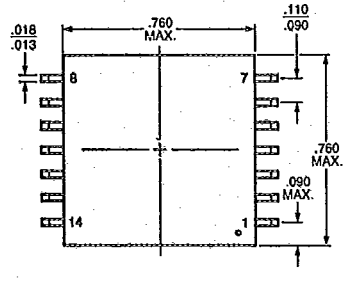
Delay Characteristics measured @ V_{CC} = 5.0V, 25°C no load.
Delay Tolerance ±2 ns or 5% (whichever is greater).
Minimum input-pulse width 40% of total delay.

Hermetic Gull Wing GJTTLDL

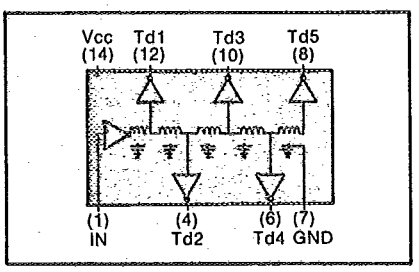


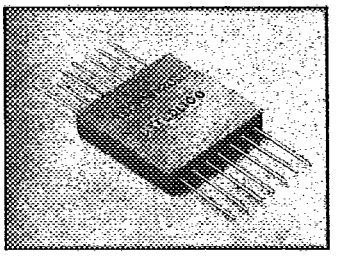
Hermetic Flat-Pack JTTLDL





Schematic and Pin-Out for GJTTLDL and JTTLDL





Actual Size

Lead material: electro tin plated (alloy 42)
Note: Pin numbers shown are for reference only and not necessarily marked on unit.

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