



## DESCRIPTION

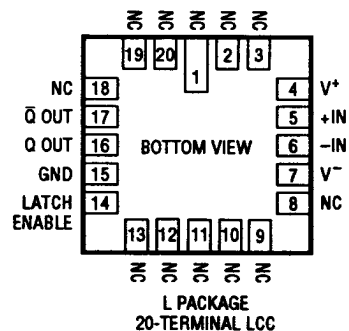
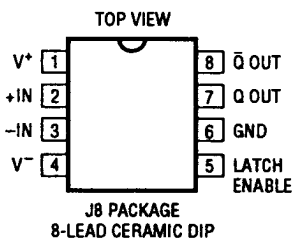
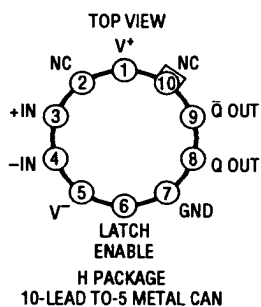
The LT1016M/883 is an ultra fast (10ns) comparator specifically designed to interface directly to TTL logic while operating off either a dual  $\pm 5V$  supply or a single 5V supply. Tight offset voltage specifications and high gain allow the LT1016M/883 to be used in precision applications. Matched complementary outputs further extend the versatility of this new comparator.

The device is processed to the requirements of MIL-STD-883 Class B to yield circuits usable in precision military applications.

## ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (Note 4)	7V
Negative Supply Voltage	-7V
Differential Input Voltage	±5V
Input Voltage (Either Input)	Equal to Supplies
Latch Pin Voltage	Equal to Supplies
Output Current (Continuous)	±20mA
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

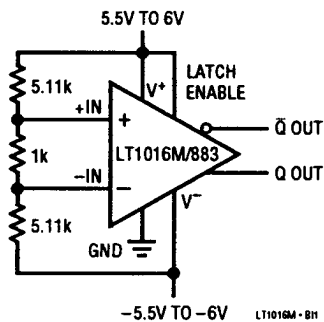
## PACKAGE/ORDER INFORMATION



ORDER PART NUMBER	PART MARKINGS†	ORDER PART NUMBER	PART MARKINGS†	ORDER PART NUMBER	PART MARKINGS†
LT1016MH/833	LT1016MH/833C	LT1016MJ8/833	LT1016MJ8/833C	LT1016ML/833	LT1016ML/833C

† The suffix letter "C" of the part mark indicates compliance per MIL-STD-883, para 1.2.1.1.

## BURN-IN CIRCUIT



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of circuits as described herein will not infringe on existing patent rights.

**TABLE 1: ELECTRICAL CHARACTERISTICS**

$V^+ = 5V$ ,  $V^- = 5V$ ,  $V_{OUT}(Q) = 1.4V$ ,  $V_{LATCH} = 0V$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ C$			SUB-GROUP	$-55^\circ C \leq T_A \leq 125^\circ C$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
$V_{OS}$	Input Offset Voltage	$R_S \leq 100\Omega$	1			$\pm 2$	1			$\pm 3$	2,3	mV
$I_{OS}$	Input Offset Current		1			1	1			1.3	2,3	$\mu A$
$I_B$	Input Bias Current		2			10	1			13	2,3	$\mu A$
	Input Voltage Range	Single 5V Supply	5	-3.75		3.5	1	-3.75		3.5	2,3	V
				1.25		3.5	1	1.25		3.5	2,3	V
CMRR	Common-Mode Rejection Ratio	$-3.75 \leq V_{CM} \leq 3.5V$		80			1	80			2,3	dB
PSRR	Power Supply Rejection Ratio	+Supply $4.6 \leq V^+ \leq 5.4V$ -Supply $-7V \leq V^- \leq -2V$	4 4	54 80			1 1	54 80			2,3 2,3	dB dB
$A_V$	Small-Signal Voltage Gain	$1V \leq V_{OUT} \leq 2V$		1400			4					V/V
$V_{OH}$	Output High Voltage	$V^+ \leq 4.6V$ $I_{OUT} = 1mA$ $I_{OUT} = 10mA$		2.7 2.4			1 1	2.7 2.4			2,3 2,3	V V
$V_{OL}$	Output Low Voltage	$I_{SINK} = 4mA$				0.5	1			0.5	2,3	V
$I^+$	Positive Supply Current					35	1			35	2,3	mA
$I^-$	Negative Supply Current					5	1			5	2,3	mA
$V_{IH}$	Latch Pin High Input Voltage			2			1	2			2,3	V
$V_{IL}$	Latch Pin Low Input Voltage					0.8	1			0.8	2,3	V
$I_{IL}$	Latch Pin Current	$V_{LATCH} = 0V$				500	1			500	2,3	$\mu A$
$t_{PD}$	Propagation Delay	$\Delta V_{IN} = 100mV$ , $OD = 5mV$ $\Delta V_{IN} = 100mV$ , $OD = 20mV$	3,6 6			14 12				16 15		ns ns
$\Delta t_{PD}$	Differential Propagation Delay	$\Delta V_{IN} = 100mV$ , $OD = 5mV$	6			3				3		ns

**Note 1:** Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

**Note 2:** Input bias current ( $I_B$ ) is defined as the average of the two input currents.

**Note 3:** Propagation delay is measured with the overdrive added to actual  $V_{OS}$ . Units are sample tested only.

**Note 4:** Electrical specifications apply only up to 5.4V.

**Note 5:** See the LT1016 data sheet for a discussion of input voltage range for supplies other than  $\pm 5V$  or 5V.

**Note 6:** Guaranteed by design, characterization, or correlation to other tested parameters.

**TABLE 2: ELECTRICAL TEST REQUIREMENTS**

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4
Group A Test Requirements (Method 5005)	1,2,3,4
Group C and D End Point Electrical Parameters (Method 5005)	1

\* PDA Applies to subgroup 1. See PDA Test Notes.

**PDA Test Notes**

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

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