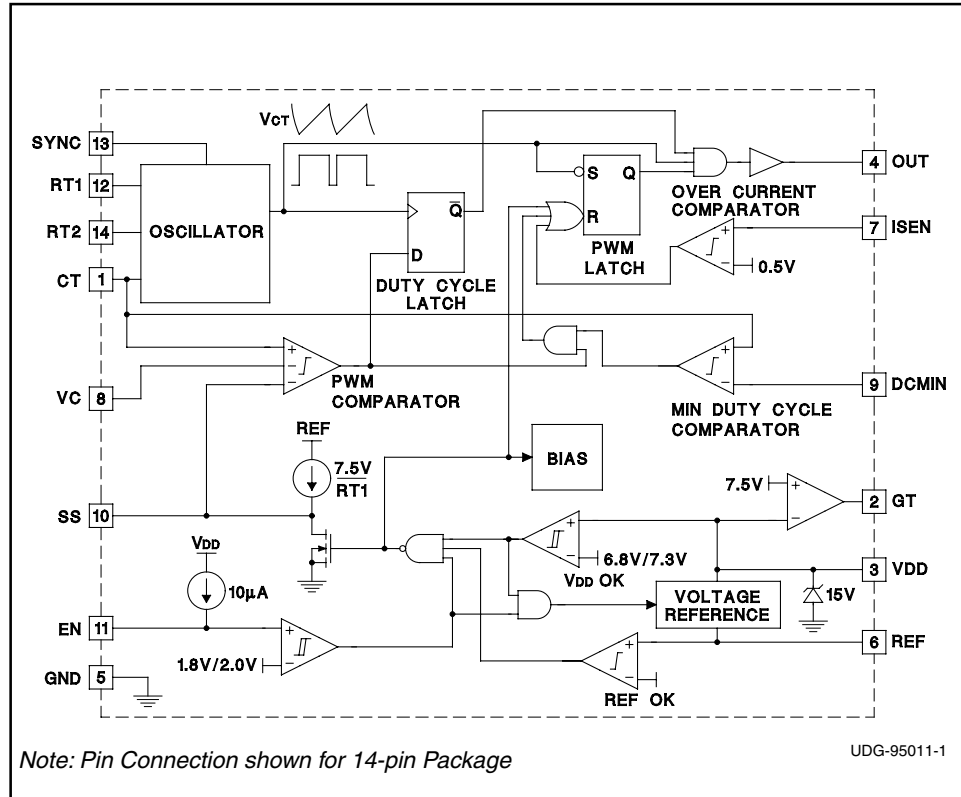


# Micropower Voltage Mode PWM

## FEATURES

- Low 85 $\mu$ A Startup Current
- Low 300 $\mu$ A Operating Current
- Automatically Disabled Startup Preregulator
- Programmable Minimum Duty Cycle with Cycle Skipping
- Programmable Maximum Duty Cycle
- Output Current 1A Peak Source and Sink
- Programmable Soft Start
- Programmable Oscillator Frequency
- External Oscillator Synchronization Capability

## BLOCK DIAGRAM



## DESCRIPTION

The UCC3581 voltage mode pulse width modulator is designed to control low power isolated DC - DC converters in applications such as Subscriber Line Power (ISDN I.430). Primarily used for single switch forward and flyback converters, the UCC3581 features BiCMOS circuitry for low startup and operating current, while maintaining the ability to drive power MOSFETs at frequencies up to 100kHz. The UCC3581 oscillator allows the flexibility to program both the frequency and the maximum duty cycle with two resistors and a capacitor. A TTL level input is also provided to allow synchronization to an external frequency source.

The UCC3581 includes programmable soft start circuitry, overcurrent detection, a 7.5V linear preregulator to control chip VDD during startup, and an on-board 4.0V logic supply.

The UCC3581 provides functions to maximize light load efficiency that are not normally found in PWM controllers.

A linear preregulator driver in conjunction with an external depletion mode N-MOSFET provides initial controller power. Once the bootstrap supply is functional, the preregulator is shut down to conserve power. During light load, power is saved by providing a programmable minimum duty cycle clamp. When a duty cycle below the minimum is called for, the modulator skips cycles to provide the correct average duty cycle required for output regulation. This effectively reduces the switching frequency, saving significant gate drive and power stage losses.

The UCC3581 is available in 14-pin plastic and ceramic dual-in-line packages and in a 14-pin narrow body small outline IC package (SOIC). The UCC1581 is specified for operation from -55°C to +125°C, the UCC2581 is specified for operation from -40°C to +85°C, and the UCC3581 is specified for operation from 0°C to +70°C.

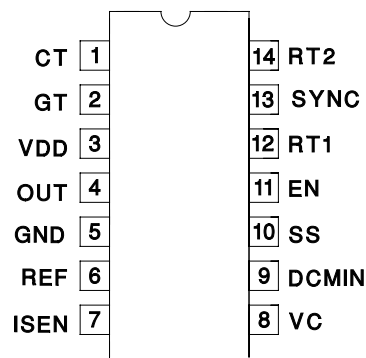
## ABSOLUTE MAXIMUM RATINGS

|   |                                      |
|---|--------------------------------------|
| Supply Voltage ( $I_{DD} \leq 10\text{mA}$ )  | 15V                                  |
| Supply Current                                | 30mA                                 |
| $V_{REF}$ Current                             | -10mA                                |
| OUT Current                                   | $\pm 1\text{A}$                      |
| Analog Inputs                                 |                                      |
| EN  | -0.3V to ( $V_{DD} + 0.3\text{V}$ )  |
| VC, ISEN, SYNC, DCMIN                         | -0.3V to ( $V_{REF} + 0.3\text{V}$ ) |
| Power Dissipation at $T_D = 25^\circ\text{C}$ |                                      |
| (N, J, Q, L Package)                          | 1W                                   |
| (D Package)                                   | 0.65W                                |
| Storage Temperature                           | -65°C to +150°C                      |
| Junction Temperature                          | -55°C to +150°C                      |
| Lead Temperature (Soldering, 10 sec.)         | +300°C                               |

Unless otherwise specified, all voltages are with respect to Ground. Currents positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## CONNECTION DIAGRAMS

DIL-14, SOIC-14 (Top View)  
N or J, D Packages



## ORDERING INFORMATION

|          | TEMPERATURE RANGE | PACKAGE |
|----------|-------------------|---------|
| UCC1581J | -55°C to +125°C   | CDIP    |
| UCC2581D | -40°C to +85°C    | SOIC    |
| UCC2581N | -40°C to +85°C    | PDIP    |
| UCC3581D | 0°C to +70°C      | SOIC    |
| UCC3581N | 0°C to +70°C      | PDIP    |

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $V_{DD} = 10\text{V}$ , 0.1 $\mu\text{F}$  capacitor from VDD to GND, 1.0 $\mu\text{F}$  capacitor from REF to GND,  $RT1 = 680\text{k}\Omega$ ,  $RT2 = 12\text{k}\Omega$ ,  $CT = 750\text{pF}$  and  $T_A = T_J$ .

| PARAMETER                             | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNITS |
|---------------------------------------|--|------|------|------|-------|
| <b>Reference Section</b>              |  |      |      |      |       |
| Output Voltage                        | $I = -0.2\text{mA}$  | 3.94 | 4.0  | 4.06 | V     |
| Load Regulation                       | $-5.0\text{mA} < I < -0.2\text{mA}$                            |      | 10   | 30   | mV    |
| <b>Undervoltage Lockout Section</b>   |  |      |      |      |       |
| Start Threshold                       |  | 6.7  | 7.3  | 7.9  | V     |
| Minimum Operating Voltage After Start |  | 6.2  | 6.8  | 7.4  | V     |
| Hysteresis                            |  | 0.2  | 0.5  | 0.8  | V     |
| <b>Linear Preregulator Section</b>    |  |      |      |      |       |
| Regulated VDD Voltage                 |  | 7.0  | 7.5  | 8.0  | V     |
| Regulated VDD to UVLO Delta           |  | 100  | 230  | 600  | mV    |
| VDD Override Threshold                |  |      |      | 8.2  | V     |
| <b>Oscillator Section</b>             |  |      |      |      |       |
| Frequency                             | 25°C   | 18   | 19.5 | 21   | kHz   |
| Temperature Stability                 | (Note 1)   |      | 3.0  |      | %     |
| CT Peak Voltage                       | (Note 1)   |      | 2.5  |      | V     |
| CT Valley Voltage                     | (Note 1)   |      | 1.0  |      | V     |
| SYNC VIH                              |  | 1.9  | 2.1  | 2.3  | V     |
| SYNC VIL                              | (Note 1)   |      | 1.8  |      | V     |
| <b>PWM SECTION</b>                    |  |      |      |      |       |
| Maximum Duty Cycle                    |  | 81   | 84   | 87   | %     |
| Minimum Duty Cycle                    | ( $VC < 1.0\text{V}$ ) $DCMIN = 0\text{V}$                     |      |      | 0    | %     |
|                                       | ( $VC > 1.0\text{V}$ at start of cycle) $DCMIN = 1.18\text{V}$ | 7    | 10   | 13   | %     |
| Input Bias Current                    | ( $DCMIN$ ), (Note 1)  | -150 | 20   | 150  | nA    |
|                                       | (VC), (Note 1)   | -150 | 20   | 150  | nA    |

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for VDD = 10V, 0.1μF capacitor from VDD to GND, 1.0μF capacitor from REF to GND, RT1 = 680kΩ, RT2 = 12kΩ, CT = 750pF and TA = TJ.

| PARAMETER                    | TEST CONDITIONS       | MIN  | TYP   | MAX  | UNITS |
|------------------------------|-----------------------|------|-------|------|-------|
| <b>Current Sense Section</b> |                       |      |       |      |       |
| Input Bias Current           |                       | –150 | 20    | 150  | nA    |
| Overcurrent Threshold        |                       | 0.4  | 0.5   | 0.6  | V     |
| <b>Output Section</b>        |                       |      |       |      |       |
| OUT Low Level                | I = 100mA             |      | 0.6   | 1.2  | V     |
| OUT High Level               | I = –100mA, VDD – OUT |      | 0.6   | 1.2  | V     |
| Rise/Fall Time               | (Note 1)              |      | 20    | 100  | ns    |
| <b>Soft start Section</b>    |                       |      |       |      |       |
| Soft start Current           | SS = 2V               | –9   | –11.5 | –14  | μA    |
| <b>Chip Enable Section</b>   |                       |      |       |      |       |
| VIH                          |                       | 1.9  | 2.0   | 2.1  | V     |
| VIL                          |                       | 1.7  | 1.8   | 1.9  | V     |
| Hysteresis                   |                       | 180  | 230   | 280  | mV    |
| Source Current               |                       | 5    | 10    | 15   | μA    |
| <b>Overall Section</b>       |                       |      |       |      |       |
| Start-Up Current             | VDD < Start Threshold |      | 85    | 130  | μA    |
| Operating Supply Current     | VC = 0V               |      | 300   | 600  | μA    |
| VDD Zener Shunt Voltage      | IDD = 10mA            | 13.5 | 15    | 16.5 | V     |
| IDD Stand-by Shunt Voltage   | EN = 0V               |      | 100   | 150  | μA    |

Note 1: Guaranteed by design. Not 100% tested in production

## PIN DESCRIPTIONS

**CT:** Oscillator timing capacitor pin. Minimum value is 100pF.

**DCMIN:** Input for programming minimum duty cycle where pulse skipping begins. This pin can be grounded to disable minimum duty cycle feature and pulse skipping.

**EN:** Enable input. This pin has an internal 10μA pull-up. A logic low input inhibits the PWM output and causes the soft start capacitor to be discharged.

**GND:** Circuit ground.

**GT:** Pin for controlling the gate of an external depletion mode N-MOSFET for the startup supply. The external N-MOSFET regulates VDD to 7.5V until the bootstrap supply comes up, then GT goes low.

**ISEN:** Input for overcurrent comparator. This function can be used for pulse-by-pulse current limiting. The threshold is 0.5V nominal.

**OUT:** Gate drive output to external N-MOSFET.

**REF:** 4.0V reference output. A minimum value bypass capacitor of 1.0μF is required for stability.

**RT1:** Resistor pin to program oscillator charging current.

The oscillator charging current is  $9.2 \cdot \left( \frac{2.0V}{RT1} \right)$ .

See Application Diagram Fig. 1.

The current into this pin is  $\left( \frac{2.0V}{RT1} \right)$ .

The value of RT1 should be between 220k and 1MΩ

**RT2:** Resistor pin to program oscillator discharge time. The minimum value of RT2 is 10kΩ See Application Diagram Fig. 1.

**SS:** Soft start capacitor pin. The charging current out of SS is 3.75X the current in RT1.

**SYNC:** Oscillator synchronization pin. Rising edge triggered CMOS/TTL compatible input with a 2.1V threshold. SYNC should be grounded if not used. The minimum pulse width of the SYNC signal is 100ns.

**VC:** Control voltage input to PWM comparator. The nominal control range of VC is 1.0V to 2.5V.

**VDD:** Chip input power with an 15V internal clamp. VDD is regulated by startup FET to 7.5V until the bootstrap voltage comes up. VDD should be bypassed at the chip with a 0.1μF minimum capacitor.

## APPLICATION INFORMATION

The UCC3581's oscillator allows the user the flexibility to program the frequency and the duty cycle by adjusting two resistors and a capacitor. Application Diagram Fig. 1 shows these components as RT1, RT2, and CT. RT1 programs the timing capacitor charging current which results in a linear ramp charging CT. Discharge of CT is accomplished through RT2 which results in a standard RC discharge waveform. The oscillator on-time (CT charging) is calculated by the formula

$$t_{ON} = 0.082 \cdot RT1 \cdot C_T$$

The off-time (CT discharging) is calculated by the formula

$$t_{OFF} = 0.95 \cdot RT2 \cdot C_T$$

Resistor RT1 programs the charging current. The current is:

$$\frac{2.0V}{RT1}$$

CT charging current is 9.2 times the current in RT1. RT1 can range from 220kΩ to 1MΩ. Minimum capacitor size is 100pF, and minimum RT2 size is 10k.

A Block Diagram of the Oscillator is shown in Fig. 2. The oscillator also has an external synchronization pin. When a low to high level is detected, and if the oscillator's output is in the high state (CT charging), the oscillator output immediately goes low and CT starts discharging. The sync input is rising edge sensitive and is ignored when the oscillator output is low.

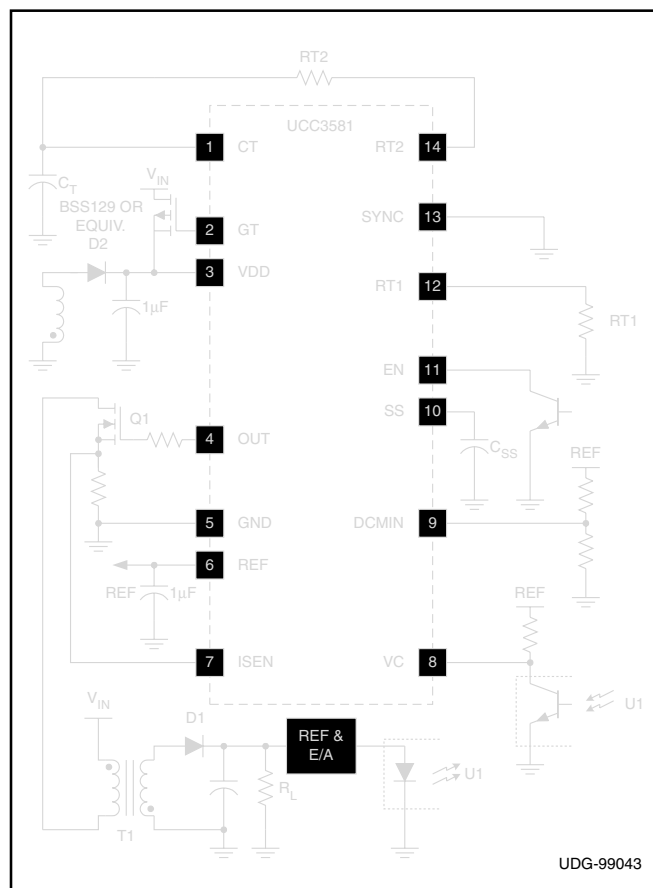


Figure 1. Application diagram.

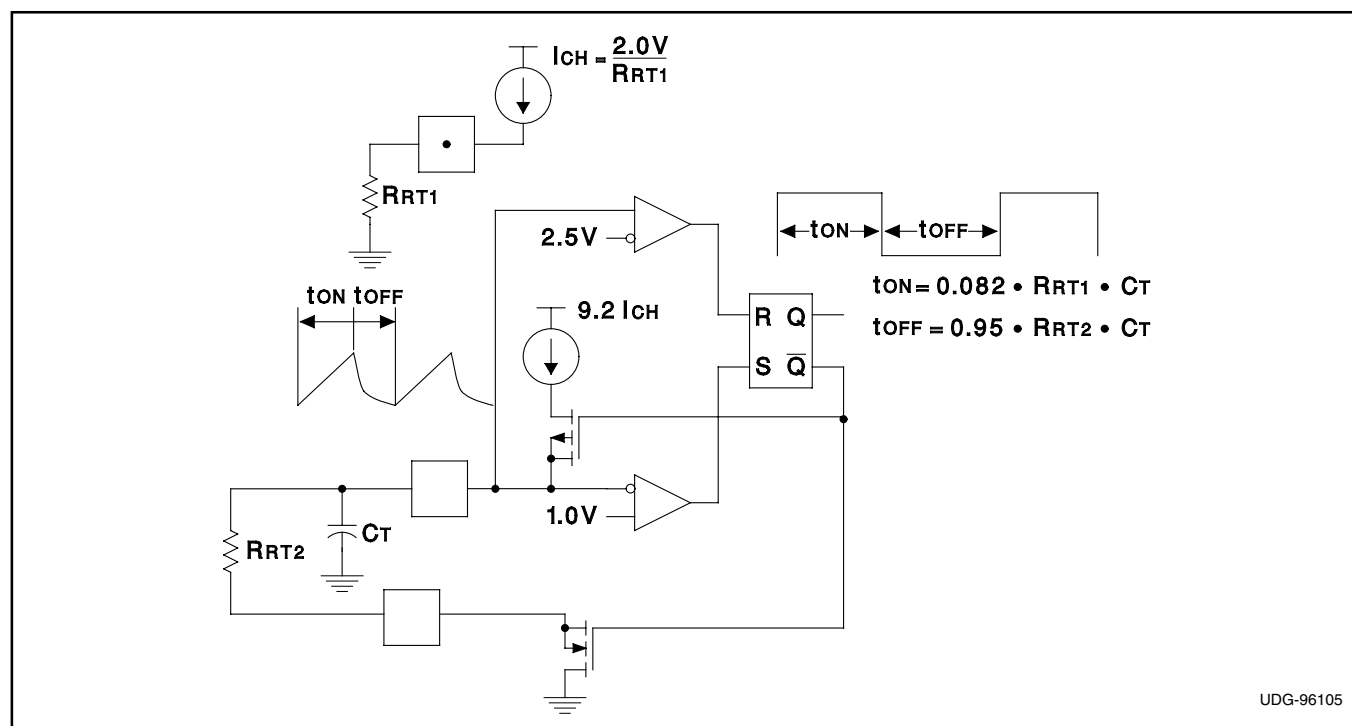


Figure 2. Oscillator.

## APPLICATION INFORMATION (cont.)

The externally bypassed 4.0V reference is controlled by undervoltage lockout and chip enable circuitry. The enable input is internally tied to a 10μA current source which allows the pin to be driven by an open collector driver. The part is also enabled if EN floats. The UCC3581 has a soft start function which requires a user supplied external timing capacitor. When in soft start mode, the soft start capacitor, C<sub>SS</sub>, is charged with a constant current source. The soft start current is 3.75X the current in RT1.

There is an on-chip control amplifier, which when driving the gate of an external depletion mode N-MOSFET, acts as a 7.5V linear preregulator supplying VDD directly from the primary input power line. The preregulator may subsequently be fully disabled by a tertiary bootstrap winding providing a minimum of 8.2V to the VDD pin.

### Computation of DCMIN

DCMIN for a given duty cycle is calculated as follows:

$$\Delta V = i_{OSC} \cdot DC \cdot \frac{(t_{ON} + t_{OFF})}{C_T}$$

where:

- $i$  = oscillator charge current = 9.2 . (2.0V/RT1)
- DC = Duty Cycle, as a fraction of 1
- $t_{ON} = 0.082 \cdot RT1 \cdot CT$
- $t_{OFF} = 0.95 \cdot RT2 \cdot CT$
- $C_T$  = Oscillator Capacitor

The CT pin ramp slews from 1V to 2.5V. Therefore, add ΔV to 1V to get DCMIN voltage.

Example: For 10% duty cycle with RT1 = 680kΩ, RT2 = 12kΩ, and CT = 705pF,

$$\Delta V = i_{OSC} \cdot DC \cdot \frac{(t_{ON} + t_{OFF})}{C_T}$$

$$= \frac{9.2 \cdot \left( \frac{2.0V}{680k} \right) \cdot (0.1) \cdot 4.182 \cdot 10^{-5} \text{ sec} + 8.55 \cdot 10^{-6} \text{ sec}}{750 \cdot 10^{-12}}$$

$$\Delta V = 0.18V$$

Therefore,

$$DCMIN = 1V + 0.18V = 1.18V$$

### A Typical Micropower Application

The circuit shown in Fig. 3 illustrates the use of the UCC3581 in a micropower application. The isolated 5V flyback power supply uses a minimum of parts and operates over an 8:1 input voltage range (15VDC to 120VDC) while delivering a regulated 5V output with a load swing from 0W to 1W. It operates in the discontinuous mode at light load or high line, and continuous mode at heavier loads and lower line voltages. Higher input line voltages are possible by simply increasing the voltage ratings of C1, Q1, D1 and D2.

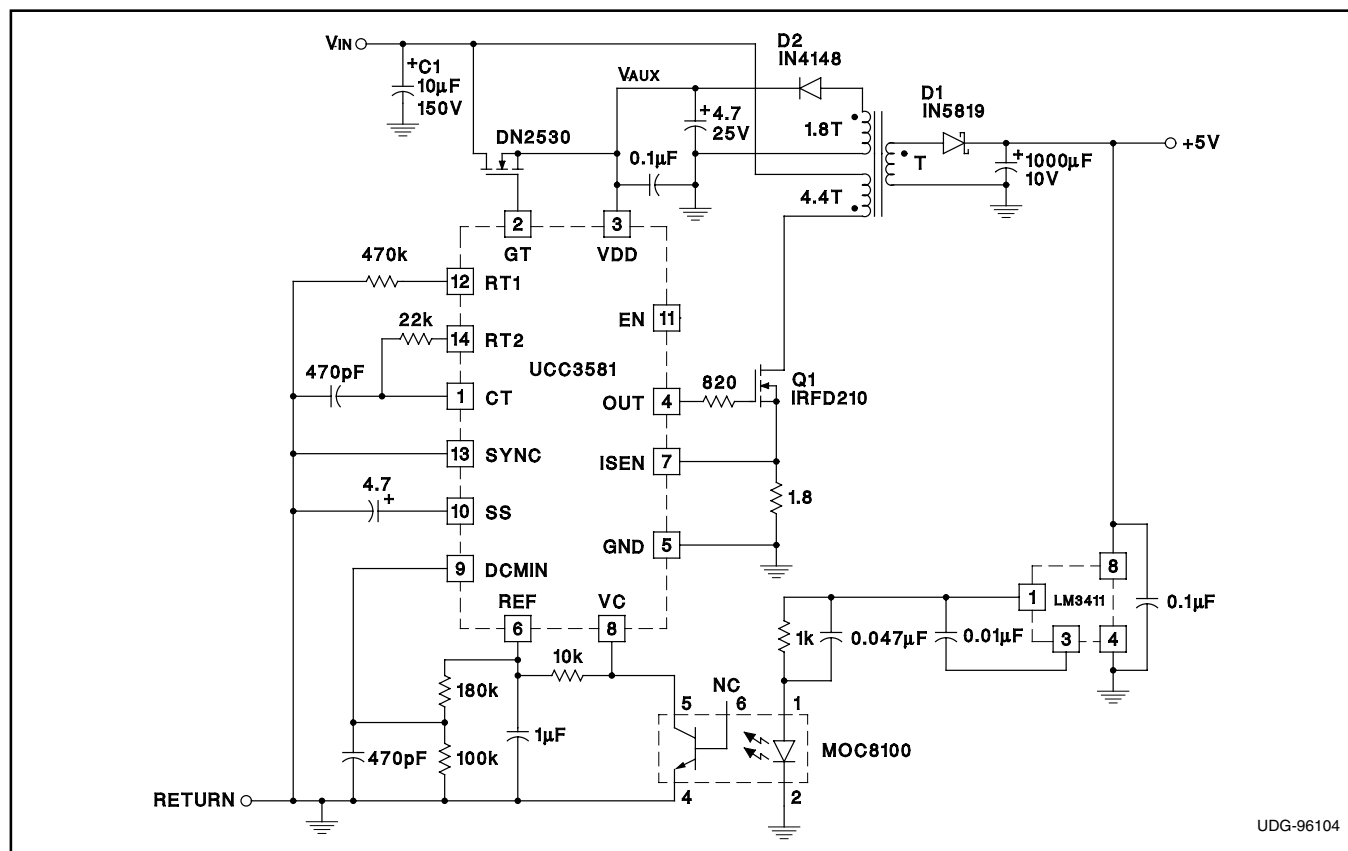
The most notable feature of the design is its efficiency. With a load of 1 watt, the typical efficiency is 82%, dropping to 70% around 50mW. With a load of only 12.5mW, the efficiency remains as high as 50%. At this load, with an input of 50V, the total input current is only 500μA. Note that the power supply can be disabled by pulling the UCC3581 enable pin low, in which case the input current drops to less than 150μA.

The UCC3581 achieves very low losses by means of low quiescent current and pulse skipping at light loads which reduces switching losses. The degree of pulse skipping is controlled by programming the minimum duty cycle. In this example, the frequency is 35kHz at maximum load and drops to <2kHz at 12.5mW load (minimum pulse width of around 6μsec, or 21% duty cycle at 35kHz). Another way losses are reduced is operating with a VDD of around 10V rather than the more common 12V to 16V. At such light primary currents, the MOSFET remains in full saturation with a gate drive voltage well below 10V.

Gate drive losses are minimized by choosing a MOSFET with low total gate charge, in this case only 8nC maximum. By choosing a large gate drive resistor, EMI is minimized by reducing peak currents. Due to pulse skipping, switching times are less critical for efficiency at light load.

The shunt regulator (LM3411) and optocoupler (MOC8100) are also key to the efficiency at such light loads, and were chosen for their low operating current. The LM3411 has a quiescent current of only 150μA maximum (compared to 1mA for the more common TL431). In addition, because it is not a three terminal device, the LM3411's quiescent current does not flow in the optocoupler LED. Since this bias current is not in the feedback control path, a higher value pull-up resistor can be used on the optocoupler output transistor, further re-

## TYPICAL APPLICATION



UDG-96104

Figure 3. Micropower power supply with 50% efficiency at 12.5mW load.

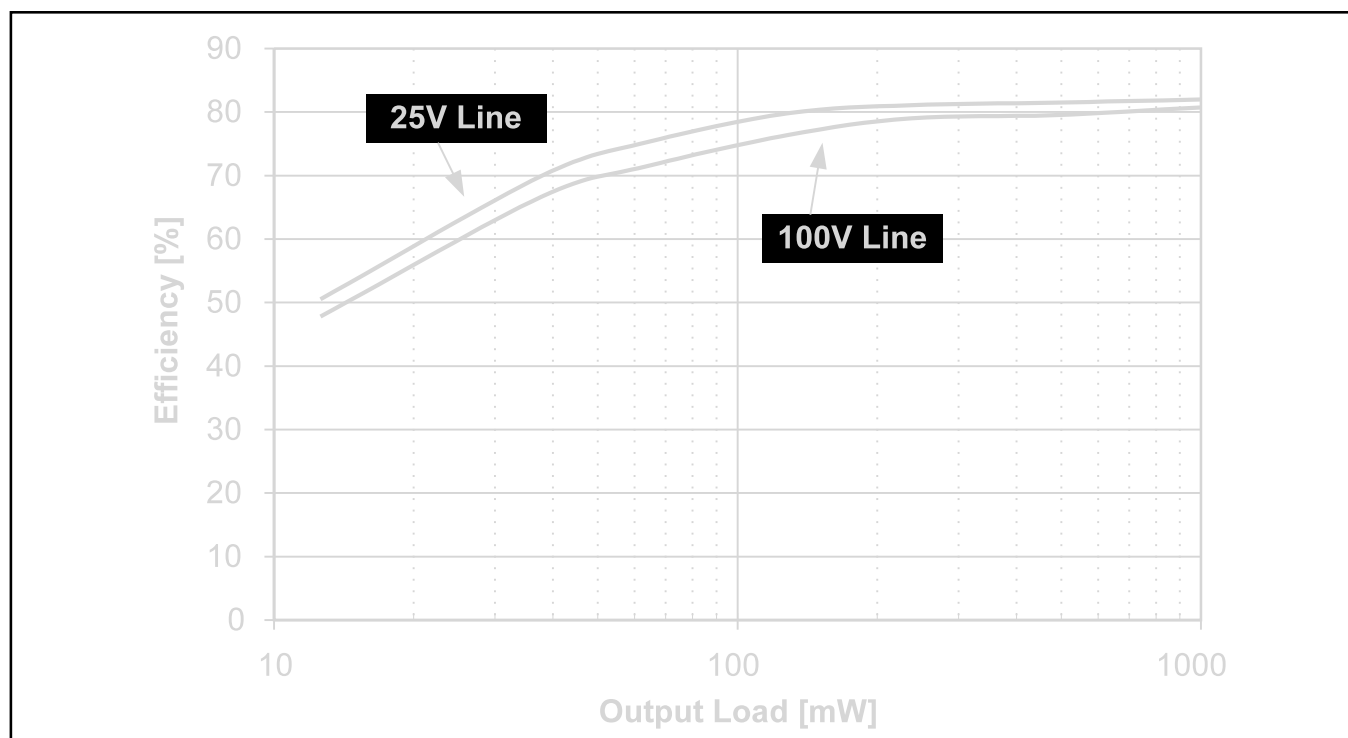


Figure 4. UCC3581 efficiency vs. line and load.

## APPLICATION INFORMATION (cont.)

ducing losses.

A rather large soft start capacitor was chosen to give a startup time of several hundred milliseconds, reducing the input surge current while the output is coming up.

Note that for stability, the UCC3581 VREF bypass capacitor needs to be at least 1 $\mu$ F. The VDD supply also needs some capacitance to hold it up between pulses at light load and high line, where the frequency may drop to less than 1kHz due to pulse skipping. Otherwise it may drop low enough for the startup MOSFET to be biased on, lowering efficiency.

If the sync input is used, it should not be left in a high impedance state where noise could cause false triggering. If unused, it should be grounded.

The transformer was designed with a standard Magnetics RM8 ferrite core using P material, gapped for an AL of 1600mH/1000Turn<sup>2</sup>. The primary consists of 44 turns, while the 5V secondary has 10 turns and the bootstrap winding 18 turns. For simplicity, all the windings can be #28 AWG. A two section bobbin was used to provide high primary to secondary isolation. A much smaller design, with reduced isolation, could have been done for this low

## TYPICAL CHARACTERISTIC CURVES

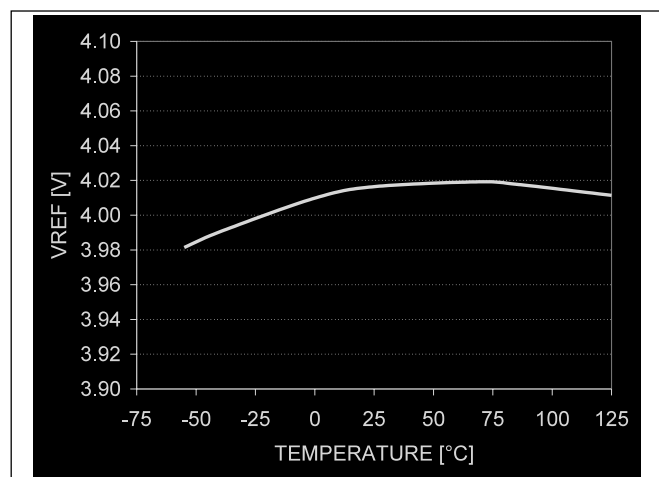


Figure 5. Reference voltage vs. temperature.

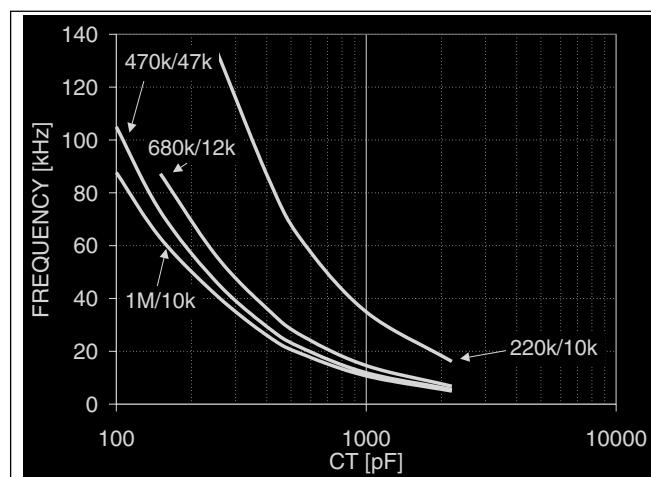


Figure 6. Frequency vs. CT vs. RT1 and RT2.

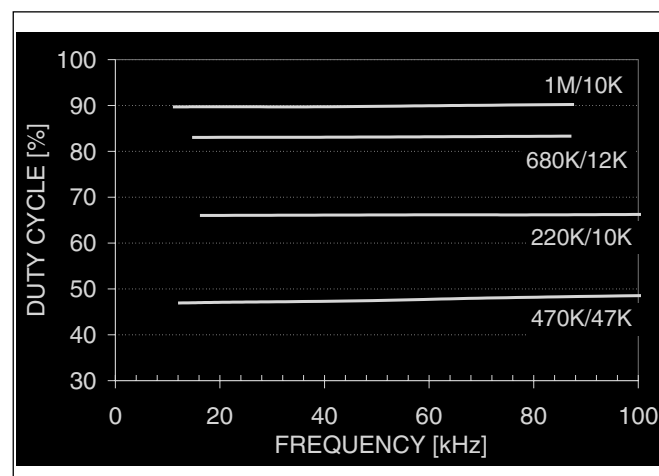


Figure 7. Duty cycle vs. frequency vs. RT1 / RT2.

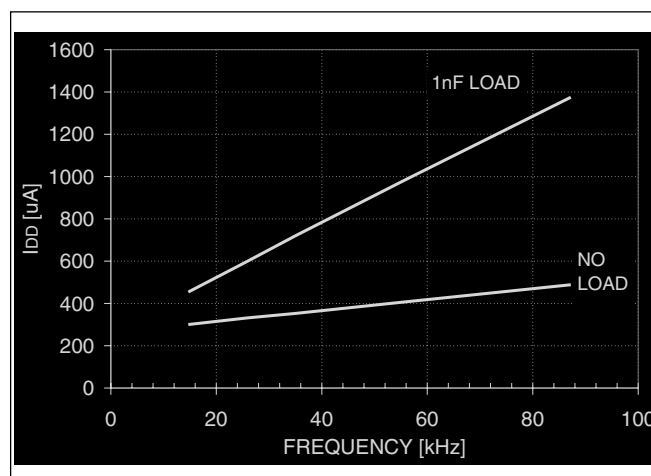
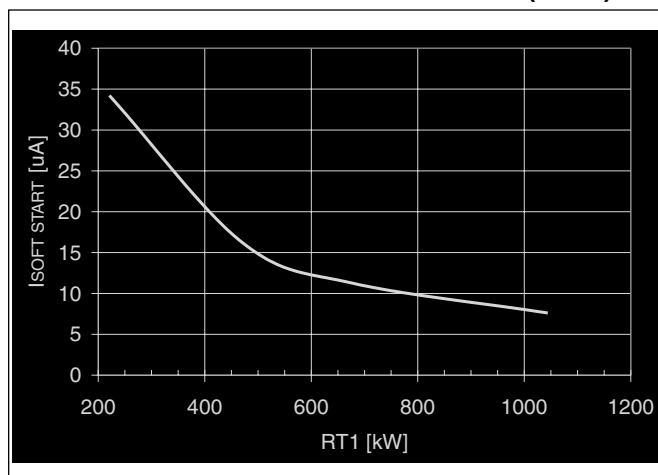


Figure 8.  $I_{DD}$  vs. frequency RT1 = 680k, RT2 = 12k.

**TYPICAL CHARACTERISTIC CURVES (cont.)**



**Figure 9. Soft start current vs. RT1.**



## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.