

Features

- Fast Read Access Time - 85 ns
- Unregulated Battery Power Supply Range, 2.7 V to 3.6 V
- Compatible with JEDEC Standard AT27C020
- Low Power CMOS Operation
 - 20 μ A max. Standby
 - 29 mW max. Active at 5 MHz for $V_{CC} = 3.6$ V
- Wide Selection of JEDEC Standard Packages
 - 32-Lead 600-mil PDIP and Cerdip
 - 32-Pad PLCC and LCC
 - 32-Lead TSOP
- High Reliability CMOS Technology
 - 2,000 V ESD Protection
 - 200 mA Latchup Immunity
- Rapid Programming - 100 μ s/byte (typical)
- Two-Line Control
- CMOS and TTL Compatible Inputs and Outputs
 - JEDEC Standard for LVTTL and LVBO
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27BV020 chip is a high performance, low power, low voltage 2,097,152 bit ultraviolet erasable and electrically programmable read only memory (EPROM) organized as 256K by 8 bits. It requires only one supply in the range of 2.7 to 3.6 V in normal read mode operation, making it ideal for fast, portable systems using either regulated or unregulated battery power.

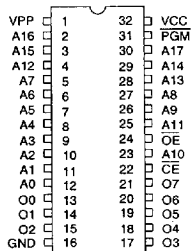
Atmel's innovative design techniques provide fast speeds that rival 5-V parts while keeping the low power consumption of a 3-V supply. At $V_{CC} = 2.7$ V, any byte can be accessed in less than 85 ns. With a typical power draw of only 18 mW at 5 MHz and $V_{CC} = 3$ V, the AT27BV020 consumes less than one-fifth the power of a standard 5-V EPROM. Standby mode supply current is typically less than 1 μ A at 3 V. The AT27BV020 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

(continued)

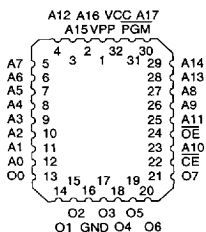
Pin Configurations

Pin Name	Function
A0-A17	Addresses
O0-O7	Outputs
CE	Chip Enable
OE	Output Enable
PGM	Program Strobe

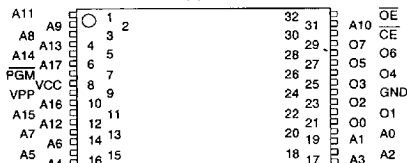
CDIP, PDIP, Top View



LCC, PLCC, Top View



TSOP Top View
Type 1



**2 Megabit
(256K x 8)
Unregulated
Battery-Voltage
High Speed
UV
Erasable
CMOS
EPROM**

Preliminary

Description (Continued)

The AT27BV020 comes in a choice of industry standard JEDEC-approved packages, including: one-time programmable (OTP) plastic PDIP, PLCC, and TSOP, as well as windowed ceramic Cerdip and LCC. All devices feature two-line control (CE, OE) to give designers the flexibility to prevent bus contention.

The AT27BV020 operating with V_{CC} at 3.0 V produces TTL level outputs that are compatible with standard TTL logic devices operating at $V_{CC} = 5.0$ V. At $V_{CC} = 2.7$ V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications.

Atmel's AT27BV020 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV020 programs exactly the same way as a standard 5-V AT27C020 and uses the same programming equipment.

Erase Characteristics

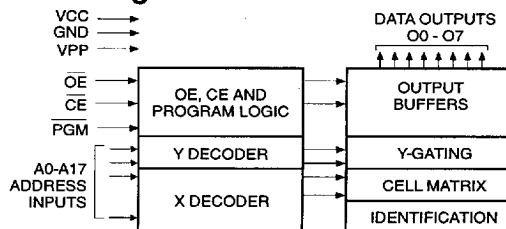
The entire memory array of the AT27BV020 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 μ W/cm² intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W-sec/cm². To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Operating Modes

Mode \ Pin	\overline{CE}	\overline{OE}	\overline{PGM}	Ai	V_{PP}	V_{CC}	Outputs
Read ⁽²⁾	V_{IL}	V_{IL}	X ⁽¹⁾	Ai	X	$V_{CC}^{(2)}$	DOUT
Output Disable ⁽²⁾	X	V_{IH}	X	X	X	$V_{CC}^{(2)}$	High Z
Standby ⁽²⁾	V_{IH}	X	X	X	X	$V_{CC}^{(2)}$	High Z
Rapid Program ⁽³⁾	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	$V_{CC}^{(3)}$	DIN
PGM Verify ⁽³⁾	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	$V_{CC}^{(3)}$	DOUT
PGM Inhibit ⁽³⁾	V_{IH}	X	X	X	V_{PP}	$V_{CC}^{(3)}$	High Z
Product Identification ^(3,5)	V_{IL}	V_{IL}	X	A9= V_H ⁽⁴⁾ A0= V_{IH} or V_{IL} A1-A17= V_{IL}	X	$V_{CC}^{(3)}$	Identification Code

- Notes:
1. X can be V_{IL} or V_{IH} .
 2. Read, output disable, and standby modes require $V_{CC} \leq 3.7$ V.
 3. Refer to Programming Characteristics. Programming modes require $V_{CC} \geq 4.5$ V.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature.....	-65°C to +125°C
Voltage on Any Pin with Respect to Ground.....	-2.0 V to +7.0 V ⁽¹⁾
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V ⁽¹⁾
V_{PP} Supply Voltage with Respect to Ground.....	-2.0 V to +14.0 V ⁽¹⁾
Integrated UV Erase Dose.....	7258 W-sec/cm ²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75$ V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions for Read Operation

AT27BV020					
		-85	-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		2.7 V to 3.6 V	2.7 V to 3.6 V	2.7 V to 3.6 V	2.7 V to 3.6 V

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D.C. and Operating Characteristics for Read Operation

(V_{CC} = 2.7 V to 3.6 V unless otherwise specified)

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0 V to V _{CC}		±1	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0 V to V _{CC}		±5	μA
I _{PP1} ⁽²⁾	V _{PP} ⁽¹⁾ Read/Standby Current	V _{PP} = V _{CC}		10	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3$ V		20	μA
		I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5 V		100	μA
I _{CC}	V _{CC} Active Current	f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$, V _{CC} = 3.6 V	Com.	8	mA
			Ind.	10	mA
V _{IL}	Input Low Voltage	V _{CC} = 3.0 to 3.6 V	-0.6	0.8	V
		V _{CC} = 2.7 to 3.6 V	-0.6	0.2xV _{CC}	V
V _{IH}	Input High Voltage	V _{CC} = 3.0 to 3.6 V	2.0	V _{CC} +0.5	V
		V _{CC} = 2.7 to 3.6 V	0.7xV _{CC}	V _{CC} +0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.0 mA		0.4	V
		I _{OL} = 100 μA		0.2	V
		I _{OL} = 20 μA		0.1	V
V _{OH}	Output High Voltage	I _{OH} = -2.0 mA	2.4		V
		I _{OH} = -100 μA	V _{CC} -0.2		V
		I _{OH} = -20 μA	V _{CC} -0.1		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP}. 2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

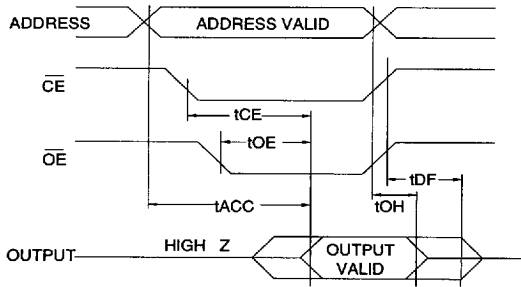
A.C. Characteristics for Read Operation (V_{CC} = 2.7 V to 3.6 V)

			AT27BV020								Units
			-85		-10		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACC} ⁽³⁾	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		85		100		120		150	ns
t _{CE} ⁽²⁾	\overline{CE} to Output Delay	$\overline{OE} = V_{IL}$		85		100		120		150	ns
t _{OE} ^(2,3)	\overline{OE} to Output Delay	$\overline{CE} = V_{IL}$		50		50		50		60	ns
t _{DF} ^(4,5)	\overline{OE} or \overline{CE} High to Output Float			40		40		40		50	ns
t _{OH}	Output Hold from Address, \overline{CE} or \overline{OE} , whichever occurred first		0		0		0		0		ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.



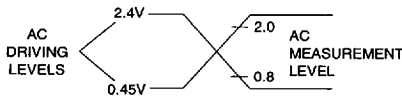
A.C. Waveforms for Read Operation ⁽¹⁾



Notes:

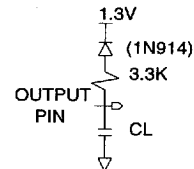
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. \overline{OE} may be delayed up to t_{CE-tOE} after the falling edge of \overline{CE} without impact on t_{CE} .
3. \overline{OE} may be delayed up to $t_{ACC-tOE}$ after the address is valid without impact on t_{ACC} .
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveform and Measurement Level



$t_R, t_F < 20$ ns (10% to 90%)

Output Test Load



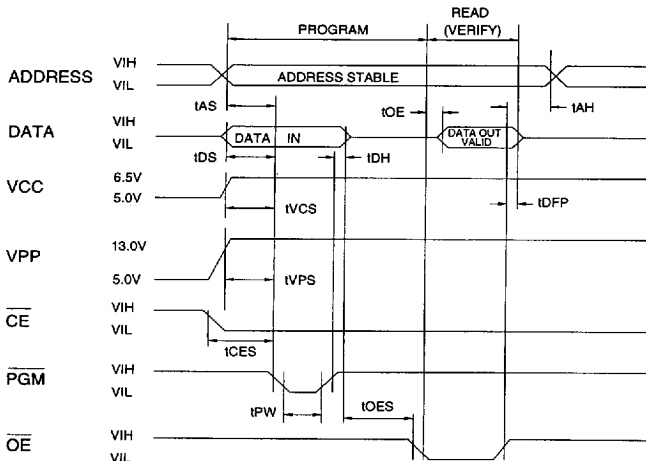
Note: $C_L = 100$ pF including jig capacitance.

Pin Capacitance ($f = 1$ MHz, $T = 25^\circ\text{C}$) ⁽¹⁾

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	$V_{IN} = 0$ V
C_{OUT}	8	12	pF	$V_{OUT} = 0$ V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms ⁽¹⁾



Notes:

1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH} .
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV020 a 0.1- μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 13.0 \pm 0.25\text{ V}$

Sym- bol	Parameter	Test Conditions	Limits		
			Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL}, V_{IH}$		10	μA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1\text{ mA}$.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\text{ }\mu\text{A}$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

 $T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 13.0 \pm 0.25\text{ V}$

Sym- bol	Parameter	Test Conditions* (see Note 1)	Limits	
			Min	Max Units
t_{AS}	Address Setup Time		2	μs
t_{CES}	\overline{CE} Setup Time		2	μs
t_{OES}	\overline{OE} Setup Time		2	μs
t_{DS}	Data Setup Time		2	μs
t_{AH}	Address Hold Time		0	μs
t_{DH}	Data Hold Time		2	μs
t_{DFP}	\overline{OE} High to Out- put Float Delay	(Note 2)	0	130 ns
t_{VPS}	V_{PP} Setup Time		2	μs
t_{VCS}	V_{CC} Setup Time		2	μs
t_{PW}	PGM Program Pulse Width	(Note 3)	95	105 μs
t_{OE}	Data Valid from \overline{OE}			150 ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20 ns
 Input Pulse Levels 0.45 V to 2.4 V
 Input Timing Reference Level 0.8 V to 2.0 V
 Output Timing Reference Level 0.8 V to 2.0 V

Notes:

- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
- This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
- Program Pulse width tolerance is $100\text{ }\mu\text{sec} \pm 5\%$.

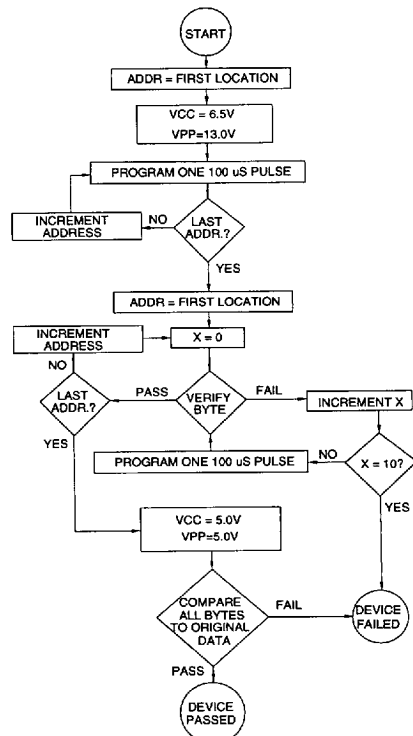
Atmel's 27BV020 Integrated Product Identification Code⁽¹⁾

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	1	0	86

Note: 1. The AT27BV020 has the same Product Identification Code as the AT27C020. Both are programming compatible.

Rapid Programming Algorithm

A 100 μs PGM pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 μs PGM pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.





Ordering Information

t _{ACC} (ns)	I _{CC} (mA) V _{CC} = 3.6 V		Ordering Code	Package	Operation Range
	Active	Standby			
85	8	0.02	AT27BV020-85DC AT27BV020-85JC AT27BV020-85LC AT27BV020-85PC AT27BV020-85TC	32DW6 32J 32LW 32P6 32T	Commercial (0°C to 70°C)
85	10	0.02	AT27BV020-85DI AT27BV020-85JI AT27BV020-85LI AT27BV020-85PI AT27BV020-85TI	32DW6 32J 32LW 32P6 32T	Industrial (-40°C to 85°C)
100	8	0.02	AT27BV020-10DC AT27BV020-10JC AT27BV020-10LC AT27BV020-10PC AT27BV020-10TC	32DW6 32J 32LW 32P6 32T	Commercial (0°C to 70°C)
100	10	0.02	AT27BV020-10DI AT27BV020-10JI AT27BV020-10LI AT27BV020-10PI AT27BV020-10TI	32DW6 32J 32LW 32P6 32T	Industrial (-40°C to 85°C)
120	8	0.02	AT27BV020-12DC AT27BV020-12JC AT27BV020-12LC AT27BV020-12PC AT27BV020-12TC	32DW6 32J 32LW 32P6 32T	Commercial (0°C to 70°C)
120	10	0.02	AT27BV020-12DI AT27BV020-12JI AT27BV020-12LI AT27BV020-12PI AT27BV020-12TI	32DW6 32J 32LW 32P6 32T	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV020-15DC AT27BV020-15JC AT27BV020-15LC AT27BV020-15PC AT27BV020-15TC	32DW6 32J 32LW 32P6 32T	Commercial (0°C to 70°C)
150	10	0.02	AT27BV020-15DI AT27BV020-15JI AT27BV020-15LI AT27BV020-15PI AT27BV020-15TI	32DW6 32J 32LW 32P6 32T	Industrial (-40°C to 85°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
32T	32 Lead, Plastic Thin Small Outline Package OTP (TSOP)

3-14

AT27BV020

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