

ADS1210 ADS1211

24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- DELTA-SIGMA A/D CONVERTER
- 24 BITS NO MISSING CODES
- 23 BITS EFFECTIVE RESOLUTION AT 10Hz AND 20 BITS AT 1000Hz
- DIFFERENTIAL INPUTS
- PROGRAMMABLE GAIN AMPLIFIER
- FLEXIBLE SPI COMPATIBLE SSI INTERFACE WITH 2-WIRE MODE
- PROGRAMMABLE CUT-OFF FREQUENCY UP TO 16kHz
- INTERNAL/EXTERNAL REFERENCE
- ON CHIP SELF-CALIBRATION
- ADS1211 INCLUDES 4 CHANNEL MUX

APPLICATIONS

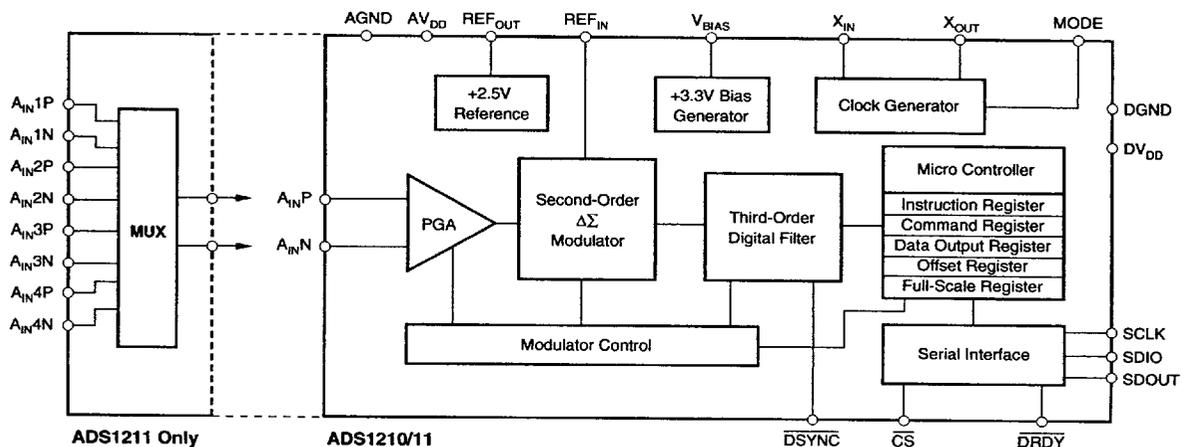
- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

DESCRIPTION

The ADS1210 and ADS1211 are precision, wide dynamic range, delta-sigma analog-to-digital converters with 24-bit resolution operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low level voltage signals. The delta-sigma architecture is used for wide dynamic range and to guarantee 24 bits of no missing code performance. An effective resolution of 23 bits is achieved through the use of a very low-noise input amplifier at conversion rates up to 10Hz. Effective resolutions of 20 bits can be maintained up to a sample rate of 1kHz through the use of the unique Turbo modulator mode of operation. The dynamic range of the converters is further increased by providing a low-noise programmable gain amplifier with a gain range of 1 to 16 in binary steps.

The ADS1210 and ADS1211 are designed for high resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography and portable instrumentation. Both converters include a flexible synchronous serial interface which is SPI compatible and also offers a two-wire control mode for low cost isolation.

The ADS1210 is a single channel converter and is offered in both 18-pin DIP and SOIC packages. The ADS1211 includes a 4 channel input multiplexer and is available in 24-pin DIP, 24-pin SOIC, and 28-pin SSOP packages.



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SPECIFICATIONS

All specifications T_{MIN} to T_{MAX} , $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 10MHz$, Programmable Gain Amplifier setting of one, Turbo Mode Rate of one, REF_{OUT} disabled, V_{BIAS} disabled, and external 2.5V reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1210U, P/ADS1211U, P, E			UNITS
		MIN	TYP	MAX	
ANALOG INPUT					
Input Voltage Range ⁽¹⁾		0 -10		+5 +10	V V
Input Impedance	With V_{BIAS} ⁽²⁾ G = Gain, TMR = Turbo Mode Rate		$4/(G \cdot TMR)$ ⁽³⁾		MΩ
Programmable Gain Amplifier	User Selectable Gain Ranges	1		16	
Input Capacitance			12		pF
Input Leakage Current			5	50	pA
SYSTEMS PERFORMANCE					
Resolution			24		Bits
No Missing Codes	$f_{DATA} = 60Hz$	24			Bits
	$f_{DATA} = 100Hz$, TMR of 4	24			Bits
	$f_{DATA} = 250Hz$, TMR of 8	23			Bits
	$f_{DATA} = 500Hz$, TMR of 16	24			Bits
	$f_{DATA} = 1000Hz$, TMR of 16	23			Bits
Integral Linearity	$f_{DATA} = 60Hz$			±0.003	%FSR
	$f_{DATA} = 1000Hz$, TMR of 16			±0.003	%FSR
Unipolar Offset Error ⁽⁴⁾			See Note 5		μV/°C
Unipolar Offset Drift ⁽⁶⁾			1		μV/°C
Gain Error ⁽⁴⁾			See Note 5		μV/°C
Gain Error Drift ⁽⁶⁾			1		μV/°C
Common-Mode Rejection	At dc	90	110		dB
	50Hz, $f_{DATA} = 50Hz$ ⁽⁷⁾	160			dB
	60Hz, $f_{DATA} = 60Hz$ ⁽⁷⁾	160			dB
Normal-Mode Rejection	50Hz, $f_{DATA} = 50Hz$ ⁽⁷⁾	100			dB
	60Hz, $f_{DATA} = 60Hz$ ⁽⁷⁾	100			dB
Output Noise		See Typical Performance Curves			
Power Supply Rejection	dc, 50Hz, and 60Hz	65			dB
VOLTAGE REFERENCE					
Internal Reference (REF_{OUT})		2.4	2.5	2.6	V
Drift			25		ppm/°C
Noise			50		μVp-p
Load Current	Source or Sink			1	mA
Output Impedance			2		Ω
External Reference (REF_{IN})		2.0		3.0	V
Load Current				2.5	μA
V_{BIAS} Output	Using Internal Reference	3.15	3.3	3.45	V
Drift			50		ppm/°C
Load Current	Source or Sink			10mA	
DIGITAL INPUT/OUTPUT					
Logic Family		TTL Compatible CMOS			
Logic Level: (all except X_{IN})					
V_{IH}	$I_{IH} = +5\mu A$	2.0		+ DV_{DD}	V
V_{IL}	$I_{IL} = +5\mu A$	0		0.8	V
V_{OH}	$I_{OH} = 2$ TTL Loads	2.4		+ DV_{DD}	V
V_{OL}	$I_{OL} = 2$ TTL Loads	0		0.4	V
X_{IN} Input Levels: V_{IH}		3.5		+ DV_{DD}	V
V_{IL}		0		0.8	V
X_{IN} Frequency Range (f_{XIN})		0.5		10	MHz
Output Data Rate (f_{XIN})	User Programmable	2.4		16,000	Hz
	$f_{XIN} = 500kHz$	0.12		800	Hz
Data Format	User Programmable	Two's Complement or Offset Binary			
SYSTEM CALIBRATION					
Offset and Full-Scale Limits	$V_{FS} = \text{Full-Scale Differential Voltage}^{(8)}$ $V_{OS} = \text{Offset Differential Voltage}^{(8)}$	$0.7 \cdot (2 \cdot REF_{IN})/G$		$1.3 \cdot (2 \cdot REF_{IN})/G$	

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ADS1210/1211

SPECIFICATIONS (CONT)

All specifications T_{MIN} to T_{MAX} , $AV_{DD} = DV_{DD} = +5V$, $f_{XIN} = 10MHz$, Programmable Gain Amplifier setting of one, Turbo Mode Rate of one, REF_{OUT} disabled, V_{BIAS} disabled, and external 2.5V reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1210U, P/ADS1211U, P, E			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Power Supply Voltage		4.75		5.25	V
Power Supply Current:					
Analog Current			2		mA
Digital Current			3.5		mA
Additional Analog Current with REF_{OUT} Enabled			1.6		mA
V_{BIAS} Enabled	No Load		1		mA
Power Dissipation	TMR of 16		26	40	mW
	$f_{XIN} = 2.5MHz$		37	60	mW
	$f_{XIN} = 2.5MHz$, TMR of 16		17		mW
	Sleep Mode		27		mW
			11		mW
TEMPERATURE RANGE					
Specified		-40		+85	°C
Storage		-60		+125	°C

NOTES: (1) In order to achieve the converter's full-scale range, the input must be fully differential ($A_{IN,N} = REF_{IN} - A_{IN,P}$). If the input is single-ended ($A_{IN,N}$ or $A_{IN,P}$ is fixed), then the full scale range is one-half that of the differential range. (2) This range is set with external resistors and V_{BIAS} (as described in the text). Other ranges are possible. (3) Input impedance is higher with lower f_{XIN} . (4) Applies after calibration. (5) These errors will be of the order of the effective resolution of the converter. Refer to the Typical Performance Curves which apply to the desired mode of operation. (6) Recalibration can remove these errors. (7) The specification also applies at $f_{DATA} \cdot i$ where i is 2, 3, 4, etc. (8) Voltages at the analog inputs must remain within AGND to AV_{DD} .

ABSOLUTE MAXIMUM RATINGS

Analog Input: Current	$\pm 100mA$, Momentary
	$\pm 10mA$, Continuous
Voltage	AGND $-0.3V$ to $AV_{DD} + 0.3V$
AV_{DD} to DV_{DD}	$-0.3V$ to $6V$
AV_{DD} to AGND	$-0.3V$ to $6V$
DV_{DD} to DGND	$-0.3V$ to $6V$
AGND to DGND	$\pm 0.3V$
REF_{IN} Voltage to AGND	$-0.3V$ to $AV_{DD} + 0.3V$
Digital Input Voltage to DGND	$-0.3V$ to $DV_{DD} + 0.3V$
Digital Output Voltage to DGND	$-0.3V$ to $DV_{DD} + 0.3V$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$
Power Dissipation (Any package)	500mW

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

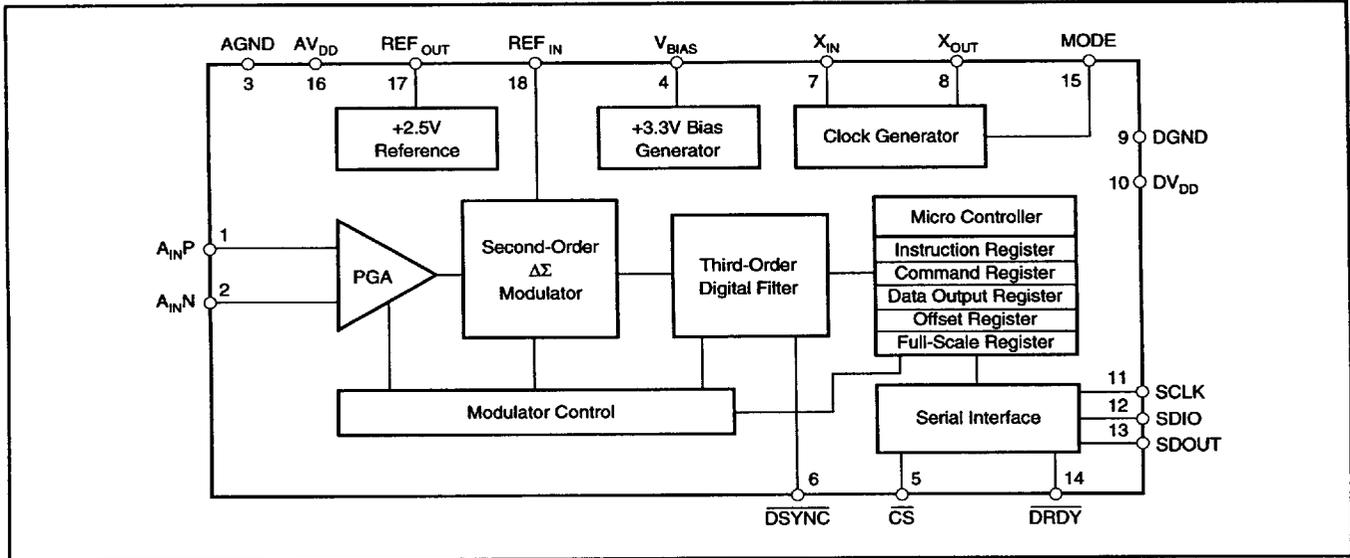
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
ADS1210P	18-Pin Plastic DIP	218
ADS1210U	18-Lead SOIC	219
ADS1211P	24-Pin Plastic DIP	243
ADS1211U	24-Lead SOIC	239
ADS1211E	28-Lead SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

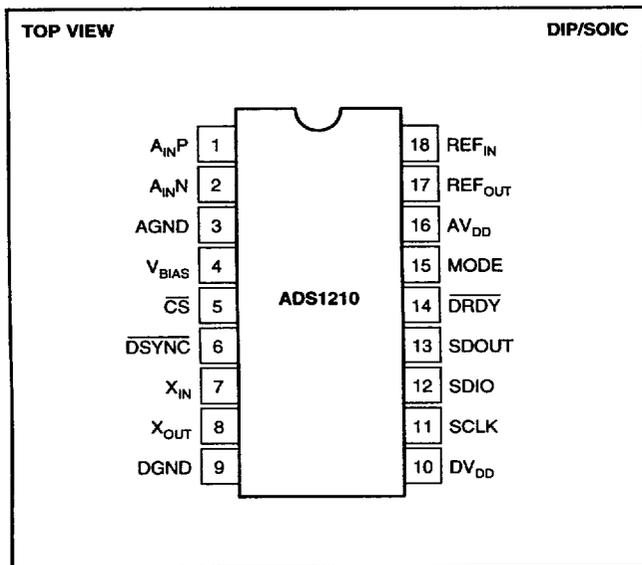
ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
ADS1210P	18-Pin Plastic DIP	$-40^{\circ}C$ to $+85^{\circ}C$
ADS1210U	18-Lead SOIC	$-40^{\circ}C$ to $+85^{\circ}C$
ADS1211P	24-Pin Plastic DIP	$-40^{\circ}C$ to $+85^{\circ}C$
ADS1211U	24-Lead SOIC	$-40^{\circ}C$ to $+85^{\circ}C$
ADS1211E	28-Lead SSOP	$-40^{\circ}C$ to $+85^{\circ}C$

ADS1210 SIMPLIFIED BLOCK DIAGRAM



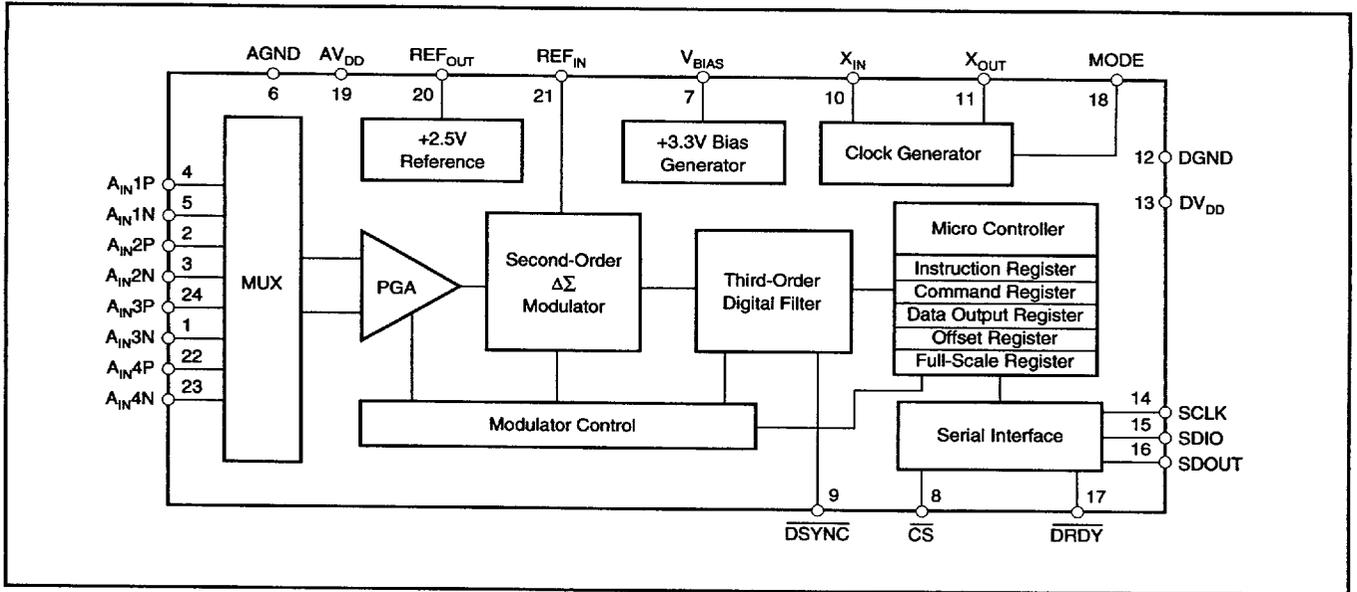
ADS1210 PIN CONFIGURATION



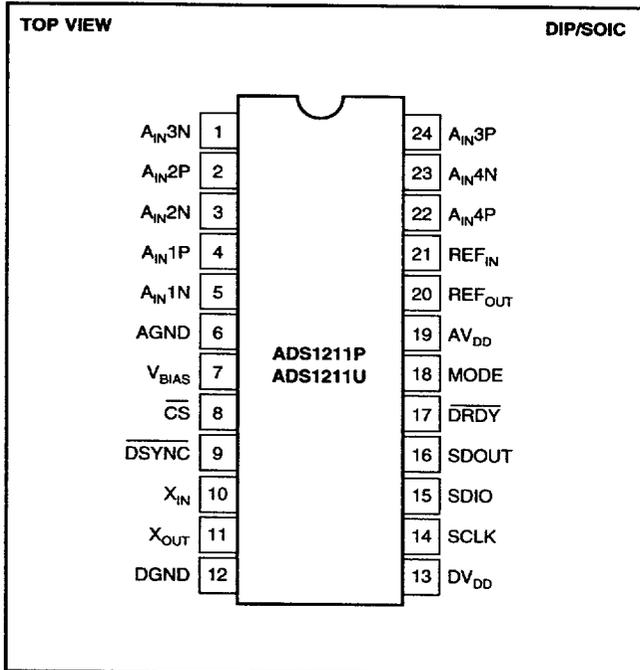
ADS1210 PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	A _{INP}	Noninverting Input.
2	A _{INN}	Inverting Input.
3	AGND	Analog Ground.
4	V _{BIAS}	Bias Voltage Output, +3.3V nominal.
5	CS	Chip Select Input.
6	DS $\overline{\text{SYNC}}$	Control Input to Synchronize Serial Output Data.
7	X _{IN}	System Clock Input.
8	X _{OUT}	System Clock Output (for Crystal or Resonator).
9	DGND	Digital Ground.
10	DV _{DD}	Digital Supply, +5V nominal.
11	SCLK	Clock Input/Output for serial data transfer.
12	SDIO	Serial Data Input (can also function as Serial Data Output).
13	SDOUT	Serial Data Output.
14	DRDY	Data Ready.
15	MODE	SCLK Control Input (Master = 1, Slave = 0).
16	AV _{DD}	Analog Supply, +5V nominal.
17	REF _{OUT}	Reference Output, +2.5V nominal.
18	REF _{IN}	Reference Input.

ADS1211 SIMPLIFIED BLOCK DIAGRAM



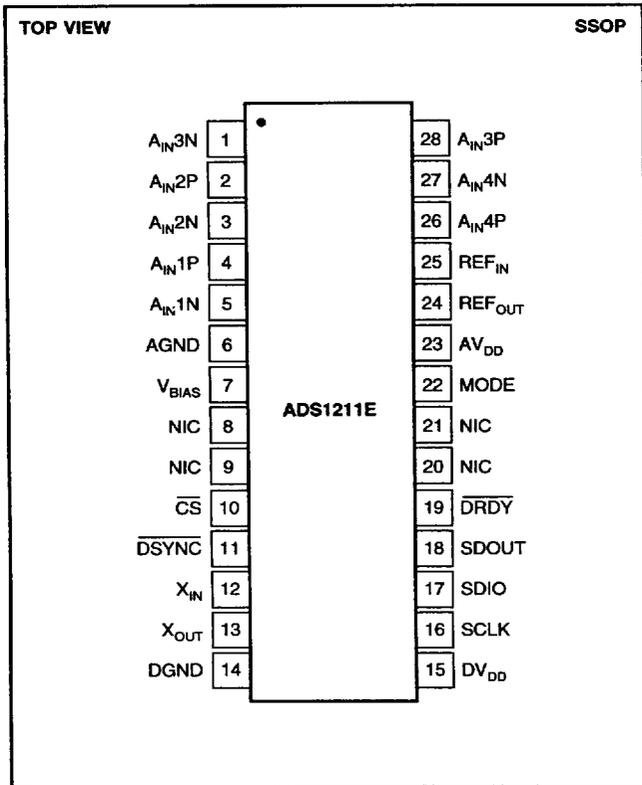
ADS1211P AND ADS1211U PIN CONFIGURATION



ADS1211P AND ADS1211U PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	A _{IN} 3N	Inverting Input Channel 3.
2	A _{IN} 2P	Noninverting Input Channel 2.
3	A _{IN} 2N	Inverting Input Channel 2.
4	A _{IN} 1P	Noninverting Input Channel 1.
5	A _{IN} 1N	Inverting Input Channel 1.
6	AGND	Analog Ground.
7	V _{BIAS}	Bias Voltage Output, +3.3V nominal.
8	CS	Chip Select Input.
9	DSYNC	Control Input to Synchronize Serial Output Data.
10	X _{IN}	System Clock Input.
11	X _{OUT}	System Clock Output (for Crystal or Resonator).
12	DGND	Digital Ground.
13	DV _{DD}	Digital Supply, +5V nominal.
14	SCLK	Clock Input/Output for serial data transfer.
15	SDIO	Serial Data Input (can also function as Serial Data Output).
16	SDOUT	Serial Data Output.
17	DRDY	Data Ready.
18	MODE	SCLK Control Input (Master = 1, Slave = 0).
19	AV _{DD}	Analog Supply, +5V nominal.
20	REF _{OUT}	Reference Output: +2.5V nominal.
21	REF _{IN}	Reference Input.
22	A _{IN} 4P	Noninverting Input Channel 4.
23	A _{IN} 4N	Inverting Input Channel 4.
24	A _{IN} 3P	Noninverting Input Channel 3.

ADS1211E CONFIGURATION

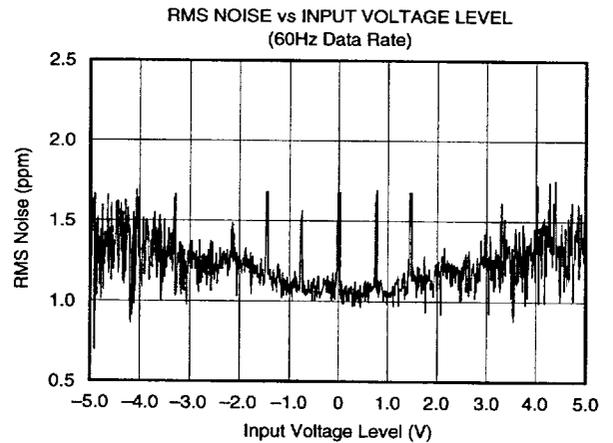
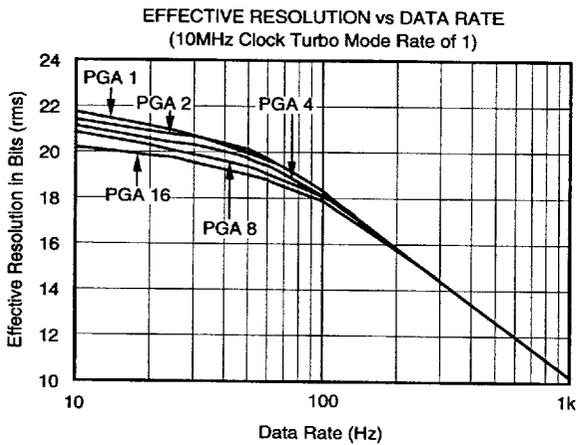
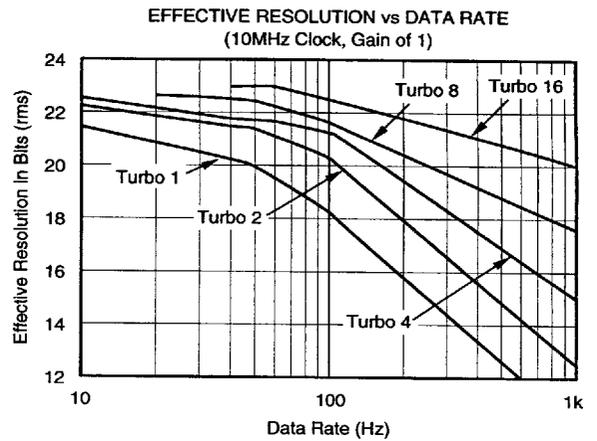
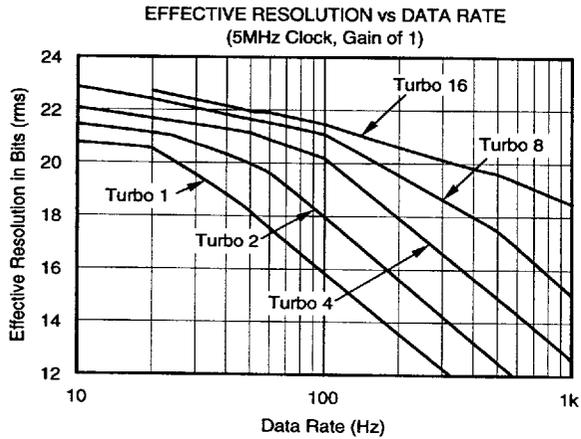
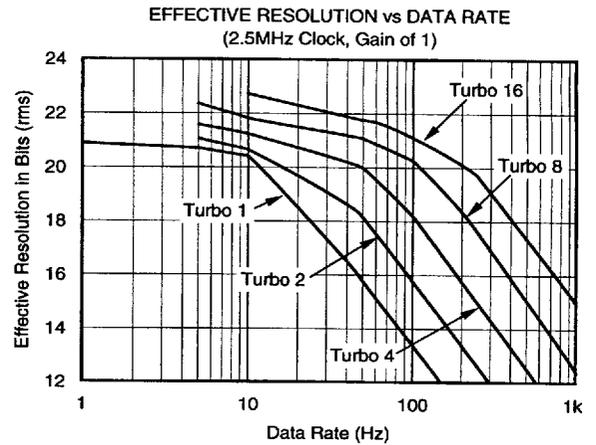
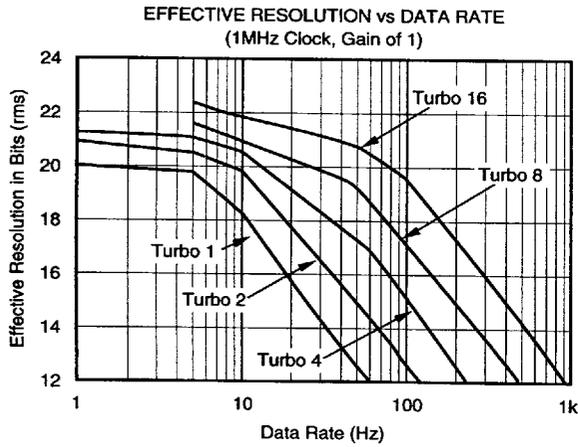


ADS1211E PIN DEFINITIONS

PIN NO	NAME	DESCRIPTION
1	A _{IN} 3N	Inverting Input Channel 3.
2	A _{IN} 2P	Noninverting Input Channel 2.
3	A _{IN} 2N	Inverting Input Channel 2.
4	A _{IN} 1P	Noninverting Input Channel 1.
5	A _{IN} 1N	Inverting Input Channel 1.
6	AGND	Analog Ground.
7	V _{BIAS}	Bias Voltage Output, +3.3V nominal.
8	NIC	Not Internally Connected.
9	NIC	Not Internally Connected.
10	\overline{CS}	Chip Select Input.
11	DSYNC	Control Input to Synchronize Serial Output Data.
12	X _{IN}	System Clock Input.
13	X _{OUT}	System Clock Output (for Crystal or Resonator).
14	DGND	Digital Ground.
15	DV _{DD}	Digital Supply, +5V nominal.
16	SCLK	Clock Input/Output for serial data transfer.
17	SDIO	Serial Data Input (can also function as Serial Data Output).
18	SDOUT	Serial Data Output.
19	\overline{DRDY}	Data Ready.
20	NIC	Not Internally Connected.
21	NIC	Not Internally Connected.
22	MODE	SCLK Control Input (Master = 1, Slave = 0).
23	AV _{DD}	Analog Supply, +5V nominal.
24	REF _{OUT}	Reference Output: +2.5V nominal.
25	REF _{IN}	Reference Input.
26	A _{IN} 4P	Noninverting Input Channel 4.
27	A _{IN} 4N	Inverting Input Channel 4.
28	A _{IN} 3P	Noninverting Input Channel 3.

TYPICAL PERFORMANCE CURVES

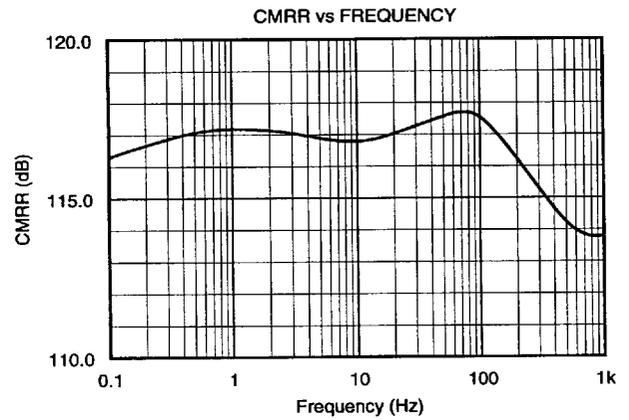
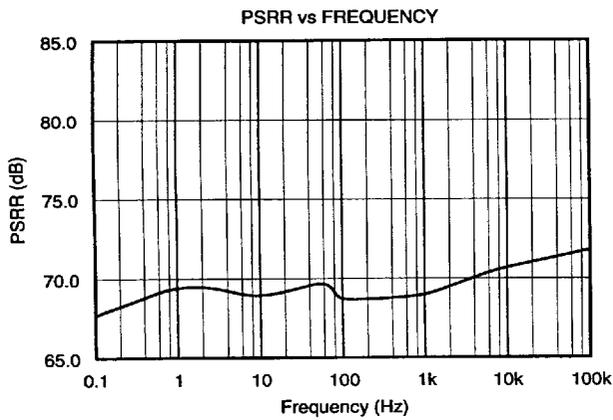
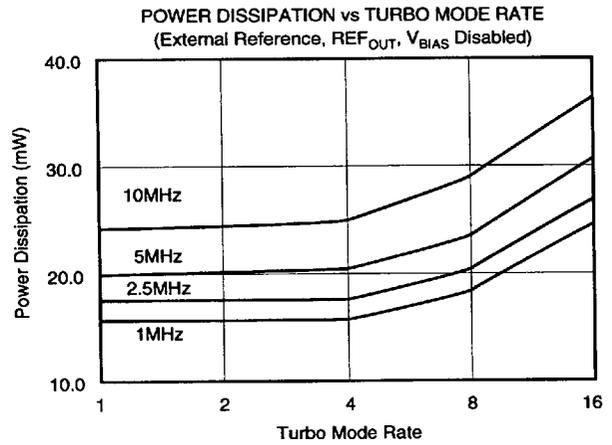
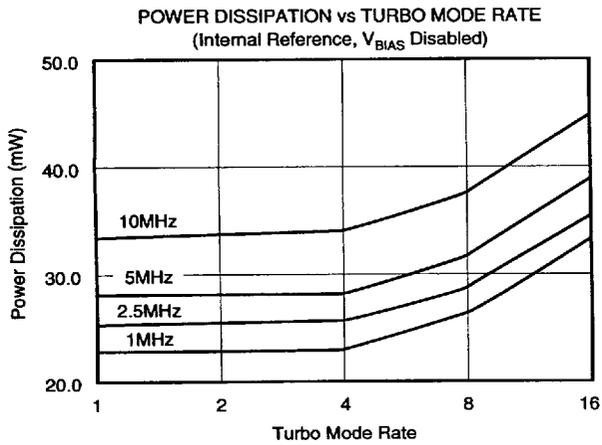
At $T = +25^{\circ}\text{C}$, $AV_{DD} = DV_{DD} = +5\text{V}$, $f_{SC} = 10\text{MHz}$, and $V_{REF} = +2.5\text{V}$, unless otherwise specified.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T = +25^{\circ}\text{C}$, $AV_{DD} = DV_{DD} = +5\text{V}$, $f_{SC} = 10\text{MHz}$, and $V_{REF} = +2.5\text{V}$, unless otherwise specified.



ADS1210/1211

THEORY OF OPERATION

The ADS1210 and ADS1211 are precision, high dynamic range, self-calibrating, 24-bit, delta-sigma A/D converters capable of achieving very high resolution digital results. Each contains a programmable gain amplifier (PGA); a second-order delta-sigma modulator; a programmable digital filter; a microcontroller including the Instruction, Command and Calibration registers; a serial interface; a clock generator circuit; and an internal 2.5V reference. The ADS1211 includes a 4-channel input multiplexer.

In order to provide low system noise, common-mode rejection of 120dB and excellent power supply rejection, the design topology is based on a fully differential switched capacitor architecture. Turbo Mode, a unique feature of the ADS1210/11, can be used to boost the sampling rate of the input capacitor, which is normally 20kHz with a 10MHz clock. By programming the Command Register, the sampling rate can be increased to 40kHz, 80kHz, 160kHz, or 320kHz. Each increase in sample rate results in an increase in performance while maintaining the same output data rate.

The programmable gain amplifier (PGA) of the ADS1210/11 can be set to a gain of 1, 2, 4, 8 or 16—substantially increasing the dynamic range of the converter and simplifying the interface to the more common transducers (see Table I). This gain is implemented by increasing the number of samples taken by the input capacitor from 20kHz for a gain of 1 to 320kHz for a gain of 16. Since the Turbo Mode and PGA functions are both implemented by varying the sampling frequency of the input capacitor, the combination of PGA gain and Turbo Mode Rate is limited to 16 (see Table II). For example, when using a Turbo Mode Rate of 8 (160kHz at 10MHz), the maximum PGA gain setting is 2.

GAIN SETTING	ANALOG INPUT ⁽¹⁾		ANALOG INPUT UTILIZING V _{BIAS} ^(1,2)	
	FULL-SCALE RANGE (V)	EXAMPLE VOLTAGE RANGE ⁽³⁾ (V)	FULL-SCALE RANGE (V)	EXAMPLE VOLTAGE RANGE ⁽³⁾ (V)
1	10	0 to 5	40	±10
2	5	1.25 to 3.75	20	±5
4	2.5	1.88 to 3.13	10	±2.5
8	1.25	2.19 to 2.81	5	±1.25
16	0.625	2.34 to 2.66	2.5	±0.625

NOTE: (1) With a 2.5V reference, such as the internal reference. (2) This example utilizes the circuit in Figure 12. Other input ranges are possible. (3) The ADS1210/11 allows common-mode voltage as long as the absolute input voltage on A_{INP} or A_{INN} does not go below AGND or above AV_{DD}.

TABLE I. Full-Scale Range vs PGA Gain Setting.

TURBO MODE RATE	AVAILABLE PGA GAIN SETTINGS
1	1, 2, 4, 8, 16
2	1, 2, 4, 8
4	1, 2, 4
8	1, 2
16	1

TABLE II. Available PGA Gain Settings vs Turbo Mode Rate.

The output data rate of the ADS1210/11 can be varied from a few hertz to as much as 16kHz, trading off lower resolution results for higher data rates. In addition, the data rate determines the first null of the digital filter and sets the -3dB point of the input bandwidth (see the Digital Filter section). Changing the data rate of the ADS1210/11 does not result in a change in the sampling rate of the input capacitor. The data rate effectively sets the number of samples which are used by the digital filter to obtain each conversion result. A lower data rate results in higher resolution, lower input bandwidth, and different notch frequencies than a higher data rate. It does not result in any change in input impedance or modulator frequency, or any appreciable change in power consumption.

The ADS1210/11 also includes complete on-board calibration that can correct for internal offset and gain errors or limited external system errors. Internal calibration can be run when needed, or automatically and continuously in the background. System calibration can be run as needed and the appropriate input voltages must be provided to the ADS1210/11. For this reason, there is no continuous system calibration mode. The calibration registers are fully readable and writable. This feature allows for switching between various configurations—different data rates, Turbo Mode Rates, and gain settings—without re-calibrating.

The various settings, rates, modes, and registers of the ADS1210/11 are read or written via a synchronous serial interface. This interface can operate in either a self-clocked mode (Master Mode) or an externally clocked mode (Slave Mode). In the Master Mode, the serial clock (SCLK) frequency is one-half of the ADS1210/11 X_{IN} clock frequency. This is an important consideration for many systems and may determine the maximum ADS1210/11 clock that can be used.

The high resolution and flexibility of the ADS1210/11 allow these converters to fill a wide variety of A/D conversion tasks. In order to ensure that a particular configuration will meet the design goals, there are several important items which must be considered. These include (but are certainly not limited to) the needed resolution, required linearity, desired input bandwidth, power consumption goal, and sensor output voltage.

The remainder of this data sheet discusses the operation of the ADS1210/11 in detail. In order to allow for easier comparison of different configurations, “effective resolution” is used as the figure of merit for most tables and graphs. For example, Table III shows a comparison between data rate (and -3dB input bandwidth) versus PGA gain setting at a Turbo Mode Rate of 1 and a clock rate of 10MHz. See the Definition of Terms section for a definition of effective resolution.

DATA RATE (HZ)	-3DB FREQUENCY (HZ)	EFFECTIVE RESOLUTION (BITS RMS)				
		G = 1	G = 2	G = 4	G = 8	G = 16
10	2.62	21.5	21.0	21.0	21.0	20.0
25	6.55	20.5	20.5	20.5	20.0	19.5
30	7.86	20.5	20.5	20.5	20.0	19.5
50	13.1	20.0	20.0	20.0	19.5	19.0
60	15.7	19.5	19.5	19.5	19.0	19.0
100	26.2	18.0	18.0	18.0	18.0	18.0
250	65.5	15.0	15.0	15.0	15.0	15.0
500	131	12.5	12.5	12.5	12.5	12.5
1000	262	10.0	10.5	10.0	10.0	10.0

TABLE III. Effective Resolution vs Data Rate and Gain Setting. (Turbo Mode Rate of 1 and a 10MHz clock.)

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Differential Voltage—For an analog signal that is fully differential, the voltage range can be compared to that of an instrumentation amplifier. For example, if both analog inputs of the ADS1210 are at 2.5V, then the differential voltage is 0V. If one is at 0V and the other at 5V, then the differential voltage is 5V. But, this is the case regardless of which input is at 0V and which is at 5V, while the digital output result is quite different.

The analog input differential voltage is always given as the voltage at A_{INP} relative to that at A_{INN} . Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 2, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is -2.5V. In each case, the actual input voltages must remain within the AGND to AV_{DD} range.

Actual Analog Input Voltage—The voltage at any one analog input relative to AGND.

Full-Scale Range (FSR)—As with most A/D converters, the full-scale range of the ADS1210/11 is defined as the "input" which produces the positive full-scale digital output minus the "input" which produces the negative full-scale digital output. For the ADS1210/11, the "input" is defined as the analog input differential voltage and, because the inputs are differential, is simply two times the voltage which produces the full-scale digital output (either positive or negative).

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the positive full-scale output is produced when the analog input differential voltage is 2.5V. The full-scale range in this configuration is 5V.

Typical Analog Input Voltage Range—This term describes the actual voltage range of the analog inputs which

will cover the converter's full-scale range, assuming that each input has a common-mode voltage that is smaller than $(AV_{DD} - REF_{IN}/PGA)$ and that the inputs are differential (actual voltage at $A_{INN} = A_{INP} - REF_{IN}/2$). It applies to both the positive and the negative input.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 2, the typical input voltage range is 1.25V to 3.75V. However, an input range of 0V to 2.5V would also cover the converter's full-scale range.

Voltage Span—This is simply the magnitude of the typical analog input voltage range. For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 2, the input voltage span is 2.5V.

Least Significant Bit (LSB) Weight—This is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full-Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

Effective Resolution—The effective resolution of the ADS1210/11 in a particular configuration can be expressed in two different units: bits rms and microvolts rms. Computed directly from the converter's output data, each is a statistical calculation based on a given number of results. Knowing one, the other can be computed as follows:

$$\text{ER in bits rms} = \frac{20 \cdot \log \left(\frac{10V}{\text{ER in Vrms}} \right) - 1.76}{6.02}$$

$$\text{ER in Vrms} = \frac{10V}{10^{\left(\frac{6.02 \cdot \text{ER in bits rms} + 1.76}{20} \right)}}$$

The 10V figure in each calculation represents the full-scale range of the ADS1210/11 in a gain setting of 1. This means that both units are absolute expressions of resolution—the performance in different configurations can be directly compared regardless of the units. Comparing the resolution of different gain settings expressed in bits rms requires accounting for the PGA setting.

For example, Table III shows that for a gain of 1 and a data rate of 10Hz, the effective resolution of the ADS1210/11 is 21.5 bits rms. For a gain of 4, the effective resolution is 21.0 bits rms. This means that the noise has increased slightly (2.8 to 3.9 μ Vrms). However, in a gain of 4, the LSB weight has decreased by a factor of 4. So, the one sigma span of the noise will now cover four times as many digital output codes.

Main Controller—A generic term for the microcontroller, microprocessor, or digital signal processor which is controlling the operation of the ADS1210/11 and receiving the output data.

f_{XIN} —The frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1210/11.

f_{MOD} —The frequency or speed at which the modulator of the ADS1210/11 is running, given by the following equation:

$$f_{MOD} = \frac{f_{XIN} \cdot \text{Turbo Mode}}{512}$$

f_{SAMP} —The frequency or switching speed of the input sampling capacitor. The value is given by the following equation:

$$f_{SAMP} = \frac{f_{XIN} \cdot \text{Turbo Mode} \cdot \text{Gain Setting}}{512}$$

f_{DATA} , t_{DATA} —The frequency of the digital output data produced by the ADS1210/11 or the inverse of this (the period), respectively, f_{DATA} is also referred to as the data rate.

$$f_{DATA} = \frac{f_{XIN} \cdot \text{Turbo Mode}}{512 \cdot \text{Decimation Ratio}}, \quad t_{DATA} = \frac{1}{f_{DATA}}$$

Conversion Cycle—The term “conversion cycle” usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period. However, each digital output is actually based on the modulator results from the last three t_{DATA} time periods.

DIGITAL FILTER

The digital filter of the ADS1210/11 computes the output result based on the most recent results from the delta-sigma modulator. The number of modulator results that are used depend on the decimation ratio set in the Command Register. At the most basic level, the digital filter can be thought of as simply averaging the modulator results and presenting this average as the digital output.

While the decimation ratio determines the number of modulator results to use, the modulator runs faster at higher Turbo Modes. These two items, together with the ADS1210/11 clock frequency, determine the output data rate:

$$f_{DATA} = \frac{f_{XIN} \cdot \text{Turbo Mode}}{512 \cdot \text{Decimation Ratio}}$$

Also, since the conversion result is essentially an average, the data rate determines where the resulting notches are in the digital filter. For example, if the output data rate is 1kHz, then a 1kHz input frequency will average to zero during the 1ms conversion cycle. Likewise, a 2kHz input frequency will average to zero, etc.

In this manner, the data rate can be used to set specific notch frequencies in the digital filter response (see Figure 1 for the normalized response of the digital filter). For example, if the rejection of power line frequencies is desired, then the data rate can simply be set to the power line frequency. Figures 2 and 3 show the digital filter response for a data rate of 50Hz and 60Hz, respectively.

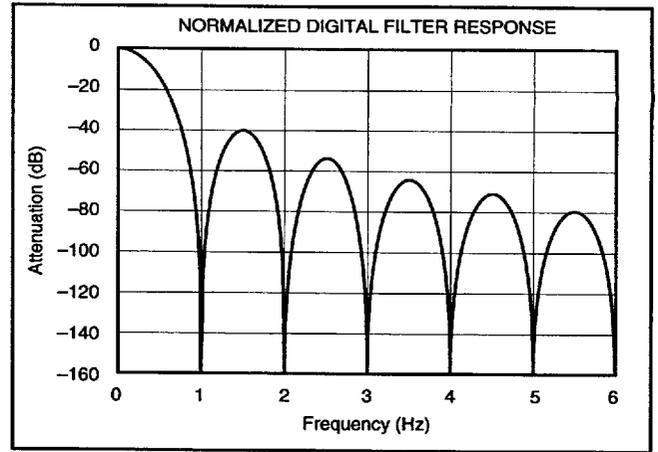


FIGURE 1. Normalized Digital Filter Response.

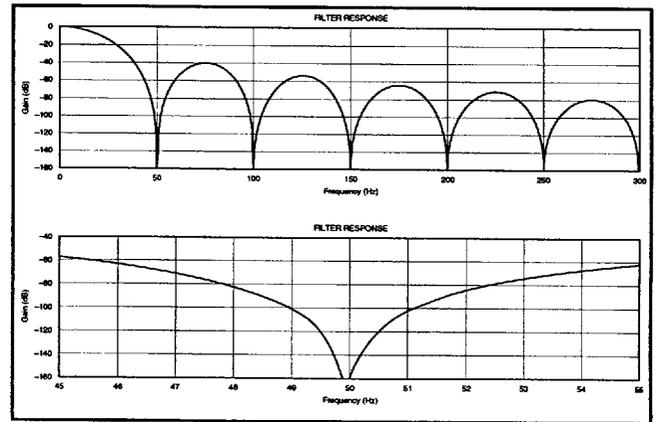


FIGURE 2. Digital Filter Response at a Data Rate of 50Hz.

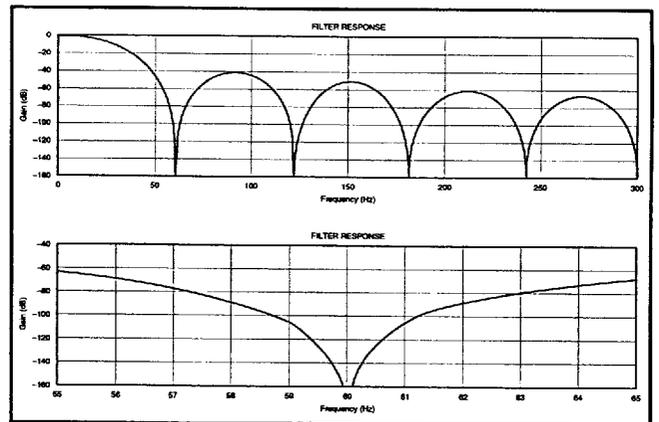


FIGURE 3. Digital Filter Response at a Data Rate of 60Hz.

If the effective resolution at a 50Hz or 60Hz data rate is not adequate for the particular application, then power line frequencies could still be rejected by operating the ADS1210/11 at 25/30Hz, 16.7/20Hz, 12.5/15Hz, etc. If a higher data rate is needed, then power line frequencies must either be rejected before conversion (with an analog notch filter) or after conversion (with a digital notch filter running on the main controller).

Filter Equation

The digital filter is described by the following transfer function:

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi \cdot f \cdot N}{f_{MOD}}\right)}{N \cdot \sin\left(\frac{\pi \cdot f}{f_{MOD}}\right)} \right|^3$$

where N is the Decimation Ratio.

This filter has a $(\sin(x)/x)^3$ response and is referred to a sinc³ filter. For the ADS1210/11, this type of filter allows the data rate to be changed over a very wide range (nearly four orders of magnitude). However, the -3dB point of the filter is 0.262 times the data rate. And, as can be seen in Figures 1 and 2, the rejection in the stopband (frequencies higher than the first notch frequency) may only be -40dB.

These factors must be considered in the overall system design. For example, with a 50Hz data rate, a significant signal at 75Hz may alias back into the passband at 25Hz. The analog front end can be designed to provide the needed attenuation to prevent aliasing, or the system may simply provide this inherently. Another possibility is increasing the data rate and then post filtering with a digital filter on the main controller.

Filter Settling

The number of modulator results used to compute each conversion result is three times the Decimation Ratio. This means that any step change (or any channel change for the ADS1211) will require at least three conversions to fully settle. However, if the change occurs asynchronously, then at least four conversions are required to ensure complete settling. For example, on the ADS1211, the fourth conversion result after a channel change will be valid (see Figure 4).

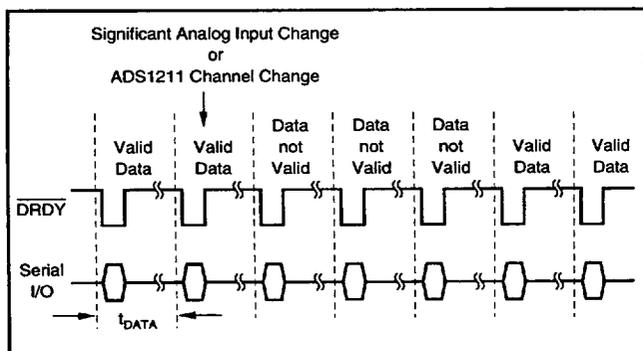


FIGURE 4. ADS1210/11 Analog Input Voltage Step or ADS1211 Channel Change to Fully Settled Output Data.

TURBO MODE

The ADS1210/11 offers a unique Turbo Mode feature which can be used to increase the modulator sampling rate by 2, 4, 8, or 16 times normal. With the increase of modulator sampling frequency, there can be a substantial increase in

the effective resolution of the output data at a given data rate, but there is also an increase in power dissipation. For Turbo Mode Rates 2 and 4, the increase is slight. For rates 8 and 16, the increase is more substantial. See the Typical Performance Curves for more information.

In a Turbo Mode Rate of 16, the ADS1210/11 can offer 20 bits of effective resolution at a 1kHz data rate. A comparison of effective resolution versus Turbo Mode Rates and output data rates is shown in Table IV while Table V shows the corresponding noise level in μVrms .

Data Rate (Hz)	Effective Resolution (Bits rms)				
	Turbo Mode Rate 1	Turbo Mode Rate 2	Turbo Mode Rate 4	Turbo Mode Rate 8	Turbo Mode Rate 16
10	21.5	22.0	22.5		
20	21.0	22.0	22.0	22.5	
40	20.0	21.5	22.0	22.5	23.0
50	20.0	21.5	21.5	22.0	23.0
60	19.5	21.0	21.5	22.0	23.0
100	18.0	20.0	21.0	21.5	22.5
1000	10.0	12.5	15.0	17.5	20.0

TABLE IV. Effective Resolution vs Data Rate and Turbo Mode Rate. (PGA gain setting of 1 and 10MHz clock.)

DATA RATE (Hz)	NOISE LEVEL (μVrms)				
	TURBO MODE RATE 1	TURBO MODE RATE 2	TURBO MODE RATE 4	TURBO MODE RATE 8	TURBO MODE RATE 16
10	2.9	1.7	1.3		
20	4.3	2.1	1.7	1.3	
40	6.9	3.0	2.3	1.6	1.0
50	8.1	3.2	2.4	1.8	1.0
60	10.5	3.9	2.6	1.9	1.0
100	26.9	6.9	3.5	2.7	1.4
1000	6909.7	1354.5	238.4	46.6	7.8

TABLE V. Noise Level vs Data Rate and Turbo Mode Rate. (PGA gain setting of 1 and 10MHz clock.)

The Turbo Mode feature allows trade-offs to be made between the ADS1210/11 X_{IN} clock frequency, power dissipation, and effective resolution. If a 5MHz clock is available but a 10MHz clock is needed to achieve the desired performance, a Turbo Mode Rate of 2X will result in the same effective resolution. Table VI provides a comparison of effective resolution at various clock frequencies, data rates, and Turbo Mode Rates.

DATA RATE (Hz)	X_{IN} CLOCK FREQUENCY (MHz)	TURBO MODE RATE	EFFECTIVE RESOLUTION (Bits rms)
60	10	1	19.5
60	5	2	19.5
60	2.5	4	19.5
60	1.25	8	19.5
60	0.625	16	19.5
100	10	1	18.0
100	5	2	18.0
100	2.5	4	18.0
100	1.25	8	18.0
100	0.625	16	18.0

TABLE VI. Effective Resolution vs Data Rate, Clock Frequency, and Turbo Mode Rate. (PGA gain setting of one.)



ADS1210/1211

The Turbo Mode Rate is programmed via the Sampling Frequency Bits of the Command Register. Due to the increase in input capacitor sampling frequency, higher Turbo Mode settings result in lower analog input impedance;

$$\text{Typical Analog Input Impedance } (\Omega) = (10\text{MHz}/X_{\text{IN}} \text{ Clock Frequency}) \cdot 4.3\text{E}6 / (\text{G} \cdot \text{TMR})$$

where TMR is the Turbo Mode Rate. Because the modulator rate also changes in direct relation to the Turbo Mode setting, higher values result in a lower impedance for the REF_{IN} input:

$$\text{Typical } \text{REF}_{\text{IN}} \text{ Input Impedance } (\Omega) = (10\text{MHz}/ X_{\text{IN}} \text{ Clock Frequency}) \cdot 1\text{E}6 / \text{TMR}$$

The Turbo Mode Rate can be set to 1, 2, 4, 8, or 16. Consult the graphs shown in the Typical Performance Curves for full details on the performance of the ADS1210/11 operating in different Turbo Mode Rates. Keep in mind that higher Turbo Mode Rates result in fewer available gain settings as shown in Table II.

PROGRAMMABLE GAIN AMPLIFIER

The programmable gain amplifier gain setting is programmed via the PGA Gain Bits of the Command Register. Changes in the gain setting of the programmable gain amplifier results in an increase in the input capacitor sampling frequency. Thus, higher gain settings result in a lower analog input impedance:

$$\text{Typical Analog Input Impedance } (\Omega) = (10\text{MHz}/X_{\text{IN}} \text{ Clock Frequency}) \cdot 4.3\text{E}6 / (\text{G} \cdot \text{TMR})$$

where TMR is the Turbo Mode Rate. Because the modulator speed does not depend on the gain setting, the input impedance seen at REF_{IN} does not change.

The PGA can be set to gains of 1, 2, 4, 8, or 16. These gain settings with their resulting full-scale range and typical voltage range are shown in Table I. Keep in mind that higher Turbo Mode Rates result in fewer available gain settings as shown in Table II.

SOFTWARE GAIN

The excellent performance, flexibility, and low cost of the ADS1210/11 allow the converter to be considered for designs which would not normally need a 24-bit ADC. For example, many designs utilize a 12-bit converter and a high-gain INA or PGA for digitizing low amplitude signals. For some of these cases, the ADS1210/11 by itself may be a solution, even though the maximum gain is limited to 16.

To get around the gain limitation, the digital result can simply be shifted up by "n" bits in the main controller—resulting in a gain of "n" times G, where G is the gain setting. While this type of manipulation of the output data is obvious, it may not be immediate. In addition, it may be easy to miss how much the gain can be increased in this manner on a 24-bit converter.

For example, shifting the result up by three bits when the ADS1210/11 is set to a gain of 16 results in an effective gain of 128. At lower data rates, the converter can easily provide

more than 12 bits of resolution. Even higher gains are possible. The limitation is a combination of the needed data rate, desired noise performance, and desired linearity.

CALIBRATION

The ADS1210/11 offers several different types of calibration, and the particular calibration desired is programmed via the Command Register. In the case of Background Calibration, the calibration will repeat at regular intervals indefinitely. For all others, the calibration is performed once and then normal operation is resumed.

Each type of calibration is covered in detail in their respective section. In general, calibration is recommended immediately after power-on and whenever there is a "significant" change in the operating environment. The amount of change which should cause a re-calibration is dependent on the application, effective resolution, etc. Where high accuracy is important, re-calibration should be done on changes in temperature and power supply. In all cases, re-calibration should be done when the gain, Turbo Mode, or data rate is changed.

After a calibration has been accomplished, the Offset Calibration Register and the Full-Scale Calibration Register contain the results of the calibration. The data in these registers are accurate to the effective resolution of the ADS1210/11's mode of operation during the calibration. Thus, these values will show a variation (or noise) equivalent to a regular conversion result.

For those cases where this error must be reduced, it is tempting to consider running the calibration at a slower data rate and then increasing the converter's data rate after the calibration is complete. Unfortunately, this will not work as expected. The reason is that the results calculated at the slower data rate would not be valid for the higher data rate. Instead, the calibration should be done repeatedly. After each calibration, the results can be read and stored. After the desired number of calibrations, the main controller can compute an average and write this value into the calibration registers. The resulting error in the calibration values will be reduced by the square root of the number of calibrations which were averaged.

The calibration registers can also be used to provide system offset and gain corrections separate from those computed by the ADS1210/11. For example, these might be burned into E²PROM during product which uses the ADS1210/11 manufacture. On power-on, the main controller would load these values into the calibration registers. A further possibility is a look-up table based on temperature calibration done at the factory.

Note that the values in the calibration registers will vary from configuration to configuration and from part to part. There is no method of reliably computing what a particular calibration register should be to correct for a given amount of system error. It is possible to present the ADS1210/11 with a known amount of error, perform a calibration, read the desired calibration register, change the error value, perform another calibration, read the new value and use these values to interpolate an intermediate value.

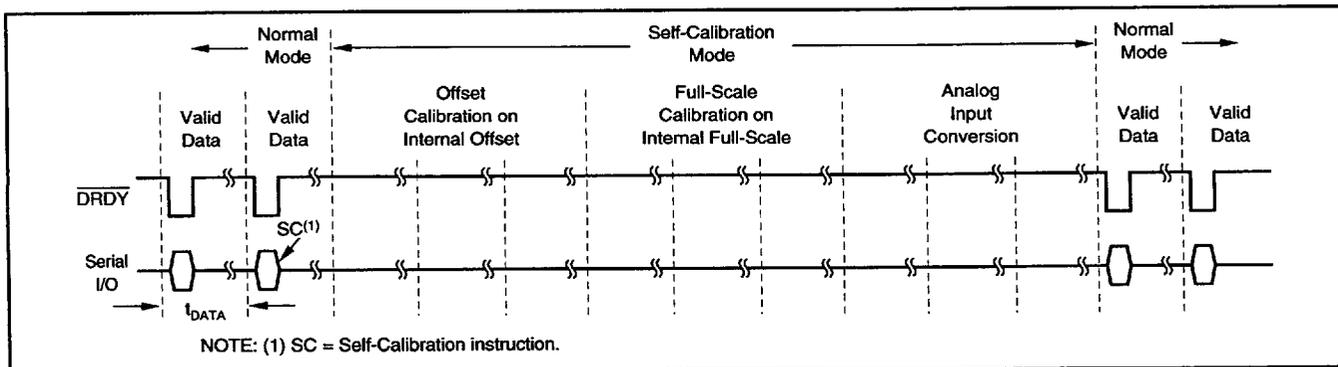


FIGURE 5. Self-Calibrating Timing Diagram.

Self Calibration

A self-calibration is performed after the bits 001 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following sequence at the start of the next conversion cycle (see Figure 5). The $\overline{\text{DRDY}}$ signal will not go LOW but will remain HIGH and will continue to remain HIGH throughout the calibration sequence. The inputs to the sampling capacitor are disconnected from the converter's analog inputs and are shorted together. An offset calibration is performed over the next three conversion periods. Then, the input to the sampling capacitor is connected across REF_{IN} , and a full-scale calibration is performed over the next three conversions.

After this, the Operation Mode bits are reset to 000 (normal mode) and the input capacitor is reconnected to the input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. $\overline{\text{DRDY}}$ remains HIGH during this time. On the start of the fourth cycle (tenth cycle since the calibration started), $\overline{\text{DRDY}}$ goes LOW indicating valid data and resumption of normal operation.

System Offset Calibration

A system offset calibration is performed after the bits 010 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following sequence (see Figure 6). At the start of the next conversion cycle, the $\overline{\text{DRDY}}$ signal will not go LOW but will remain HIGH and will continue to remain HIGH throughout the calibration sequence. The offset calibration will be performed on the differential input voltage present at the converter's input over the next three conversion periods. When this is done, the Operation Mode bits are reset to 000

(Normal Mode). A single conversion is done with $\overline{\text{DRDY}}$ HIGH. After this conversion, the $\overline{\text{DRDY}}$ signal goes LOW indicating resumption of normal operation.

Normal operation returns within a single conversion cycle because it is assumed that the input voltage at the converter's input is not removed immediately after the offset calibration is performed. In this case, the digital filter already contains a valid result. The extra conversion is performed in order to clean up the internal calibration state and to move the valid data to the Data Output Register.

For full system calibration, offset calibration must be performed first and then full-scale calibration. In addition, the offset calibration error will be the rms sum of the conversion error and the noise on the system offset voltage. See the System Calibration Limits section for information regarding the limits on the magnitude of the system offset voltage.

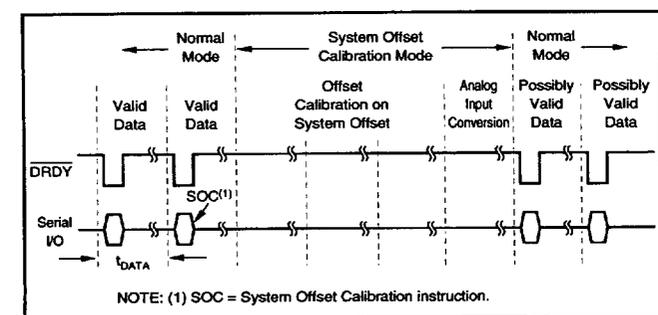


FIGURE 6. System Offset Calibration Timing.

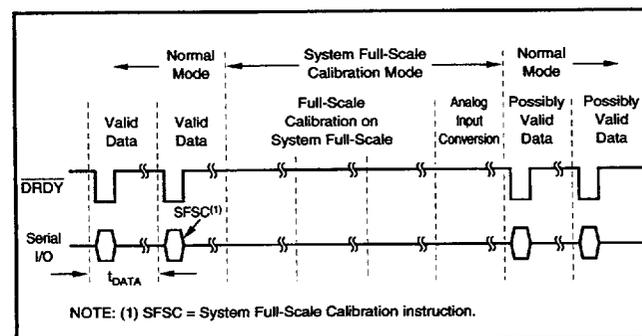


FIGURE 7. System Full-Scale Calibration Timing.

Normal operation returns within a single conversion cycle because it is assumed that the input voltage at the converter's input is not removed immediately after the full-scale calibration is performed. In this case, the digital filter already contains a valid result. The extra conversion is performed in order to clean up the internal calibration state and to move the valid data to the Data Output Register.

For full system calibration, offset calibration must be performed first and then full-scale calibration. The calibration error will be a sum of the rms noise on the conversion result and the input signal noise. See the System Calibration Limits section for information regarding the limits on the magnitude of the system full-scale voltage.

Pseudo System Calibration

The Pseudo System Calibration is performed after the bits 100 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following sequence (see Figure 8). At the start of the next conversion cycle, the DRDY signal will not go LOW but will remain HIGH and will continue to remain HIGH throughout the calibration sequence. The offset calibration will be performed on the differential input voltage present at the converter's input over the next three conversion periods. Then, the input to the sampling capacitor is disconnected from the converter's analog input and connected across REF_{IN}. A gain calibration is performed over the next three conversions.

After this, the Operation Mode bits are reset to 000 (normal mode) and the input capacitor is then reconnected to the input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. \overline{DRDY} remains HIGH during this time. On the start of the fourth cycle (tenth cycle since the calibration started), the \overline{DRDY} signal goes LOW indicating valid data and resumption of normal operation.

The system offset calibration range of the ADS1210/11 is limited and is listed in the Specifications Table. For more information on how to use these specifications, see the System Calibration Limits section. To calculate V_{OS} , use $2 \cdot \text{REF}_{IN}/\text{GAIN}$ for V_{FS} .

Background Calibration

The Background Calibration Mode is entered after the bits 101 have been written to the Command Register Operation Mode bits (MD2 through MD0). This initiates the following continuous sequence (see Figure 9). At the start of the next conversion cycle, the \overline{DRDY} signal will not go LOW but will remain HIGH. The inputs to the sampling capacitor are disconnected from the converter's analog input and shorted together. An offset calibration is performed over the next three conversion periods. Then, the input capacitor is reconnected to the input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. \overline{DRDY} remains HIGH during this time. On the start of the seventh cycle since the calibration was started, the \overline{DRDY} signal goes LOW indicating valid data.

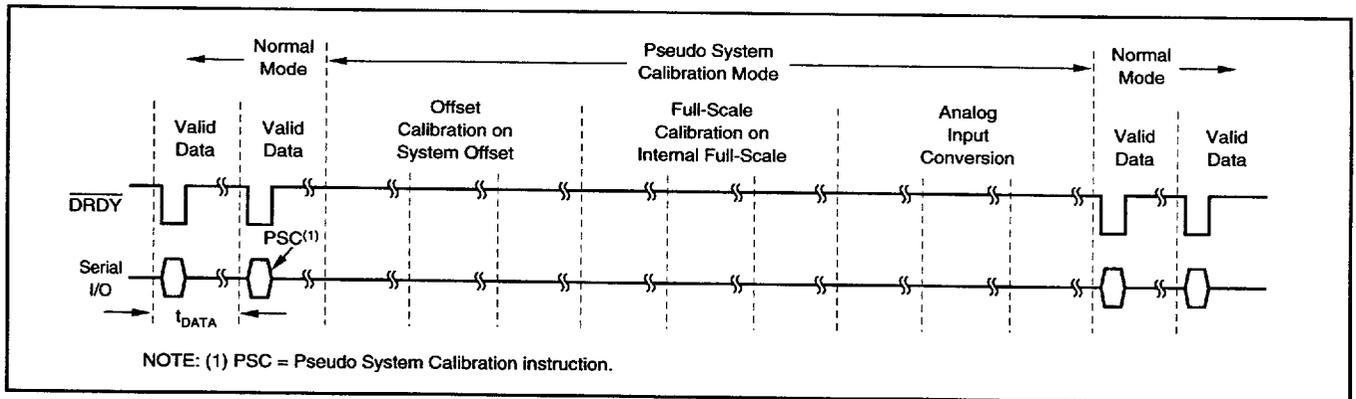


FIGURE 8. Pseudo System Calibration Timing.

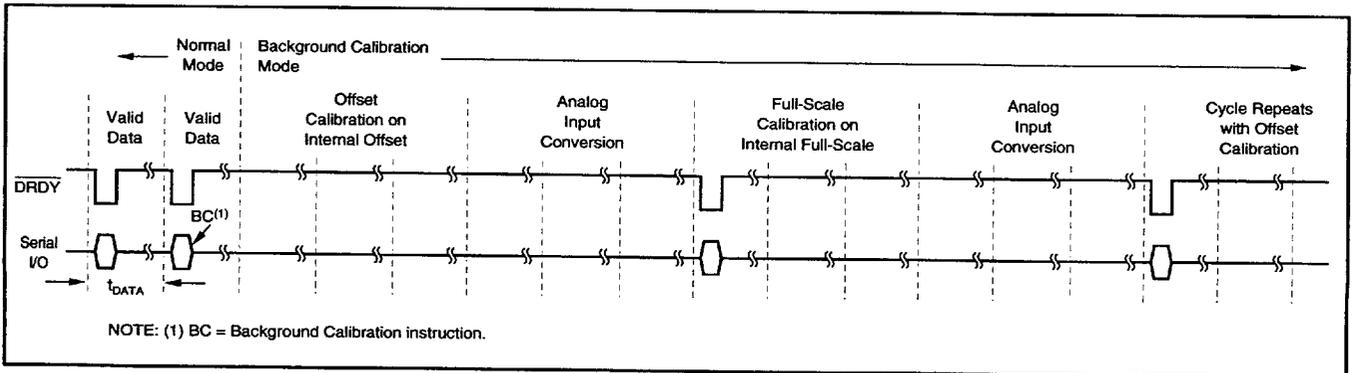


FIGURE 9. Background Calibration Timing.

Also, at the start of the seventh cycle, the sampling capacitor is disconnected from the converter's analog input and is connected across REF_{IN} . A gain calibration is initiated and proceeds over the next three conversions. After this, the input capacitor is once again connected to the analog input. Conversions proceed as usual over the next three cycles in order to fill the digital filter. $DRDY$ remains HIGH during this time. On the start of the thirteenth cycle, the $DRDY$ signal goes LOW indicating valid data, the input to the sampling capacitor is shorted, and an offset calibration is initiated. At this point, the Background Calibration sequence repeats.

In essence, the Background Calibration Mode performs continuous self-calibration where the offset and gain calibrations are interleaved with regular conversions. Thus, the data rate is reduced by a factor of 6. The advantage is that the converter is continuously adjusting to environmental changes such as ambient or component temperature (due to airflow variations).

The ADS1210/11 will remain in the Background Calibration mode indefinitely. To move to any other mode, the Command Register Operation Mode bits (MD2 through MD0) must be set to the appropriate values.

System Calibration Offset and Full-Scale Calibration Limits

The System Offset and Full-Scale Calibration range of the ADS1210/11 is limited and is listed in the Specifications Table. The range is specified as:

$$\begin{aligned} (V_{FS} - |V_{OS}|) &< 1.3 \cdot (2 \cdot REF_{IN})/GAIN \\ (V_{FS} - |V_{OS}|) &> 0.7 \cdot (2 \cdot REF_{IN})/GAIN \end{aligned}$$

where V_{FS} is the system full-scale voltage and $|V_{OS}|$ is the absolute value of the system offset voltage. In the following discussion, keep in mind that these voltages are differential voltages.

For example, with the internal reference (2.5V) and a gain of two, the previous equations become (after some manipulation):

$$V_{FS} - 3.25 < V_{OS} < V_{FS} - 1.75$$

If V_{FS} is perfect at 2.5V (positive full-scale), then V_{OS} must be greater than -0.75V and less than 0.75V. Thus, when offset calibration is performed, the positive input can be no more than 0.75V below or above the negative input. If this range is exceeded, the ADS1210/11 may not calibrate properly.

This calculation method works for all gains other than one. For a gain of one and the internal reference (2.5V), the equation becomes:

$$V_{FS} - 6.5 < V_{OS} < V_{FS} - 3.5$$

With a 5V positive full-scale input, V_{OS} must be greater than -1.5V and less than 1.5V. Since the offset represents a common-mode voltage and the input voltage range in a gain of one is 0V to 5V, a common-mode voltage will cause the actual input voltage to possibly go below 0V or above 5V. The specifications also show that for the specifications to be valid, the input voltage must not go below AGND by more than 30mV or above AV_{DD} by more than 30mV.

This will be an important consideration in many systems which use a 2.5V or greater reference, as the input range is constrained by the expected power supply variations. In addition, the expected full-scale voltage will impact the allowable offset voltage (and vice-versa) as the combination of the two must remain within the power supply and ground potentials, regardless of the results obtained via the range calculation shown previously.

There are only two solutions to this constraint: either the system design must ensure that the full-scale and offset voltage variations will remain within the power supply and ground potentials, or the part must be used in a gain of 2 or greater.

SLEEP MODE

The Sleep Mode is entered after the bits 110 have been written to the Command Register Operation Mode bits (MD2 through MD0). This mode is a permanent mode and is exited by entering a new mode into the MD2-MD0 bits.

The Sleep Mode causes the analog section and a good deal of the digital section to power down. For full analog power down, the V_{BIAS} generator and the internal reference must also be powered down by setting the BIAS and REFO bits in the Command Register accordingly. The power dissipation shown in the Specifications Table is with the internal reference and the V_{BIAS} generator disabled.

The Sleep Mode is exited depending on how the serial interface is configured. If \overline{CS} is being used, simply taking \overline{CS} LOW will enable serial communication to proceed normally. If \overline{CS} is not being used (tied LOW) and the ADS1210/11 is in the Master Mode, then a falling edge must be produced on the SDIO line. If SDIO is LOW, the SDIO line must be taken HIGH for $2 \cdot t_{XIN}$ periods (minimum) and then taken LOW. Alternatively, SDIO can be forced HIGH after putting the ADS1210/11 to "sleep" and then taken LOW when the Sleep Mode is to be exited. Finally, if \overline{CS} is not being used (tied LOW) and the ADS1210/11 is in the Slave Mode, then simply sending a normal Instruction Register command will enable the serial interface.

Once serial communication is resumed, the Sleep Mode is exited by changing the MD2-MD0 bits to any other mode. When a new mode (other than Sleep) has been entered, the ADS1210/11 will execute a very brief internal power-up sequence of the analog and digital circuitry. Once this has been done, one normal conversion cycle is performed before the new mode is actually entered. At the end of this conversion cycle, the new mode takes effect and the converter will respond accordingly. The $DRDY$ signal will remain HIGH through the first conversion cycle. It will also remain HIGH through the second, even if the new mode is the Normal Mode.

If the V_{BIAS} generator and/or the internal reference have been disabled, then they must be manually re-enabled via the appropriate bits in the Command Register. In addition, the internal reference will have to charge the external bypass capacitor(s) and possibly other circuitry. There may also be



considerations associated with V_{BIAS} and the settling of external circuitry. All of these must be taken into account when determining the amount of time required to resume normal operation. The timing diagram shown in Figure 10 does not take into account the settling of external circuitry.

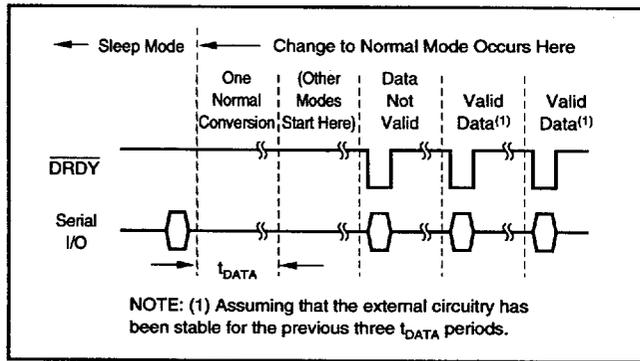


FIGURE 10. Sleep Mode to Normal Mode Timing.

ANALOG OPERATION

ANALOG INPUT

The input impedance of the analog input changes with ADS1210/11 clock frequency (f_{XIN}), gain (G), and Turbo Mode Rate (TMR). The relationship is:

$$A_{IN} \text{ Input Impedance } (\Omega) = (10\text{MHz}/f_{XIN}) \cdot 4.3\text{E}6 / (G \cdot \text{TMR})$$

Figure 11 shows the basic input structure of the ADS1210. The ADS1211 includes an input multiplexer, but this has little impact on the analysis of the input structure. The impedance is directly related to the sampling frequency of the input capacitor. The X_{IN} clock rate sets the basic sampling rate in a gain of 1 and Turbo Mode Rate of 1. Higher gains and higher Turbo Mode Rates result in an increase of the sampling rate, while slower clock (X_{IN}) frequencies result in a decrease.

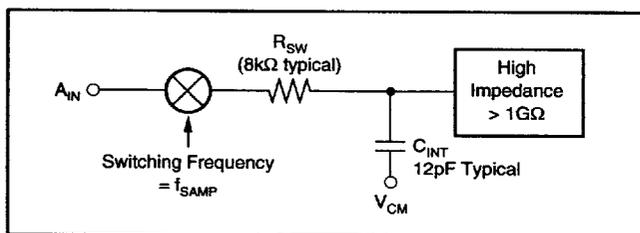


FIGURE 11. Analog Input Structure.

This input impedance can become a major point of consideration in some designs. If the source impedance of the input signal is significant or if there is passive filtering prior to the ADS1210/11, then a significant portion of the signal can be lost across this external impedance. How significant this effect is depends on the desired system performance.

There are two restrictions on the analog input signal to the ADS1210/11. Under no conditions should the current into or out of the analog inputs exceed 10mA. In addition, while

the analog signal must reside within this range, the linearity of the ADS1210/11 is only guaranteed when the actual analog input voltage resides within a range defined by $AGND \geq -30\text{mV}$ and $\leq AV_{DD} + 30\text{mV}$. This is due to leakage paths which occur within the part when $AGND$ and AV_{DD} are exceeded.

For this reason, the 0V to 5V input range (gain of 1 with a 2.5V reference) must be used with caution. Should AV_{DD} be 4.75V, the analog input signal would swing outside of the guaranteed specifications of the device. Designs utilizing this mode of operation should consider limiting the span to a slightly smaller range. Common-mode voltages are also a significant concern in this mode and must be carefully analyzed.

An input voltage range of 0.75V to 4.25V is the smallest span that is allowed if a full system calibration will be performed (see the Calibration section for more details). This also assumes an offset error of zero. A better choice would be 0.5V to 4.5V (a full-scale range of 9V). This span would allow some offset error, gain error, power supply error, and common-mode voltage while still providing full system calibration over reasonable variation in each of these parameters.

The actual input voltage exceeding $AGND$ or AV_{DD} should not be a concern in higher gain settings as the input voltage range will reside well within 0V to 5V. This is true unless the common-mode voltage is large enough to place positive full-scale or negative full-scale outside of the $AGND$ to AV_{DD} range.

REFERENCE INPUT

The input impedance of the REF_{IN} input changes with clock frequency (f_{XIN}) and Turbo Mode Rate (TMR). The relationship is:

$$REF_{IN} \text{ Input Impedance } (\Omega) = (10\text{MHz}/f_{XIN}) \cdot 1\text{E}6 / \text{TMR}$$

Unlike the analog input, the reference input impedance has a negligible dependency on the PGA gain setting. This is because the reference input drives a reference point in the modulator. Also, the sampling capacitance decreases with the PGA gain setting, which is balanced by an increase in the sampling rate.

The reference input voltage can vary between 2V and 3V. A nominal voltage of 2.5V appears at REF_{OUT} , and this can be directly connected to REF_{IN} . Higher reference voltages will cause the full-scale range to increase while the internal circuit noise of the converter remains approximately the same. This will increase the LSB weight but not the internal noise, resulting in increased signal-to-noise ratio and effective resolution. Likewise, lower reference voltages will decrease the signal-to-noise ratio and effective resolution.

REFERENCE OUTPUT

The ADS1210/11 contains an internal +2.5V reference. Tolerances, drift, noise, and other specifications for this reference are given in the Specification Table. Note that it is not designed to sink or to source more than 1mA of current. In addition, loading the reference with a dynamic or variable load is not recommended. This can result in small changes in reference voltage as the load changes.

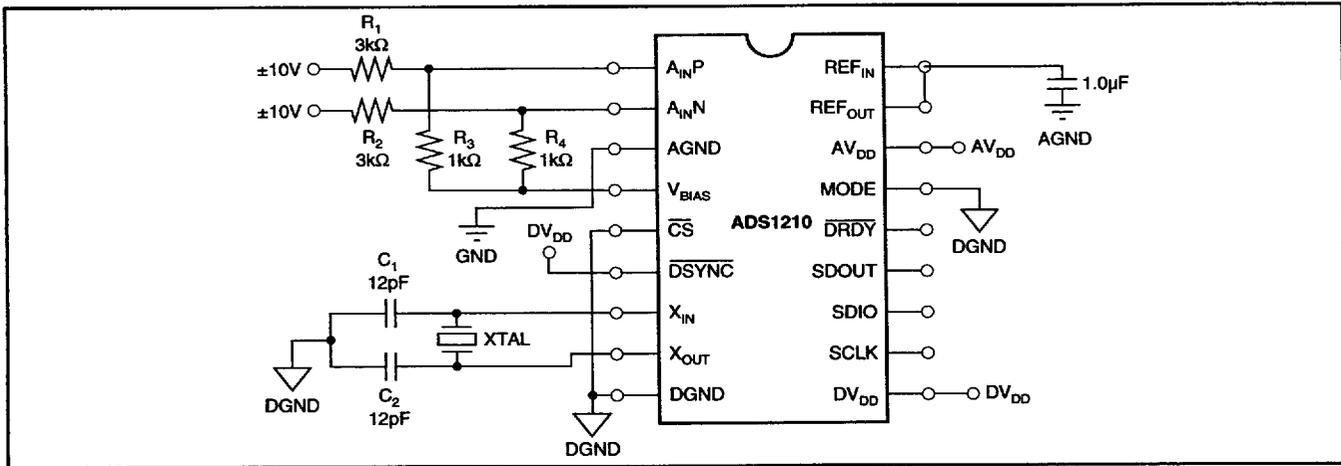


FIGURE 12. $\pm 10\text{V}$ Input Configuration Using V_{BIAS} .

The circuitry which generates the $+2.5\text{V}$ reference can be disabled via the Command Register and will result in a lower power dissipation. The reference circuitry consumes a little over 1.6mA of current with no external load. When the ADS1210/11 is in its default state, the internal reference is enabled.

V_{BIAS}

The V_{BIAS} output voltage is dependent on the reference input (REF_{IN}) voltage and is approximately 1.33 times as great. This output is used to bias input signals such that bipolar signals with spans of greater than 5V can be scaled to match the input range of the ADS1210/11. Figure 12 shows a connection diagram which will allow the ADS1210/11 to accept a $\pm 10\text{V}$ input signal (40V full-scale range).

This method of scaling and offsetting the $\pm 20\text{V}$ differential input signal will be a concern for those requiring minimum power dissipation. V_{BIAS} will supply 1.68mA for every channel connected as shown. For the ADS1211, the current draw is within the specifications for V_{BIAS} , but, at 12mW , the power dissipation is significant. If this is a concern, resistors R_1 and R_2 can be set to $9\text{k}\Omega$ and R_3 and R_4 to $3\text{k}\Omega$. This will reduce power dissipation by one-third. In addition, these resistors can also be set to values which will provide any arbitrary input range. In all cases, the maximum current into or out of V_{BIAS} should not exceed its specification of 10mA .

Note that the connection diagram shown in Figure 12 causes a constant amount of current to be sourced by V_{BIAS} . This will be very important in higher resolution designs as the voltage at V_{BIAS} will not change with loading, as the load is constant. However, if the input signal is single-ended and one side of the input is grounded, the load will not be constant and V_{BIAS} will change slightly with the input signal. Also, in all cases, note that noise on V_{BIAS} introduces a common-mode error signal which is rejected by the converter.

The circuitry to generate V_{BIAS} is disabled when the ADS1210/11 is in its default state, and it must be enabled, via the Command Register, in order for the V_{BIAS} voltage to be present. When enabled, the V_{BIAS} circuitry consumes approximately 1mA with no external load.

On power-up, external signals may be present before V_{BIAS} is enabled. This can create a situation in which a negative voltage is applied to the analog inputs (-2.5V for the circuit shown in Figure 12), reverse biasing the negative input protection diode. This situation should not be a problem as long as the resistors R_1 and R_2 limit the current being sourced by each analog input to under 10mA (a potential of 0V at the analog input pin should be used in the calculation).

DIGITAL OPERATION

SYSTEM CONFIGURATION

The Micro Controller (MC) consists of an ALU and a register bank. The MC has two states: power-on reset and convert. In the power-on reset state, the MC resets all the registers to their default state, sets up the modulator to a stable state, and performs self-calibration at a 850Hz data rate. After this, it enters the convert mode, which is the normal mode of operation for the ADS1210/11.

The ADS1210/11 has 5 internal registers, as shown in Table VII. Two of these, the Instruction Register and the Command Register, control the operation of the converter. The Data Output Register (DOR) contains the result from the most recent conversion. The Offset and Full-Scale Calibration Registers (OCR and FCR) contain data used for correcting the internal conversion result before it is placed into the DOR. The data in these two registers may be the result of a calibration routine, or they may be values which have been written directly via the serial interface.

INSR	Instruction Register	8 Bits
DOR	Data Output Register	24 Bits
CMR	Command Register	32 Bits
OCR	Offset Calibration Register	24 Bits
FCR	Full-Scale Calibration Register	24 Bits

TABLE VII. ADS1210/11 Registers.

Communication with the ADS1210/11 is controlled via the Instruction Register (INSR). Under normal operation, the INSR is written as the first part of each serial communication. The instruction that is sent determines what type of communication will occur next. It is not possible to read the INSR.

The Command Register (CMR) controls all of the ADS1210/11's options and operating modes. These include the PGA gain setting, the Turbo Mode Rate, the output data rate (decimation ratio), etc. The CMR is the only 32-bit register within the ADS1210/11. It, and all the remaining registers, may be read from or written to.

The Instruction Register (INSR)

The INSR is an 8-bit register which commands the serial interface either to read or to write "n" bytes beginning at the specified register location. Table VIII shows the format for the INSR.

MSB				LSB			
R/W	MB1	MB0	0	A3	A2	A1	A0

TABLE VIII. Instruction Register.

R/W (Read/Write) Bit—For a write operation to occur, this bit of the INSR must be 0. For a read, this bit must be 1, as follows:

R/W	
0	Write
1	Read

MB1, MB0 (Multiple Bytes) Bits—These two bits are used to control the word length (number of bytes) of the read or write operation, as follows:

MB1	MB0	
0	0	1 Byte
0	1	2 Bytes
1	0	3 Bytes
1	1	4 Bytes

A3-A0 (Address) Bits—These four bits select the beginning register location which will be read from or written to, as shown in Table IX. Each subsequent byte will be read from or written to the next higher location. (If the BD bit in the Command Register is set, each subsequent byte will be read from the next lower location. This bit does not affect the write operation.) If the next location is not defined in Table IX, then the results are unknown. Reading or writing continues until the number of bytes specified by MB1 and MB0 have been transferred.

A3	A2	A1	A0	REGISTER BYTE
0	0	0	0	Data Output Register Byte 2 (MSB)
0	0	0	1	Data Output Register Byte 1
0	0	1	0	Data Output Register Byte 0 (LSB)
0	1	0	0	Command Register Byte 3 (MSB)
0	1	0	1	Command Register Byte 2
0	1	1	0	Command Register Byte 1
0	1	1	1	Command Register Byte 0 (LSB)
1	0	0	0	Offset Cal Register Byte 2 (MSB)
1	0	0	1	Offset Cal Register Byte 1
1	0	1	0	Offset Cal Register Byte 0 (LSB)
1	1	0	0	Full-Scale Cal Register Byte 2 (MSB)
1	1	0	1	Full-Scale Cal Register Byte 1
1	1	1	0	Full-Scale Cal Register Byte 0 (LSB)

Note: MSB = Most Significant Byte, LSB = Least Significant Byte

TABLE IX. A3-A0 Addressing.

Each serial communication starts with the 8-bits of the INSR being sent to the ADS1210/11. This directs the remainder of the communication cycle, which consists of n bytes being read from or written to the ADS1210/11. The read/write bit, the number of bytes n, and the starting register address are defined, as shown in Table VIII. When the n bytes have been transferred, the INSR is complete. A new communication cycle is initiated by sending a new INSR (under restrictions outlined in the Interfacing section).

The Command Register (CMR)

The CMR controls all of the functionality of the ADS1210/11. The new configuration takes effect on the negative transition of the last bit in the last byte of data being written to the command register. The organization of the CMR is shown in Table X.

Most Significant Bit									Byte 3		
BIAS	REFO	DF	U/B	BD	MSB	SDL	DRDY				
0 Off	1 On	0 Two's	0 Bipol	0 MS to LS	0 MSB	0 SDIO	X				Defaults
Byte 2											
MD2	MD1	MD0	G2	G1	G0	CH1	CH0				
000 Normal Mode			000 Gain 1			00 Channel 1					Defaults
Byte 1											
SF2	SF1	SF0	DR12	DR11	DR10	DR9	DR8				
000 Turbo Mode rate of 1						00000					Defaults
Byte 0 Least Significant Byte											
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0				
(0000) 0001 0111 (23) Data Rate of 850Hz											Defaults

TABLE X. Organization of the Command Register and Default Status.

BIAS (Bias Voltage) Bit—The BIAS bit controls the V_{BIAS} output state—either on ($1.33 \cdot REF_{IN}$) or off (disabled), as follows:

BIAS	V_{BIAS} GENERATOR	V_{BIAS} STATUS	
0	Off	Disabled	Default
1	On	$1.33 \cdot REF_{IN}$	

The V_{BIAS} circuitry consumes approximately 1mA of steady state current with no external load. See the V_{BIAS} section for full details. When the internal reference (REF_{OUT}) is connected to the reference input (REF_{IN}), V_{BIAS} is 3.3V, nominal.

REFO (Reference Output) Bit—The REFO bit controls the internal reference (REF_{OUT}) state, either on (2.5V) or off (disabled), as follows:

REFO	INTERNAL REFERENCE	REF_{OUT} STATUS	
0	Off	High Impedance	Default
1	On	2.5V	

The internal reference circuitry consumes approximately 1.6mA of steady state current with no external load. See the Reference Output section for full details on the internal reference.

DF (Data Format) Bit—The DF bit controls the format of the output data, either Two's Complement or Offset Binary, as follows:

DF	FORMAT	ANALOG INPUT	DIGITAL OUTPUT	
0	Two's Complement	+Full-Scale Zero -Full Scale	7FFFFFF _H 000000 _H 800000 _H	Default
1	Offset Binary	+Full-Scale Zero -Full-scale	FFFFFF _H 800000 _H 000000 _H	

These two formats are the same for all bits except the most significant, which is simply inverted in one format vs the other. This bit only applies to the Data Output Register—it has no effect on the other registers.

U/B (Unipolar) Bit—The U/B bit controls the limits imposed on the output data, as follows:

U/B	MODE	LIMITS	
0	Bipolar	None	Default
1	Unipolar	Zero to +Full-Scale only	

The particular mode has no effect on the actual full-scale range of the ADS1210/11, data format, or data format vs input voltage. In the bipolar mode, the ADS1210/11 operates normally. In the unipolar mode, the conversion result is limited to positive values only (zero included). That is, when the Two's Complement format is selected, any negative conversion result (most significant bit is set) will result in 000000_H being placed in the Data Output Register. If the data format is Offset Binary, any result where the most significant bit is clear will result in 800000_H.

The Offset Register may contain negative values and any calibration sequences initiated when U/B is set will proceed normally. This bit only controls what is placed in the Data Output Register and is not related to the conversion in progress. When cleared, the very next conversion will produce a valid bipolar result.

BD (Byte Order) Bit—The BD bit controls the order in which bytes of data are read, either most significant byte first or least significant byte, as follows:

BD		
0	Byte Access from Most Significant Byte to Least Significant Byte	Default
1	Byte Access from Least Significant Byte to Most Significant Byte	

Note that when BD is clear and a multi-byte read is initiated, A3-A0 of the Instruction Register is the address of the most significant byte and subsequent bytes reside at higher addresses. If BD is set, then A3-A0 is the address of the least significant byte and subsequent bytes reside at lower addresses. The BD bit only affects read operations, it has no effect on write operations.

MSB (Bit Order) Bit—The MSB bit controls the order in which bits within a byte of data are read, either most significant bit first or least significant bit, as follows:

MSB		
0	Most Significant Bit First	Default
1	Least Significant Bit First	

The MSB bit only affects read operations, it has no effect on write operations.

SDL (Serial Data Line) Bit—The SDL bit controls which pin on the ADS1210/11 will be used as the serial data output pin, either SDIO or SDO_{UT}, as follows:

SDL	SERIAL DATA OUTPUT PIN	
0	SDIO	Default
1	SDO _{UT}	

If SDL is LOW, then SDIO will be used for both input and output of serial data—see the Timing section for more details on how the SDIO pin transitions between these two states. In addition, SDO_{UT} will remain in a tri-state condition at all times.

Important Note: Since the default condition is SDL LOW, SDIO has the potential of becoming an output once every data output cycle if the ADS1210/11 is in the Master Mode. This will occur until the Command Register can be written and the SDL bit set HIGH. This could present a problem if the SDIO pin is controlled by an output which is enabled when the SDIO pin also becomes an output. See the Interfacing section for more information.

DRDY (Data Ready) Bit—The DRDY bit is a read only bit which reflects the state of the ADS1210/11's DRDY output pin, as follows:

DRDY	MEANING
0	Data Ready
1	Data Not Ready

MD2-MD0 (Operating Mode) Bits—The MD2-MD0 bits initiate or enable the various calibration sequences, as follows:

MD2	MD1	MD0	OPERATING MODE
0	0	0	Normal Mode
0	0	1	Self-Calibration
0	1	0	System Offset Calibration
0	1	1	System Full-Scale Calibration
1	0	0	Pseudo System Calibration
1	0	1	Background Calibration
1	1	0	Sleep
1	1	1	Reserved

The Normal Mode, Background Calibration Mode, and Sleep Mode are permanent modes and the ADS1210/11 will remain in these modes indefinitely. All other modes are temporary and will revert to Normal Mode once the appropriate actions are complete. See the Calibration section for full details on the calibration modes. See the Sleep Mode section for more information on the Sleep Mode.

Data Rate (Hz)	Decimation Ratio	DR12	DR11	DR10	DR9	DR8	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	
1000	20	0	0	0	0	0	0	0	0	1	0	1	0	0	Default
850	23	0	0	0	0	0	0	0	0	1	0	1	1	1	
500	39	0	0	0	0	0	0	0	1	0	0	1	1	1	
250	78	0	0	0	0	0	0	1	0	0	1	1	1	0	
100	195	0	0	0	0	0	1	1	0	0	0	1	1	1	
60	326	0	0	0	0	1	0	1	0	0	0	1	1	0	
50	391	0	0	0	0	1	1	0	0	0	0	1	1	1	
20	977	0	0	0	1	1	1	1	0	1	0	0	0	1	
10	1953	0	0	1	1	1	1	0	1	0	0	0	0	1	

Table XI. Decimation Ratios vs Data Rates (Turbo Mode rate of 1 and 10MHz clock).

G2-G0 (PGA Control) Bits—The G2-G0 bits control the gain setting of the PGA, as follows:

G2	G1	G0	GAIN SETTING	AVAILABLE TURBO MODE RATES	
0	0	0	1	1-16	Default
0	0	1	2	1-8	
0	1	0	4	1-4	
0	1	1	8	1-2	
1	0	0	16	1	

The gain is partially implemented by increasing the input capacitor sampling frequency, which is given by the following equation:

$$f_{SAMP} = G \cdot TMR \cdot f_{XIN}/512$$

where G is the gain setting and TMR is the Turbo Mode Rate. The product of G and TMR cannot exceed 16. The sampling frequency of the input capacitor directly relates to the analog input impedance. See the Programmable Gain Amplifier and Analog Input sections for more details.

CH1-CH0 (Channel Selection) Bits—The CH1 and CH0 bits control the input multiplexer on the ADS1211, as follows:

CH1	CH0	ACTIVE INPUT	
0	0	Channel 1	Default
0	1	Channel 2	
1	0	Channel 3	
1	1	Channel 4	

(For the ADS1210, CH1 and CH0 must always be zero.) The channel change takes effect when the last bit of byte 2 has been written to the Command Register. Output data will not be valid for the next three conversions despite the \overline{DRDY} signal indicating that data is ready. On the fourth time that \overline{DRDY} goes LOW after a channel change has been written to the Command Register, valid data will be present in the Data Output Register (see Figure 4).

SF2-SF0 (Turbo Mode Rate) Bits—The SF2-SF0 bits control the input capacitor sampling frequency and modulator rate, as follows:

SF2	SF1	SF0	TURBO MODE RATE	AVAILABLE PGA GAIN SETTINGS	
0	0	0	1	1-16	Default
0	0	1	2	1-8	
0	1	0	4	1-4	
0	1	1	8	1-2	
1	0	0	16	1	

The input capacitor sampling frequency and modulator rate can be calculated from the following equations:

$$f_{SAMP} = G \cdot TMR \cdot f_{XIN}/512$$

$$f_{MOD} = TMR \cdot f_{XIN}/512$$

where G is the gain setting and TMR is the Turbo Mode Rate. The sampling frequency of the input capacitor directly relates to the analog input impedance. The modulator rate relates to the power consumption of the ADS1210/11 and the output data rate. See the Turbo Mode, Analog Input, and Reference Input sections for more details.

DR12-DR0 (Decimation Ratio) Bits—The DR12-DR0 bits control the decimation ratio of the ADS1210/11. In essence, these bits set the number of modulator results which are used in the digital filter to compute each individual conversion result. Since the modulator rate depends on both the ADS1210/11 clock frequency and the Turbo Mode Rate, the actual output data rate is given by the following equation:

$$f_{DATA} = f_{XIN} \cdot TMR / (512 \cdot \text{Decimation Ratio})$$

where TMR is the Turbo Mode Rate. Table XI shows various data rates and corresponding decimation ratios (with a 10MHz clock). Valid decimation ratios are from 20 to 8000. Outside of this range, the digital filter will compute results incorrectly due to inadequate or too much data.

Data Output Register (DOR)

The DOR is a 24-bit register which contains the most recent conversion result (see Table XII). This register is updated with a new result just prior to \overline{DRDY} going LOW. If the contents of the DOR are not read within a period of time defined by $1/f_{DATA} - 12 \cdot (1/f_{XIN})$, then a new conversion result will overwrite the old. (If \overline{DRDY} is not already HIGH, it is forced HIGH just before the DOR is updated.)

Most Significant Bit								Byte 2															
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16																
								Byte 1															
								DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR9	DOR8								
								Byte 0								Least Significant Byte							
								DOR7	DOR6	DOR5	DOR4	DOR3	DOR2	DOR1	DOR0								

TABLE XII. Data Output Register.

The contents of the DOR can be in Two's Complement or Offset Binary format. This is controlled by the DF bit of the Command Register. In addition, the contents can be limited to unipolar data only with the \overline{UB} bit of the Command Register.

Offset Calibration Register (OCR)

The OCR is a 24-bit register which contains the offset correction factor that is applied to the conversion result before it is placed in the Data Output Register (see Table XIII). In most applications, the contents of this register will be the result of either a self-calibration or a system calibration.

The OCR is both readable and writable via the serial interface. For applications requiring a more accurate offset calibration, multiple calibrations can be performed, each resulting OCR value read, the results averaged, and a more precise offset calibration value written back to the OCR.

The actual OCR value will change from part-to-part and with configuration, temperature, and power supply. Thus, the actual OCR value for any arbitrary situation cannot be accurately predicted. That is, a given system offset could not be corrected simply by measuring the error externally, computing a correction factor, and writing that value to the OCR. In addition, be aware that the contents of the OCR are not used to directly correct the conversion result. Rather, the correction is a function of the OCR value. This function is linear and two known points can be used as a basis for interpolating intermediate values for the OCR. Consult the Calibration section for more details.

Most Significant Bit				Byte 2			
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	DOR17	DOR16
Byte 1							
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	DOR9	DOR8
Byte 0				Least Significant Byte			
OCR7	OCR6	OCR5	OCR4	OCR3	OCR2	DOR1	DOR0

TABLE XIII. Offset Calibration Register.

The contents of the OCR are in Two's Complement format. This is not affected by the DF bit in the Command Register.

Full-Scale Calibration Register (FCR)

The FCR is a 24-bit register which contains the full-scale correction factor that is applied to the conversion result before it is placed in the Data Output Register (see Table XIV). In most applications, the contents of this register will be the result of either a self-calibration or a system calibration.

Most Significant Bit				Byte 2			
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
Byte 1							
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR9	FSR8
Byte 0				Least Significant Byte			
FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0

TABLE XIV. Full-Scale Calibration Register.

The FCR is both readable and writable via the serial interface. For applications requiring a more accurate full-scale calibration, multiple calibrations can be performed, each resulting FCR value read, the results averaged, and a more precise calibration value written back to the FCR.

The actual FCR value will change from part-to-part and with configuration, temperature, and power supply. Thus, the actual FCR value for any arbitrary situation cannot be accurately predicted. That is, a given system full-scale error cannot be corrected simply by measuring the error externally, computing a correction factor, and writing that value to the FCR. In addition, be aware that the contents of the FCR are not used to directly correct the conversion result. Rather, the correction is a function of the FCR value. This function is linear and two known points can be used as a basis for interpolating intermediate values for the FCR. Consult the Calibration section for more details. The contents of the FCR are in unsigned binary format. This is not affected by the DF bit in the Command Register.

TIMING

Table XV and Figures 13 through 21 define the basic digital timing characteristics of the ADS1210/11. Figure 13 and the associated timing symbols apply to the X_{IN} input signal. Figures 14 through 20 and associated timing symbols apply to the serial interface signals ($SCLK$, $SDIO$, $SDOUT$, and CS) and their relationship to $DRDY$. The serial interface is discussed in detail in the Serial Interface section. Figure 21 and the associated timing symbols apply to the maximum $DRDY$ rise and fall times.

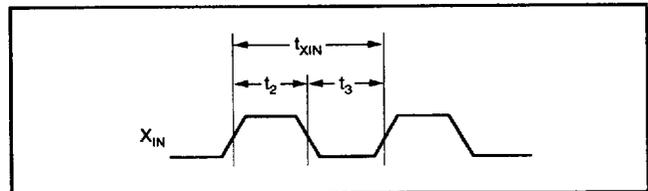


FIGURE 13. X_{IN} Clock Timing.

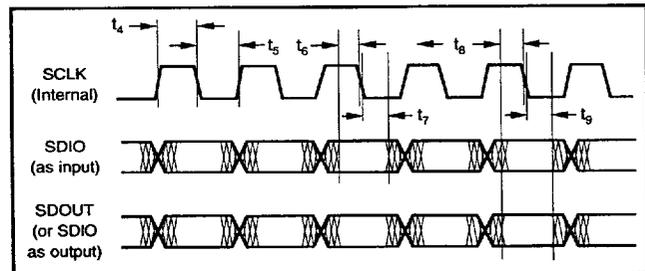


FIGURE 14. Serial Input/Output Timing, Master Mode.

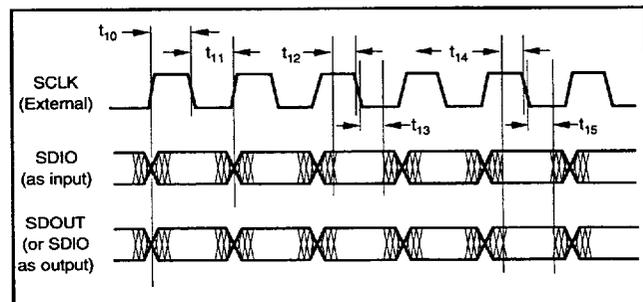


FIGURE 15. Serial Input/Output Timing, Slave Mode.

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNITS
f_{XIN}	X_{IN} Clock Frequency	0.5		10	MHz
t_{XIN}	X_{IN} Clock Period	100		2000	ns
t_2	X_{IN} Clock High	$0.4 \cdot t_{XIN}$			ns
t_3	X_{IN} Clock LOW	$0.4 \cdot t_{XIN}$			ns
t_4	Internal Serial Clock HIGH		t_{XIN}		ns
t_5	Internal Serial Clock LOW		t_{XIN}		ns
t_6	Data In Valid to Internal SCLK Falling Edge (Setup)	40			ns
t_7	Internal SCLK Falling Edge to Data In Not Valid (Hold)	20			ns
t_8	Data Out Valid to Internal SCLK Falling Edge (Setup)	$t_{XIN} - 25$			ns
t_9	Internal SCLK Falling Edge to Data Out Not Valid (Hold)	t_{XIN}			ns
t_{10}	External Serial Clock HIGH	$2.5 \cdot t_{XIN}$			ns
t_{11}	External Serial Clock LOW	$2.5 \cdot t_{XIN}$			ns
t_{12}	Data In Valid to External SCLK Falling Edge (Setup)	40			ns
t_{13}	External SCLK Falling Edge to Data In Not Valid (Hold)	20			ns
t_{14}	Data Out Valid to External SCLK Falling Edge (Setup)	$t_{XIN} - 40$			ns
t_{15}	External SCLK Falling Edge to Data Out Not Valid (Hold)	t_{XIN}			ns
t_{16}	Falling Edge of \overline{DRDY} to First SCLK Rising Edge (Master and Slave Modes, \overline{CS} Tied LOW)		$6 \cdot t_{XIN}$		ns
t_{17}	Falling Edge of Last SCLK for INSR to Rising Edge of First SCLK for Register Data (Master Mode)		$5 \cdot t_{XIN}$		ns
t_{18}	Falling Edge of Last SCLK for Register Data to Rising Edge of \overline{DRDY} (Master Mode)		$3 \cdot t_{XIN}$		ns
t_{19}	Falling Edge of Last SCLK for INSR to Rising Edge of First SCLK for Register Data (Slave Mode)	$5.5 \cdot t_{XIN}$			ns
t_{20}	Falling Edge of Last SCLK for Register Data to Rising Edge of \overline{DRDY} (Slave Mode)	$3 \cdot t_{XIN}$		$4 \cdot t_{XIN}$	ns
t_{21}	Falling Edge of \overline{DRDY} to Falling Edge of \overline{CS} (Master and Slave Mode)	t_{XIN}			ns
t_{22}	Falling Edge of \overline{CS} to Rising Edge of SCLK (Master Mode)	$5 \cdot t_{XIN}$		$6 \cdot t_{XIN}$	ns
t_{23}	Rising Edge of \overline{DRDY} to Rising Edge of \overline{CS} (Master and Slave Mode)	10			ns
t_{24}	Falling Edge of \overline{CS} to Rising Edge of SCLK (Slave Mode)		$5.5 \cdot t_{XIN}$		ns
t_{25}	Falling Edge of Last SCLK for INSR to SDIO Tri-state (Master Mode)		$2 \cdot t_{XIN}$		ns
t_{26}	SDIO as Output to Rising Edge of First SCLK for Register Data (Master and Slave Modes)		$2 \cdot t_{XIN}$		ns
t_{27}	Falling Edge of Last SCLK for INSR to SDIO Tri-state (Slave Mode)	$2 \cdot t_{XIN}$		$3 \cdot t_{XIN}$	ns
t_{28}	SDIO Tri-state Time (Master and Slave Modes)		t_{XIN}		ns
t_{29}	Falling Edge of Last SCLK for Register Data to SDIO Tri-State (Master Mode)	t_{XIN}			ns
t_{30}	Falling Edge of Last SCLK for Register Data to SDIO Tri-state (Slave Mode)	t_{XIN}		$2 \cdot t_{XIN}$	ns
t_{31}	\overline{DRDY} Fall Time			30	ns
t_{32}	\overline{DRDY} Rise Time			30	ns
t_{33}	Minimum \overline{DSYNC} LOW Time	$10.5 \cdot t_{XIN}$			ns
t_{34}	\overline{DSYNC} Valid HIGH to Rising Edge of X_{IN} (for Exact Synchronization of Multiple Converters only)	10			ns
t_{35}	Rising Edge of X_{IN} to \overline{DSYNC} Not Valid LOW (for Exact Synchronization of Multiple Converters only)	10			ns
t_{36}	Falling Edge of Last SCLK for Register Data to Rising Edge of First SCLK of next INSR (Slave Mode, \overline{CS} Tied LOW)	$20.5 \cdot t_{XIN}$			ns
t_{37}	Rising Edge of \overline{CS} to Falling Edge of \overline{CS} (Slave Mode, Using \overline{CS})	$10.5 \cdot t_{XIN}$			ns

TABLE XV. Digital Timing Characteristics.

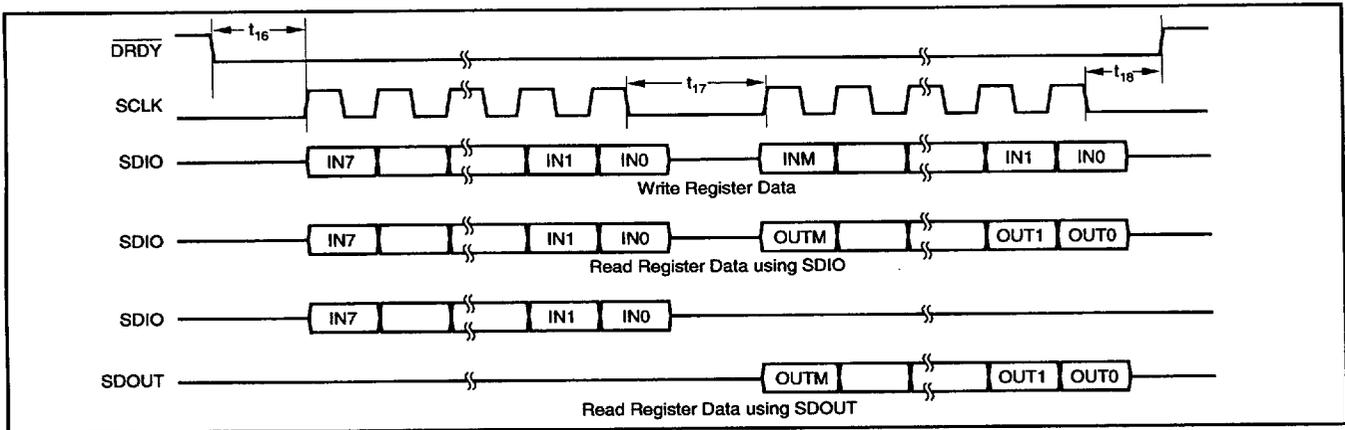


FIGURE 16. Serial Interface Timing (\overline{CS} Tied LOW), Master Mode.

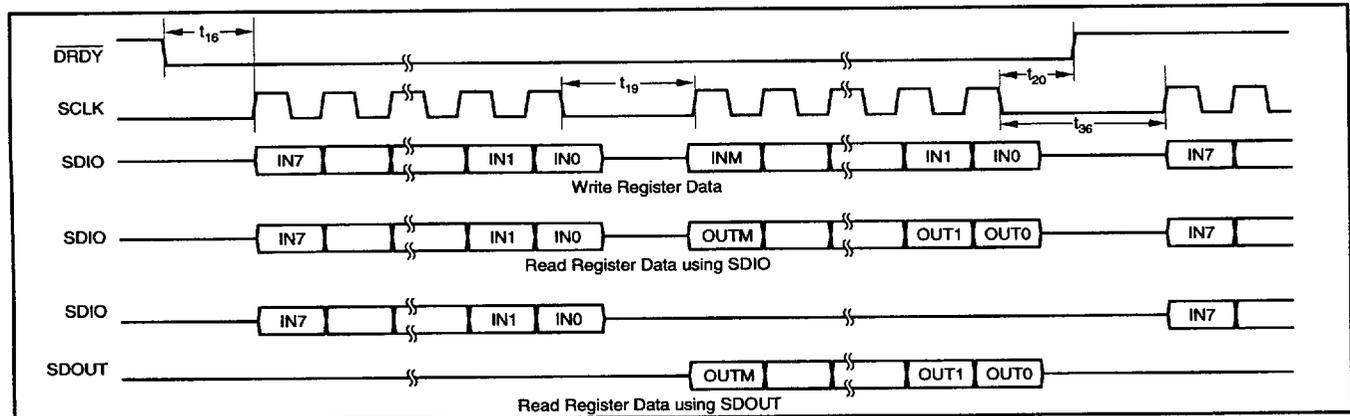


FIGURE 17. Serial Interface Timing (\overline{CS} Tied LOW), Slave Mode.

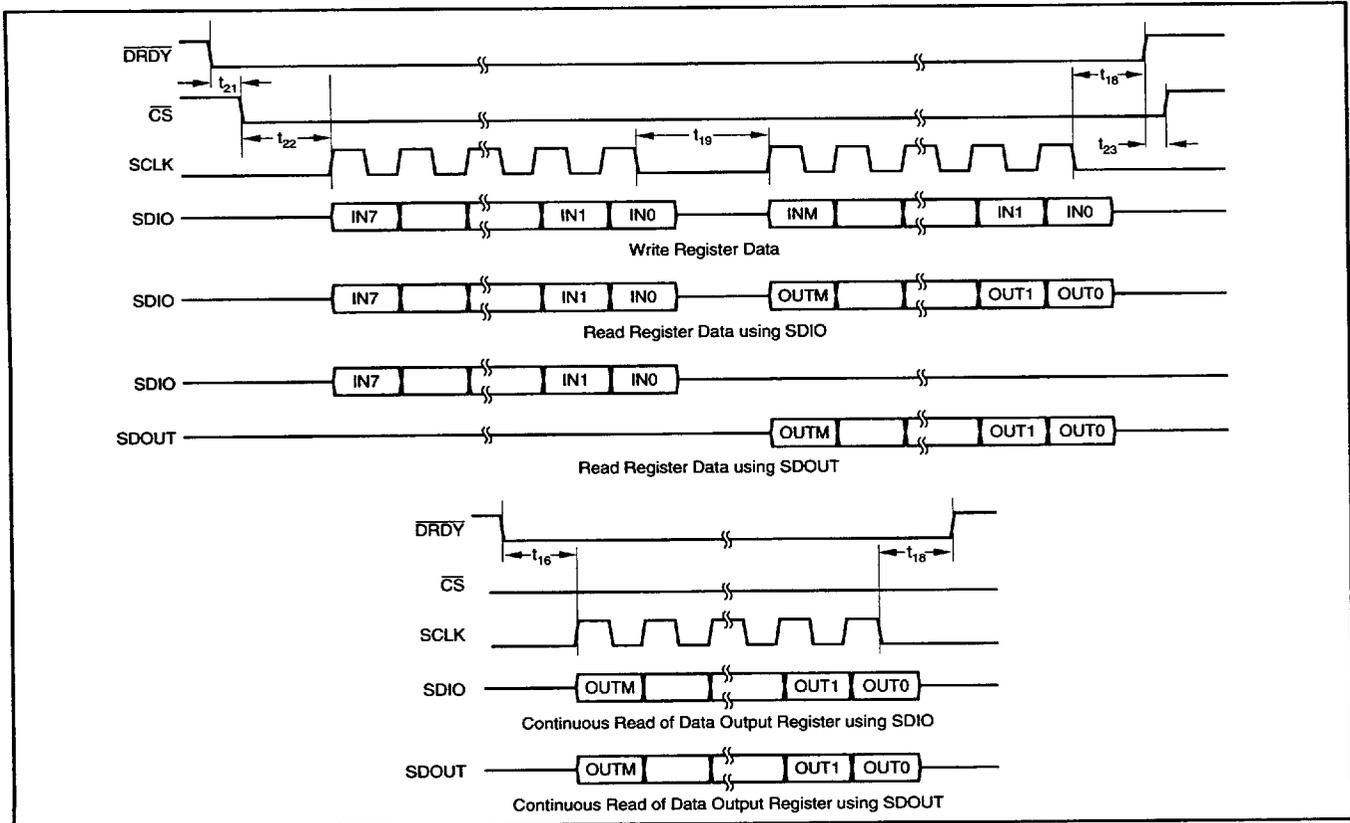


FIGURE 18. Serial Interface Timing (Using \overline{CS}), Master Mode.

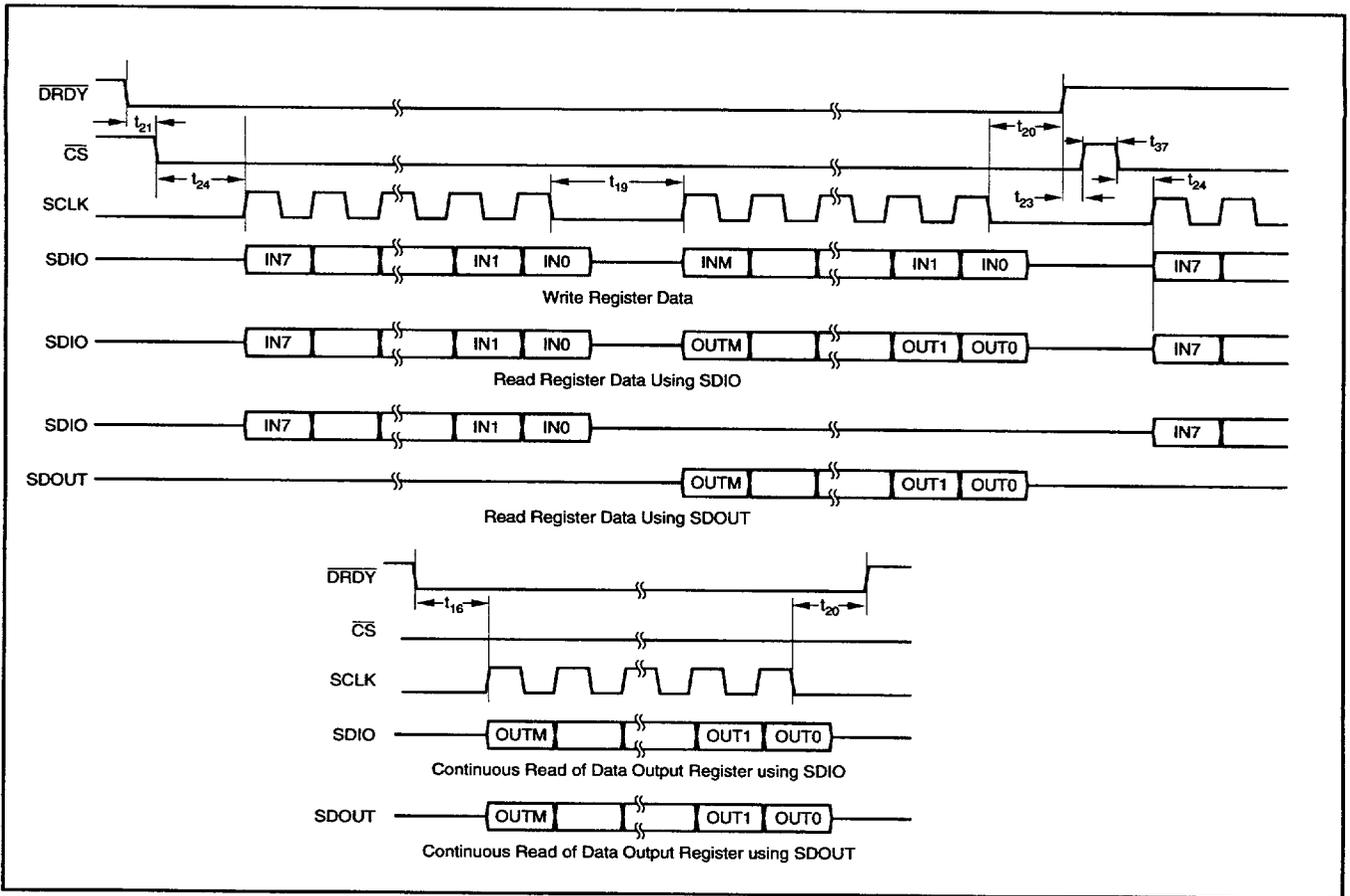


FIGURE 19. Serial Interface Timing (Using \overline{CS}), Slave Mode.

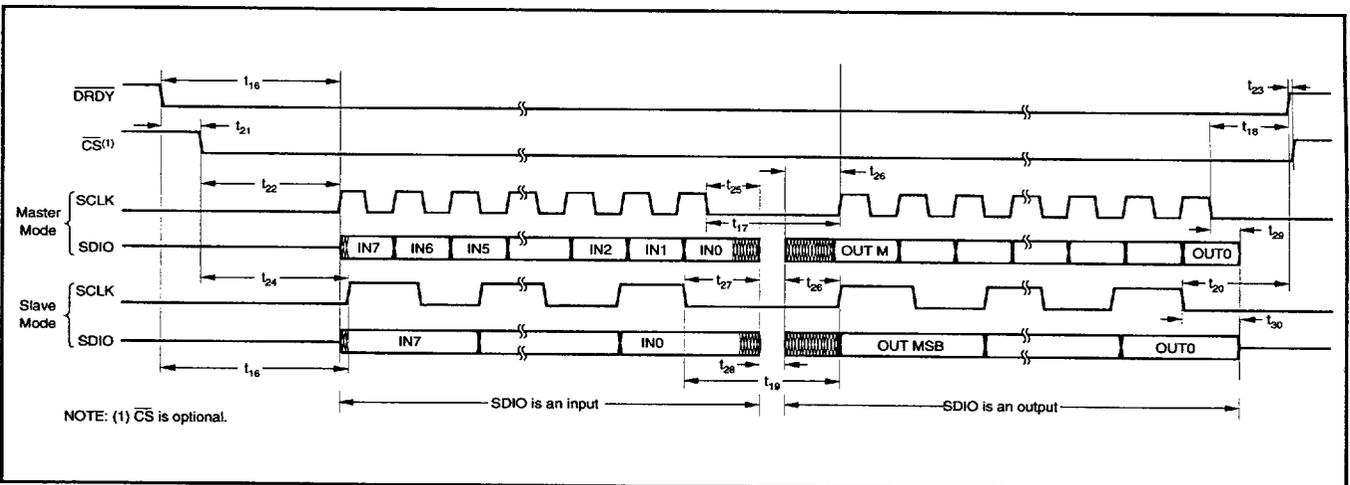


FIGURE 20. SDIO Input to Output Transition Timing.

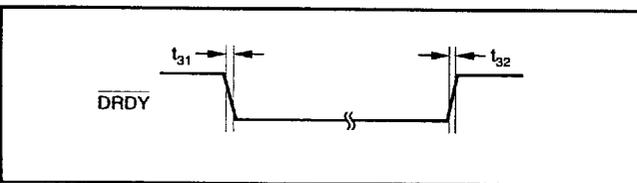


FIGURE 21. \overline{DRDY} Rise and Fall Time.

Synchronizing Multiple Converters

By placing a short low pulse on the $\overline{\text{DSYNC}}$ input, the data output of multiple ADS1210/11s can be synchronized. This assumes that each ADS1210 is driven from the same master clock and is set to the same Decimation Ratio and Turbo Mode Rate. The affect that this signal has on data output timing in general is discussed in the Serial Interface section.

The concern here is what happens if the $\overline{\text{DSYNC}}$ input is completely asynchronous to this master clock. If the $\overline{\text{DSYNC}}$ input rises at a critical point in relation to the master clock input, then some ADS1210/11s may start-up one X_{IN} clock cycle before the others. Thus, the output data will be synchronized, but only to within one X_{IN} clock cycle.

For many applications, this will be more than adequate. In these cases, the timing symbols which relate the $\overline{\text{DSYNC}}$ signal to the X_{IN} signal can be ignored. For other multiple-converter applications, this one X_{IN} clock cycle difference could be a problem. These types of applications would include using the $\overline{\text{DRDY}}$ and/or the SCLK output from one ADS1210/11 as the "master" signal for all converters.

To ensure exact synchronization to the same X_{IN} edge, the timing relationship between the $\overline{\text{DSYNC}}$ and X_{IN} signals, as shown in Figure 22, must be observed. Figure 23 shows a simple circuit which can be used to clock multiple ADS1210/11s from one ADS1210/11, as well as to ensure that an asynchronous $\overline{\text{DSYNC}}$ signal will exactly synchronize all the converters.

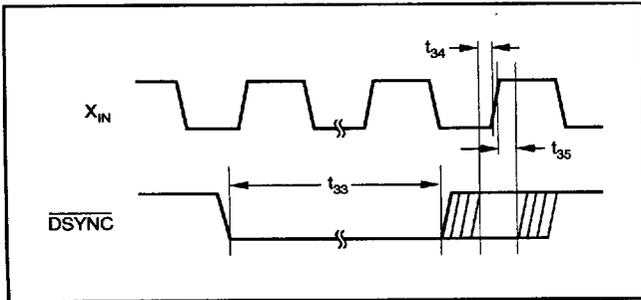


FIGURE 22. $\overline{\text{DSYNC}}$ to X_{IN} Timing for Synchronizing Multiple ADS1210/11s.

SERIAL INTERFACE

The ADS1210/11 includes a flexible serial interface which can be connected to microcontrollers and digital signal processors in a variety of ways. Along with this flexibility, there is also a good deal of complexity. This section describes the trade-offs between the different types of interfacing methods in a top-down approach—starting with the overall flow and control of serial data, moving to specific interface examples, and then providing information on various issues related to the serial interface.

Multiple Instructions

The general timing diagrams which appear throughout this data sheet show serial communication to and from the ADS1210/11 occurring during the $\overline{\text{DRDY}}$ LOW period (see Figures 4 through 10 and Figure 36). This communication represents one instruction that is executed by the ADS1210/11, resulting in a single read or write of register data.

However, more than one instruction can be executed by the ADS1210/11 during any given conversion period (see Figure 24). Note that $\overline{\text{DRDY}}$ remains HIGH during the subsequent instructions. There are several important restrictions on how and when multiple instructions can be issued during any one conversion period.

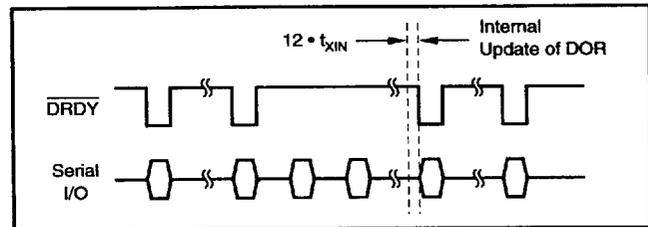


FIGURE 24. Timing of Data Output Register Update.

The first restriction is that the converter must be in the Slave Mode. There is no provision for multiple instructions when the ADS1210/11 is operating in the Master Mode. The second is that some instructions will produce invalid results if started at the end of one conversion period and carried into the start of the next conversion period.

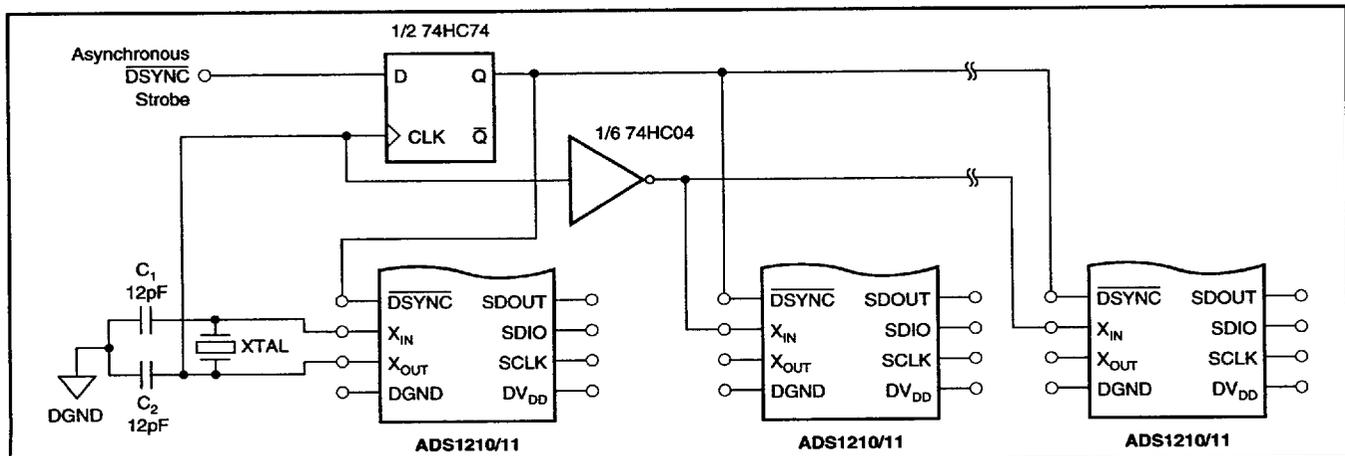


FIGURE 23. Exactly Synchronizing Multiple ADS1210/11s to an Asynchronous $\overline{\text{DSYNC}}$ Signal.

For example, Figure 24 shows that just prior to the $\overline{\text{DRDY}}$ signal going LOW, the internal Data Output Register (DOR) is updated. This update involves the Offset Calibration Register (OCR) and the Full-Scale Register (FSR). If the DOR is being read at the time, the results may be a mix of the last result and the current result, or invalid data. If the OCR or FSR are being written, their final value may not be correct, and the result placed into the DOR will certainly not be valid. Problems can also arise if certain bits of the Command Register are being changed.

In general, multiple instructions may be issued, but the last one in any conversion period should be complete within $12 \cdot X_{\text{IN}}$ clock periods of the next $\overline{\text{DRDY}}$ LOW time. In this usage, "complete" refers to the point where $\overline{\text{DRDY}}$ rises in Figures 17 and 19 (in the Timing Section). Consult Figures 25 and 26 for the flow of serial data during any one conversion period. Figure 25 applies to the Master Mode and Figure 26 to the Slave Mode.

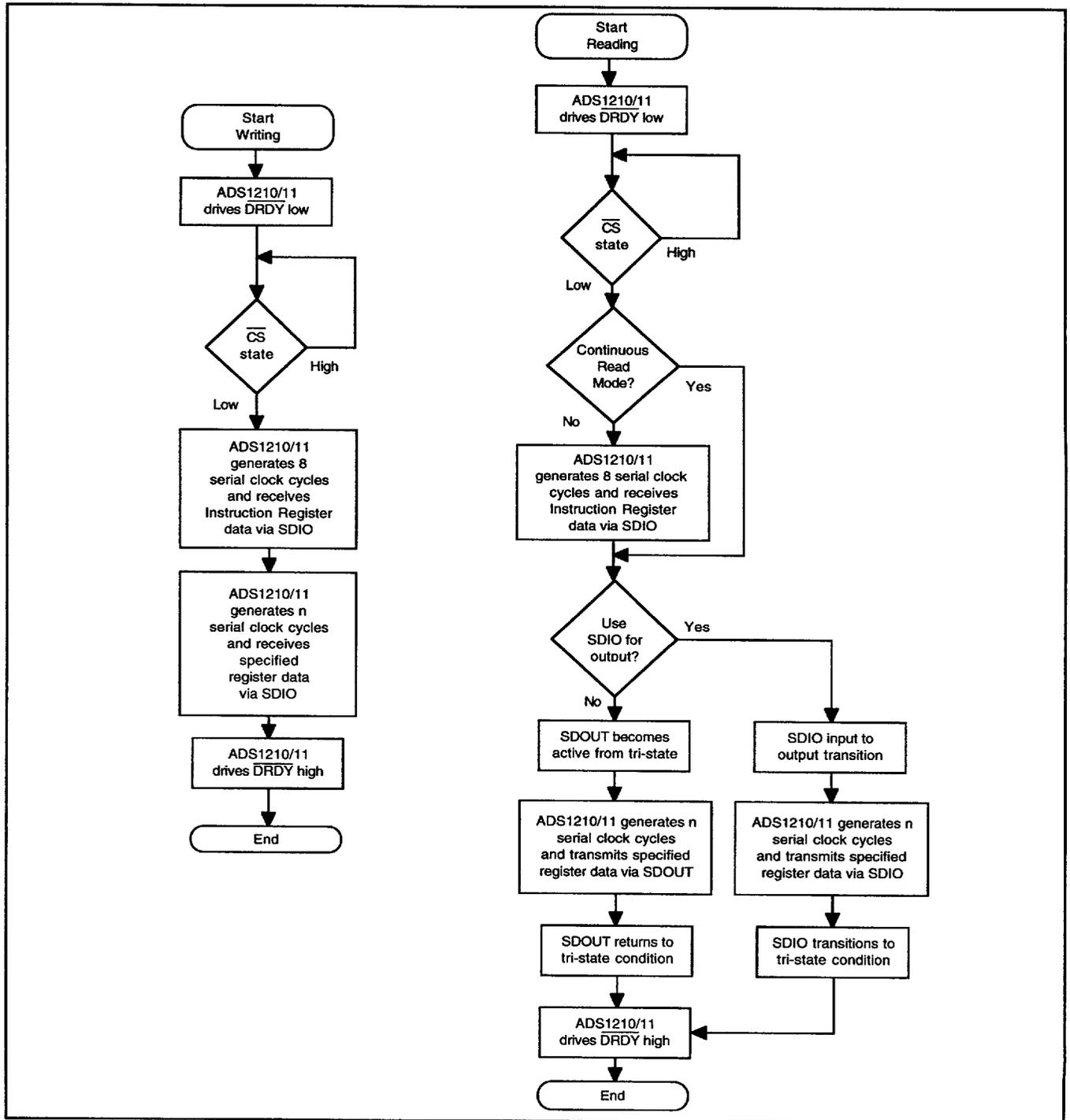


FIGURE 25. Flowchart for Writing and Reading Register Data, Master Mode.

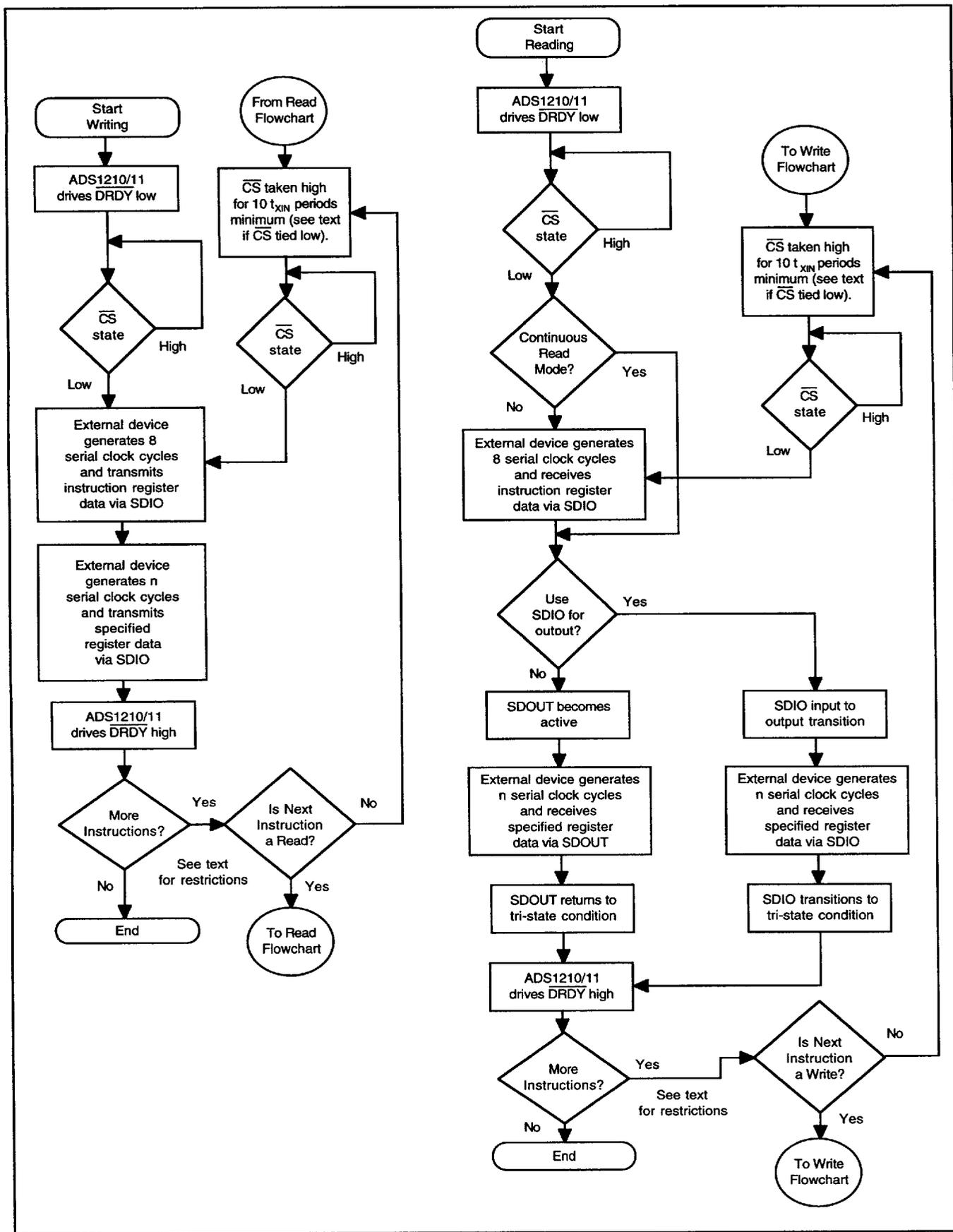


FIGURE 26. Flowchart for Writing and Reading Register Data, Slave Mode.

Using CS and Continuous Read Mode

The serial interface may make use of the \overline{CS} signal, or this input may simply be tied LOW. There are several issues associated with choosing to do one or the other.

The \overline{CS} signal does not directly control the tri-state condition of the SDO_{OUT} or SDIO output. These signals are normally in the tri-state condition. They only become active when serial data is being transmitted from the ADS1210/11. If the ADS1210/11 is in the middle of a serial transfer and SDO_{OUT} or SDIO is an output, taking \overline{CS} HIGH will not tri-state the output signal.

If there are multiple serial peripherals utilizing the same serial I/O lines and communication may occur with any peripheral at any time, then the \overline{CS} signal must be used. The ADS1210/11 may be in the Master Mode or the Slave Mode. In the Master Mode, the \overline{CS} signal is used to hold-off serial communication with a "ready" (\overline{DRDY} LOW) ADS1210/11 until the main controller can accommodate the communication. In the Slave Mode, the \overline{CS} signal can be used to gate the serial clock to the ADS1210/11. (If this is not done, the ADS1210/11 will think that another instruction is being issued when there is activity on the serial clock line.)

The \overline{CS} input has another use. If the \overline{CS} state is left LOW after a read of the Data Output Register has been performed, then the next time that \overline{DRDY} goes LOW, the ADS1210/11 Instruction Register will not be entered. Instead, the Instruction Register contents will be re-used, and the new contents of the Data Output Register, or some part thereof, will be transmitted. This will occur as long as \overline{CS} is LOW and not toggled.

This mode of operation is called the Continuous Read Mode and is shown in the read flowcharts of Figures 25 and 26. It is also shown in the Timing Diagrams of Figures 18 and 19 in the Timing section. Note that once \overline{CS} has been taken HIGH, the Continuous Read Mode is enabled (but not entered) and can never be disabled. The mode is actually entered and exited as described previously.

Because of the Continuous Read Mode, \overline{CS} must be used carefully. For example, consider the following situation: The \overline{CS} signal is being used to enable the ADS1210/11 for data transfer. \overline{DRDY} goes LOW to indicate that new data is ready but the main controller cannot get to the serial transfer right away. After some time, the main controller reads the new data. Before the controller sets the \overline{CS} HIGH, an interrupt occurs and the main controller goes off on an interrupt routine. At this point, the original delay, transfer time, and interrupt time have been enough that new data is now ready and \overline{DRDY} goes LOW. In this case, the ADS1210/11 is now in the Continuous Read Mode and will be expecting to transmit the Data Output Register immediately once \overline{CS} goes LOW, without receiving a new instruction.

POWER-ON CONDITIONS FOR SDIO

Even if the SDIO connection will be used only for input, there is one important item to consider regarding SDIO. This only applies when the ADS1210/11 is in the Master Mode

and \overline{CS} will be tied LOW. At power-up, the serial I/O lines of most microcontrollers and digital signal processors will be in a tri-state condition, or they will be configured as inputs. When power is applied to the ADS1210/11, it will begin operating as defined by the default condition of the Command Register (see Table X in the System Configuration section). This condition defines SDIO as the data output pin.

Since the ADS1210/11 is the Master Mode and \overline{CS} is tied LOW, the serial clock will run whenever \overline{DRDY} is LOW and an instruction will be entered and executed. If the SDIO line is HIGH, as it might be with an active pull-up, then the instruction is a read operation and SDIO will become an output every \overline{DRDY} LOW period—for 32 serial clock cycles. When the serial port on the main controller is enabled, signal contention could result.

The recommended solution to this problem is to actively pull SDIO LOW. If SDIO is LOW when the ADS1210/11 enters the instruction byte, then the resulting instruction is a write of one byte of data to the Data Output Register, which results in no internal operation.

If the SDIO signal cannot be actively pulled LOW, then another possibility is to time the initialization of the controller's serial port such that it becomes active between adjacent \overline{DRDY} LOW periods. The default configuration for the ADS1210/11 produces a data rate of 850Hz—a conversion period of 1.2ms. This time should be more than adequate for most microcontrollers and DSPs to monitor \overline{DRDY} and initialize the serial port at the appropriate time.

Master Mode

The Master Mode is active when the MODE input is HIGH. All serial clock cycles will be produced by the ADS1210/11 in this mode, and the SCLK pin is configured as an output. The frequency of the serial clock will be one-half of the X_{IN} frequency. Multiple instructions cannot be issued during a single conversion period in this mode—only one instruction per conversion cycle is possible.

The Master Mode will be difficult for some microcontrollers, particularly when the X_{IN} input frequency is greater than a few MHz, as the serial clock may exceed the microcontroller's maximum serial clock frequency. For the majority of digital signal processors, this will be much less of a concern. In addition, if SDIO is being used as an input and an output, then the transition time from input to output may be a concern. This will be true for both microcontrollers and DSPs. See Figure 20 in the Timing section.

Note that if \overline{CS} is tied LOW, there are special considerations regarding SDIO as outlined previously in this section. Also note that if \overline{CS} is being used to control the flow of data from the ADS1210/11 and it remains HIGH for one conversion period, the ADS1210/11 will operate properly. However, the results in the Data Output Register will be lost when they are overwritten by the new result at the start of the next conversion period. Just prior to this update, \overline{DRDY} will be forced HIGH and will return LOW after the update.

Slave Mode

Most systems will use the ADS1210/11 in the Slave Mode. This mode allows multiple instructions to be issued per conversion period as well as allowing the main controller to set the serial clock frequency and pace the serial data transfer. The ADS1210/11 is in the Slave mode when the MODE input is LOW.

There are several important items regarding the serial clock for this mode of operation. The maximum serial clock frequency cannot exceed the ADS1210/11 X_{IN} frequency divided by 5 (see Figure 15 in the Timing section). In addition, the serial clock must be synchronous to the X_{IN} input signal. If it is not, two simple ways of synchronizing the two are shown in Figure 27.

All of the timing diagrams and values given in the Timing section which apply to the Slave Mode of operation are given with respect to the circuits in Figure 27. That is, timing values which relate signals to the external serial clock must be met at the input of the D-type flip-flop, not at the serial clock input of the ADS1210/11. Thus, the numbers include the possible delay of the serial clock by one X_{IN} cycle and this does not have to be considered by the system designer.

As with the Master Mode of operation, when using SDIO as both an input and output, the SDIO transition time from input to output must be carefully considered. At the falling edge of the last serial clock cycle of the instruction byte, the SDIO pin will begin its transition from input to output. Between three and four X_{IN} cycles after this falling edge, the SDIO pin will become an output. This transition may be too fast for some microcontrollers and digital signal processors.

If a serial communication does not occur during any conversion period, the ADS1210/11 will continue to operate properly. However, the results in the Data Output Register will be lost when they are overwritten by the new result at the start of the next conversion period. Just prior to this update, DRDY will be forced HIGH and will return LOW after the update.

Two-Wire Interface

For a two-wire interface between the main controller and the ADS1210/11, the Master Mode of operation is recommended. Otherwise, it will be very difficult for the controller to know when the data result is valid. It is possible to use a two-wire interface in the Slave Mode, but the main controller will have to read and write "blindly." Thus, the controller would have to verify that each write to a register was successful by reading the register back, possibly more than once. This would also apply to the Data Output Register. The read rate would have to exceed two times the data rate. See the Multiple Instructions information in this section.

Three-Wire Interface

Figure 28 shows a three-wire interface with a 8xC32 microprocessor. Note that the Slave Mode is being used and that the serial clock of the 8xC32 will be synchronous to the X_{IN} input as both are ultimately derived from the same crystal oscillator. The SDIO pin is being used for input and output.

Figure 29 shows a different type of three-wire interface with a 8xC51 microprocessor. Here, the Master Mode is used. The interface signals consist of SDOUT, SDIO, and SCLK.

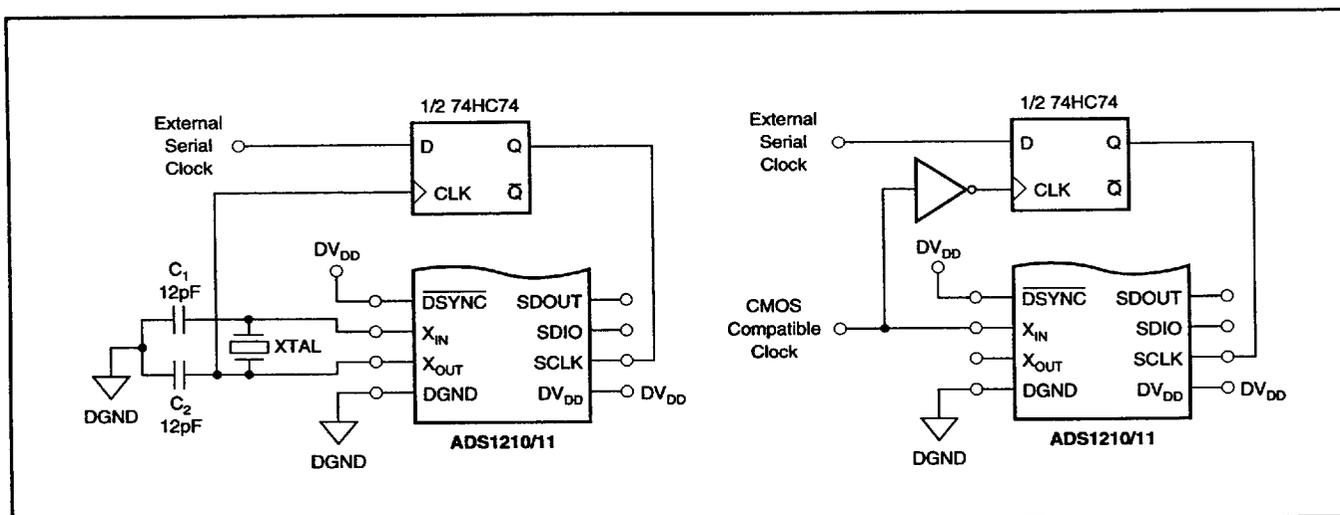


FIGURE 27. Circuits to Synchronize an External Serial Clock to the X_{IN} Input.

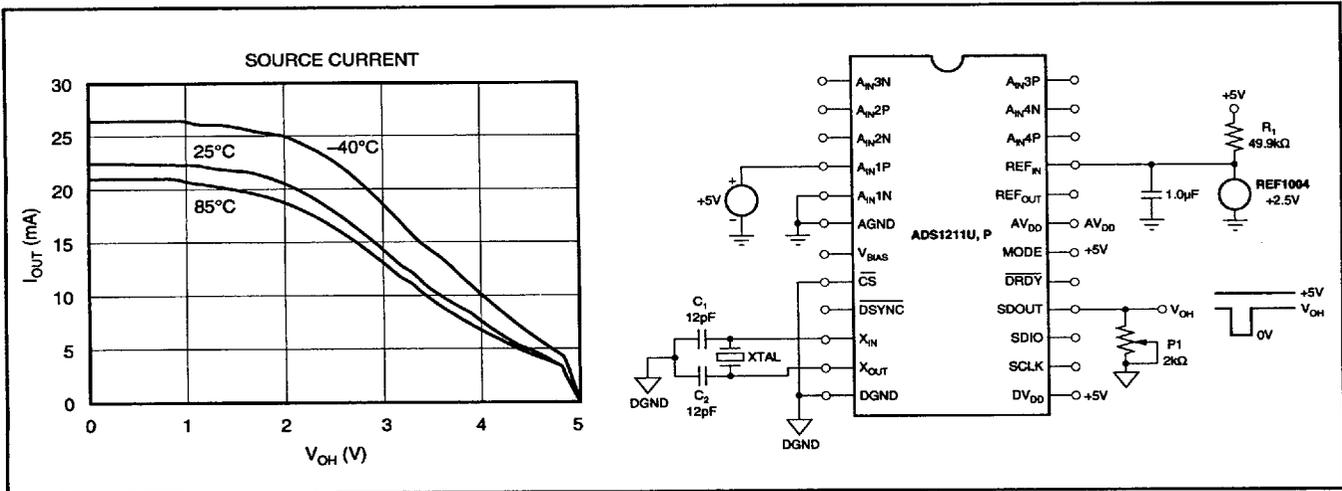


FIGURE 34. Source Current vs V_{OH} for SDOUT Under Worst-Case Conditions.

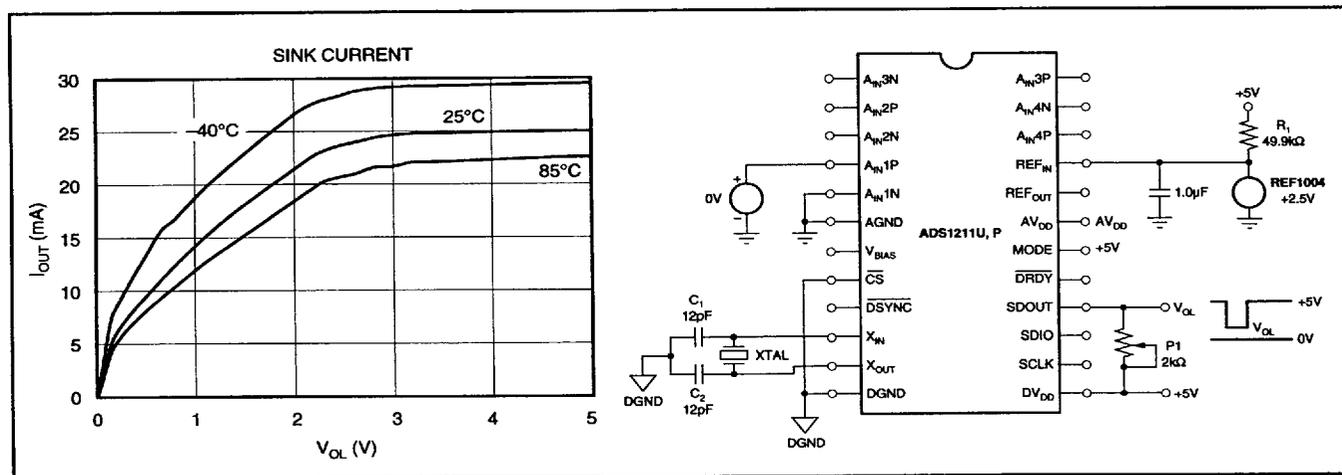


FIGURE 35. Sink Current vs V_{OL} for SDOUT Under Worst-Case Conditions.

voltage is 5V and the output format is Offset Binary (FFFFFF_H). For sink current, the worst-case condition occurs when the analog input differential voltage is 0V and the output format is Two's Complement (000000_H).

Note that SDOUT is tri-stated for the majority of the conversion period and the opto-isolator connection must take this into account.

Synchronization of Multiple Converters

The \overline{DSYNC} input is used to synchronize the output data of multiple ADS1210/11s. Synchronization involves configuring each ADS1210/11 to the same Decimation Ratio and Turbo Mode setting, and providing a common signal to the X_{IN} inputs. Then, the \overline{DSYNC} signal is pulsed LOW (see Figure 22 in the Timing section). This results in an internal reset of the modulator count for the current conversion. Thus, all the converters start counting from zero at the same time, producing a \overline{DRDY} LOW signal at approximately the same point (see Figure 36).

Note that an asynchronous \overline{DSYNC} input may cause multiple converters to be different from one another by one X_{IN} clock cycle. This should not be a concern for most applications. However, the Timing section contains information on exactly synchronizing multiple converters to the same X_{IN} clock cycle.

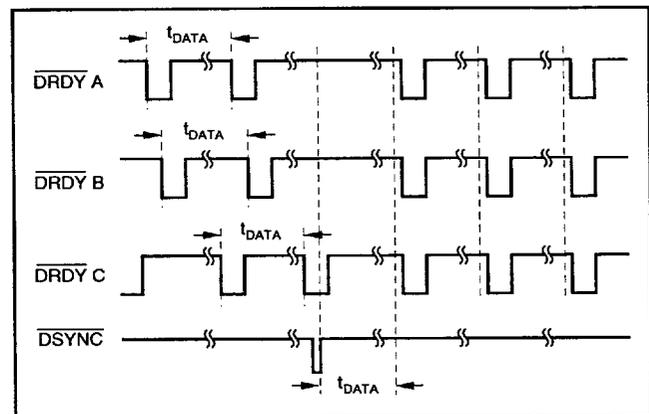


FIGURE 36. Affect of Synchronization on Output Data Timing.

APPLICATIONS

The ADS1210/11 can be used in a broad range of data acquisition tasks. The following application diagrams show the ADS1210 and/or ADS1211 being used for bridge transducer measurements, temperature measurement, and 4-20mA receiver applications.

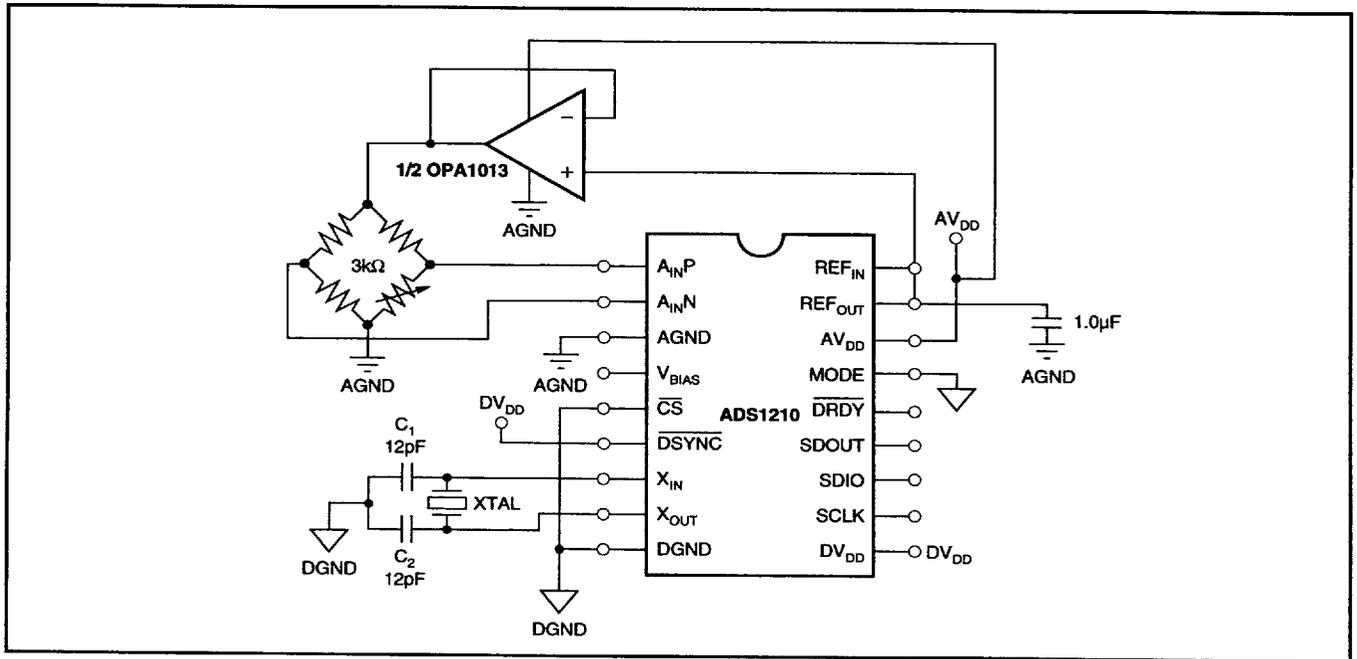


FIGURE 37. Bridge Transducer Interface With Voltage Excitation.

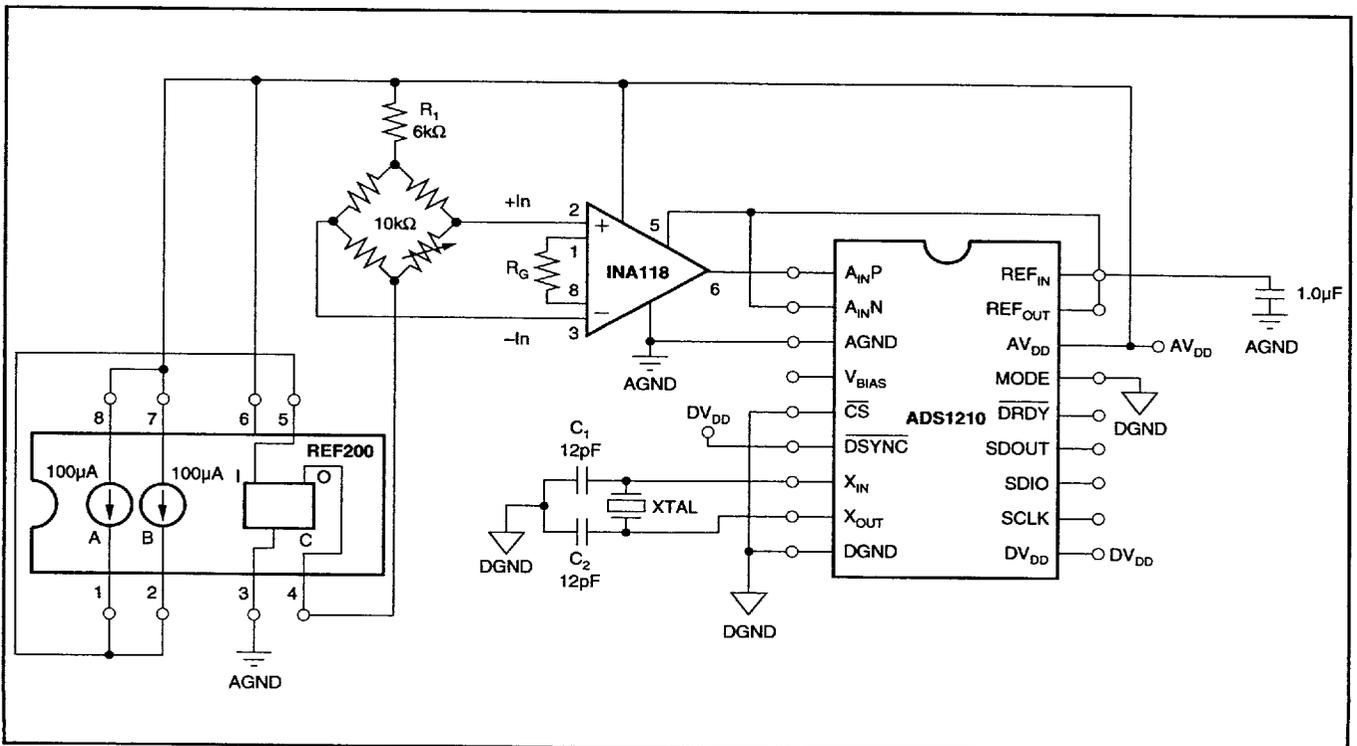


FIGURE 38. Bridge Transducer Interface With Current Excitation.

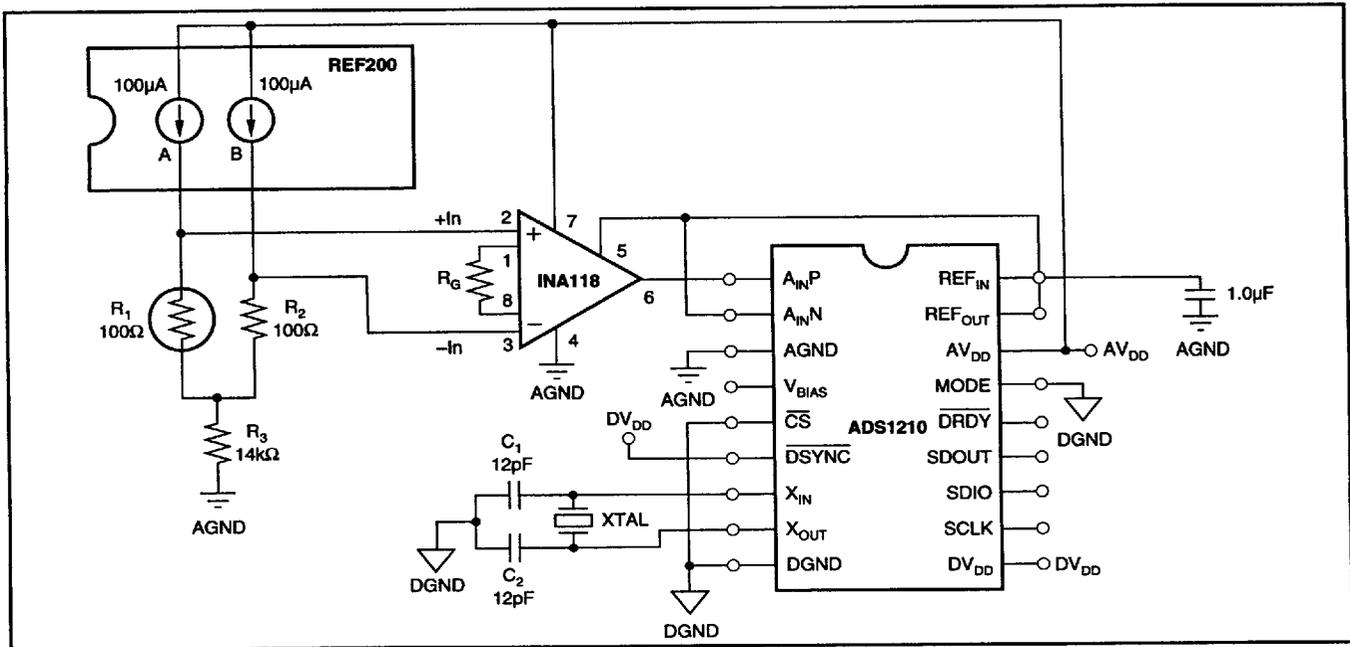


FIGURE 39. PT100 Interface.

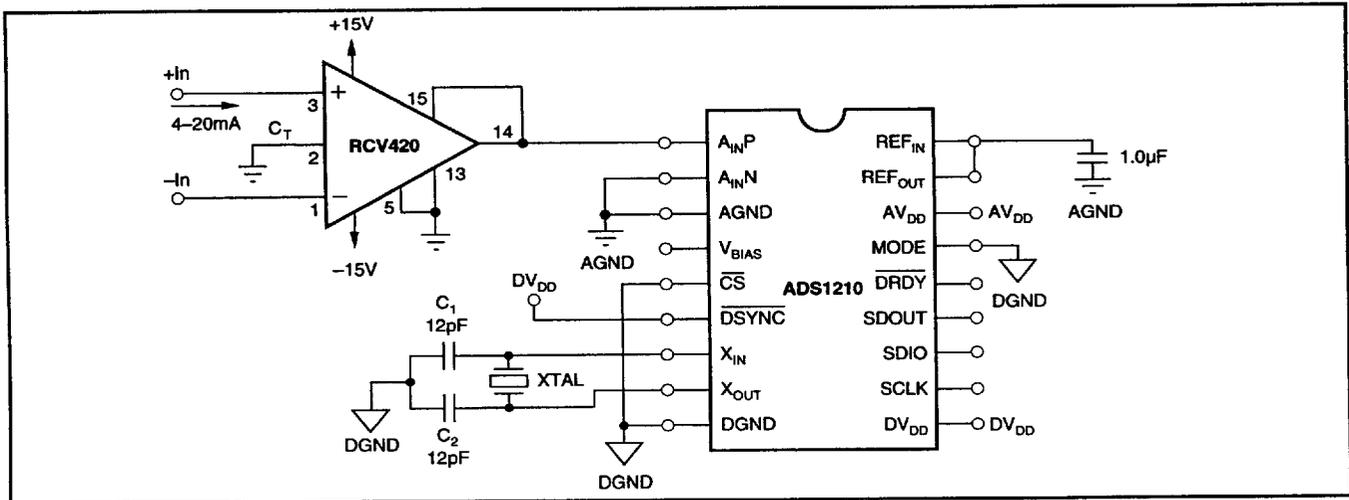


FIGURE 40. Complete 4-20mA Receiver.

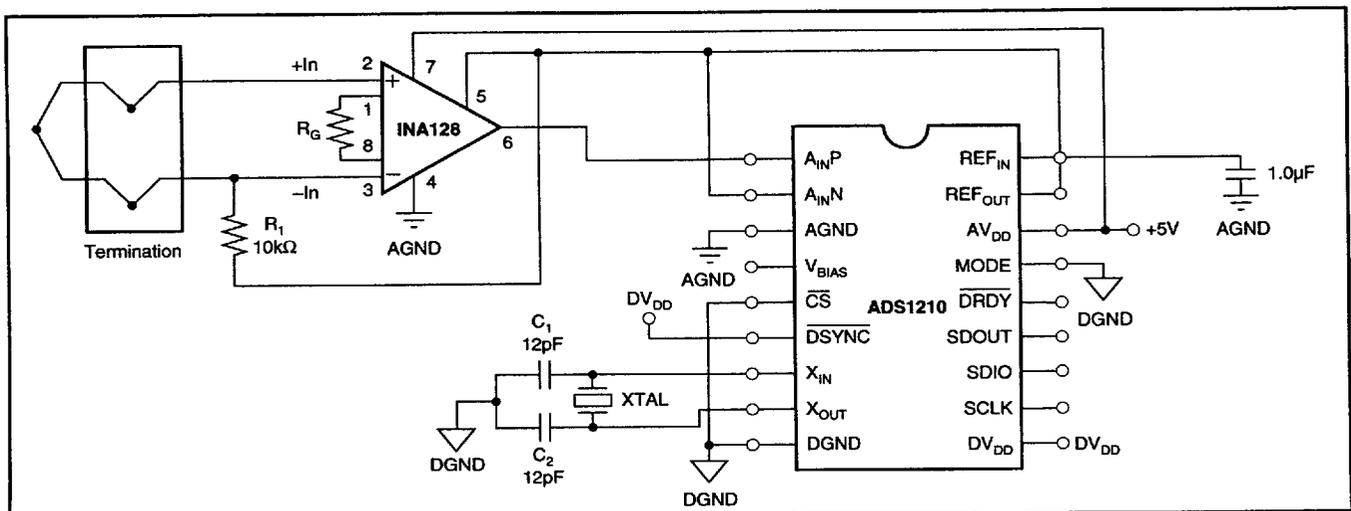


FIGURE 41. Single Supply, High Accuracy Thermocouple.

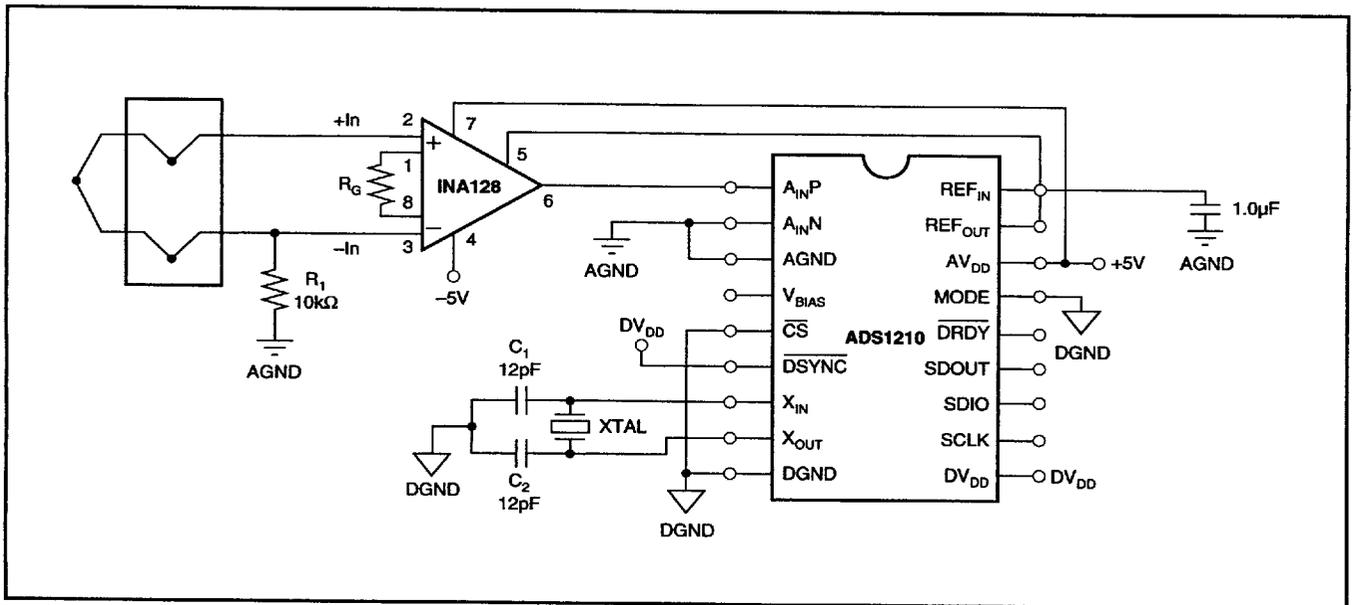


FIGURE 42. Dual Supply, High Accuracy Thermocouple.

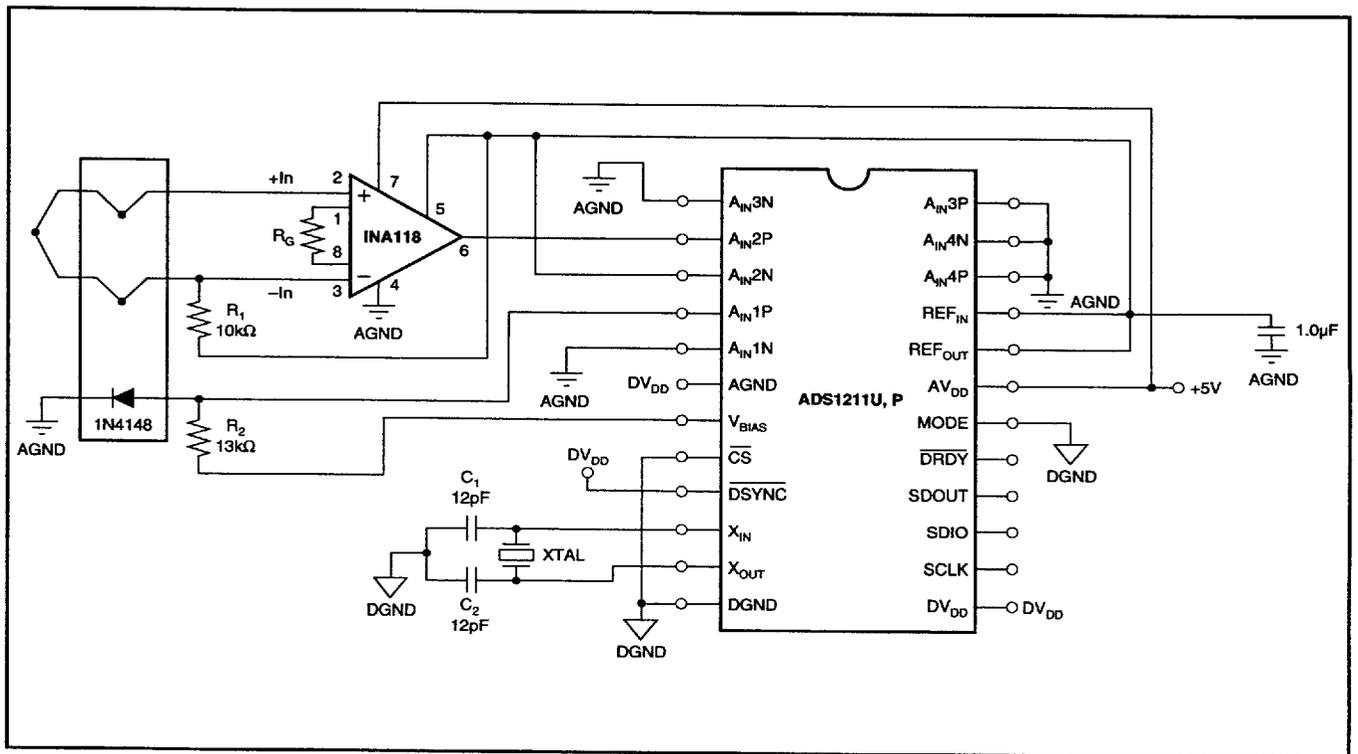


FIGURE 43. Single Supply, High Accuracy Thermocouple Interface With Cold Junction Compensation.

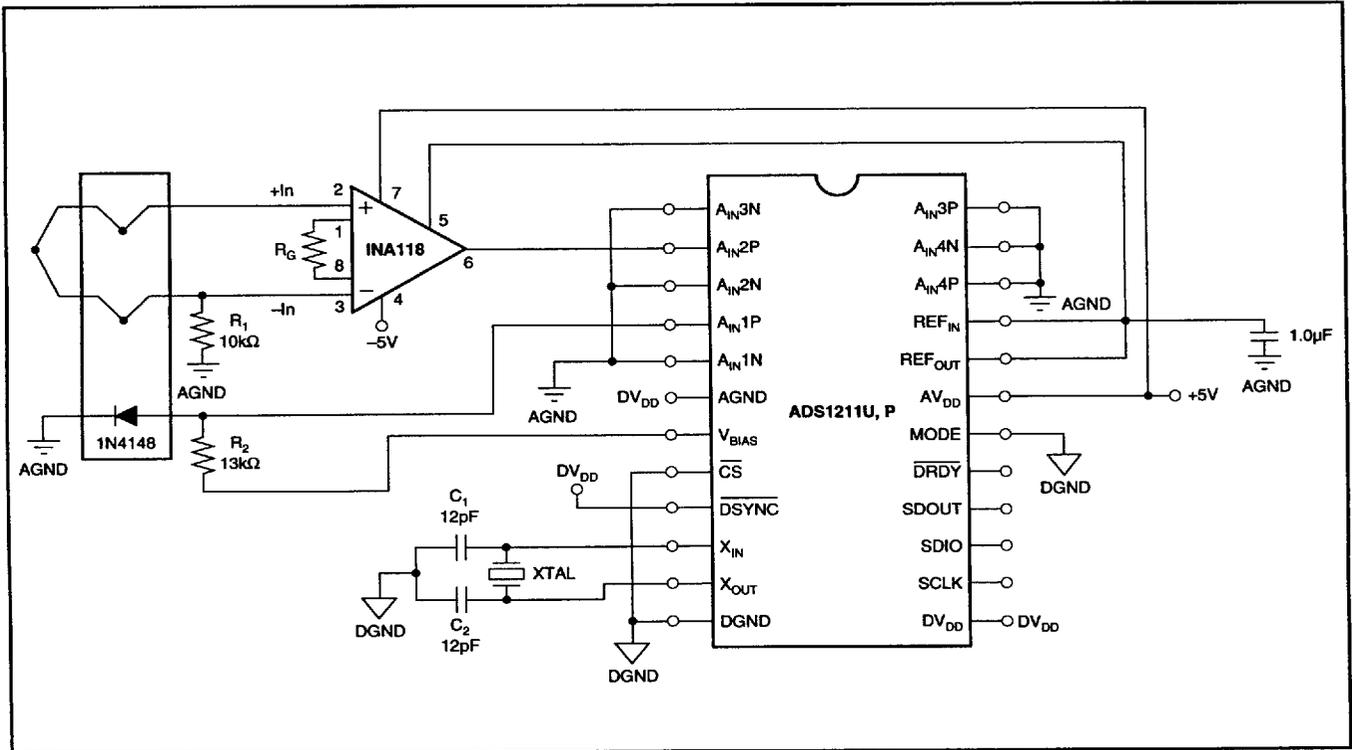


FIGURE 44. Dual Supply, High Accuracy Thermocouple Interface With Cold Junction Compensation.

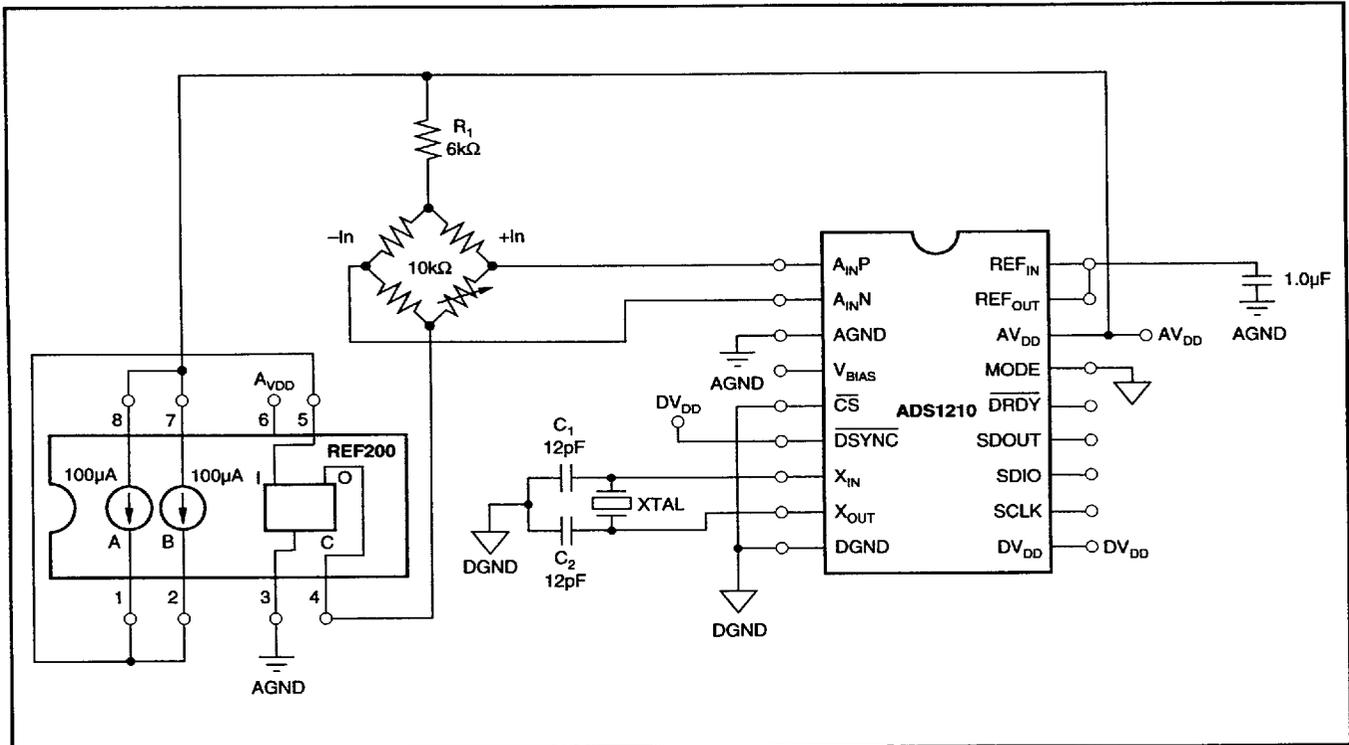
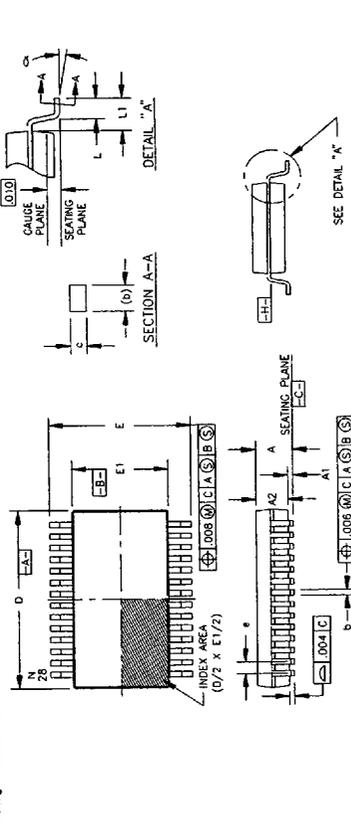


FIGURE 45. Low Cost Bridge Transducer Interface with Current Excitation.

PACKAGE DRAWINGS

Package Number 324 - 28-Lead Plastic 850P



DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.002	0.05	0.05	1.27
A1	0.002	0.05	0.05	1.27
A2	0.002	0.05	0.05	1.27
B	0.009	0.15	0.22	3.81
C	0.004	0.10	0.09	2.54
D	0.390	0.413	9.90	10.50
E	0.231	0.233	5.86	5.91
E1	0.025	0.027	0.635	0.686
E2	0.043	0.045	1.092	1.143
L1	0.043	0.045	1.092	1.143
L2	0.043	0.045	1.092	1.143
N	0.07	0.08	1.78	2.03
B	0.07	0.08	1.78	2.03

NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.3-1982.
 2. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT DATUM PLANE C.
 3. DIMENSIONS DO NOT INCLUDE ALLOWABLE DAMBAR PROTRUSION EXCESS OF 0.005 INCH TOTAL IN MAXIMUM MATERIAL CONDITION.
 4. DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM C.
 5. N IS THE NUMBER OF TERMINAL POSITIONS.
 6. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-SECTION A-A.
 7. SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

DAMBAR INTRUSION SHALL NOT EXCEED .005 INCH TOTAL IN MAXIMUM MATERIAL CONDITION.
 DIMENSION L TO BE DETERMINED AT SEATING PLANE-DATUM C.
 N IS THE NUMBER OF TERMINAL POSITIONS.
 A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-SECTION A-A.
 SECTION A-A DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .004 AND .010 INCH FROM THE LEAD TIP.

PACKAGE NUMBER: 72324
 JEDEC NUMBER: MO-150
 REV.: C



ADS1210/1211

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