



**ANALOG
DEVICES**

Dual Channel, 14-Bit, 65 MSPS A/D Converter with Analog Input Signal Conditioning

AD10465

FEATURES

Dual, 65 MSPS Minimum Sample Rate
Channel-to-Channel Matching, $\pm 0.5\%$ Gain Error
Channel-to-Channel Isolation, >90 dB
DC-Coupled Signal Conditioning Included
Selectable Bipolar Input Voltage Range
 (± 0.5 V, ± 1.0 V, ± 2.0 V)
Gain Flatness up to 25 MHz: < 0.2 dB
80 dB Spurious-Free Dynamic Range
Two's Complement Output Format
3.3 V or 5 V CMOS-Compatible Output Levels
1.75 W per Channel
Industrial and Military Grade

APPLICATIONS

Phased Array Receivers
Communications Receivers
FLIR Processing
Secure Communications
GPS Antijamming Receivers
Multichannel, Multimode Receivers

PRODUCT DESCRIPTION

The AD10465 is a full channel ADC solution with on-module signal conditioning for improved dynamic performance and fully matched channel-to-channel performance. The module includes two wide dynamic range AD6644 ADCs. Each AD6644 has a dc-coupled amplifier front end including an AD8037 low distortion, high bandwidth amplifier, providing a high input impedance and gain, and driving the AD8138 single-to-differential amplifier. The AD6644s have on-chip track-and-hold circuitry and

utilize an innovative multipass architecture to achieve 14-bit, 65 MSPS performance. The AD10465 uses innovative high-density circuit design and laser-trimmed thin-film resistor networks to achieve exceptional matching and performance, while still maintaining excellent isolation and providing for significant board area savings.

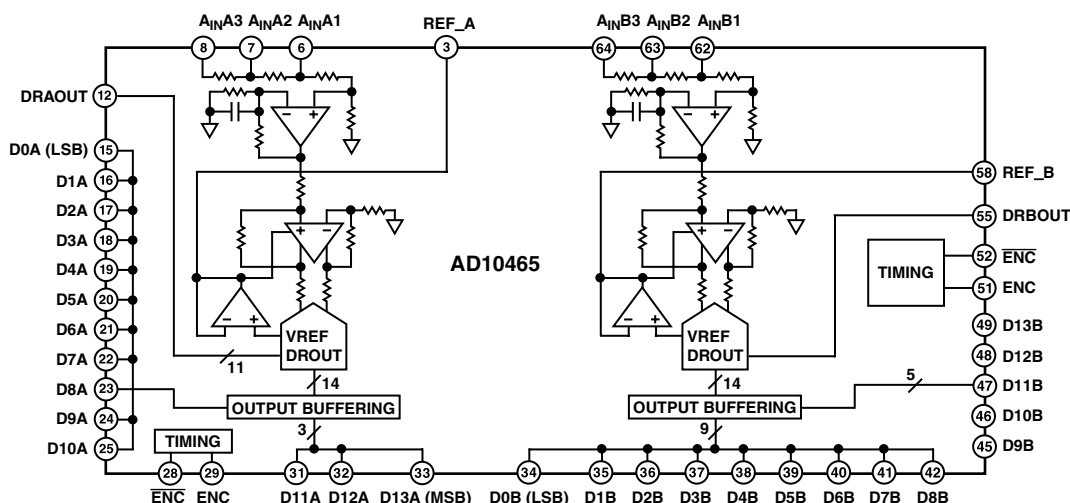
The AD10465 operates with ± 5.0 V for the analog signal conditioning with a separate 5.0 V supply for the analog-to-digital conversion and 3.3 V digital supply for the output stage. Each channel is completely independent, allowing operation with independent encode and analog inputs. The AD10465 also offers the user a choice of analog input signal ranges to further minimize additional external signal conditioning, while still remaining general-purpose.

The AD10465 is packaged in a 68-lead Ceramic Gull Wing package, footprint-compatible with the earlier generation AD10242 (12-bit, 40 MSPS) and AD10265 (12-bit, 65 MSPS). Manufacturing is done on Analog Devices, Inc. Mil-38534 Qualified Manufacturers Line (QML) and components are available up to Class-H (-40°C to $+85^{\circ}\text{C}$). The AD6644 internal components are manufactured on Analog Devices, Inc. high-speed complementary bipolar process (XFCB).

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 65 MSPS.
2. Input amplitude options, user configurable.
3. Input signal conditioning included; both channels matched for gain.
4. Fully tested/characterized performance.
5. Footprint compatible family; 68-lead LCC.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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AD10465—SPECIFICATIONS ($AV_{CC} = +5\text{ V}$; $AV_{EE} = -5\text{ V}$; $DV_{CC} = 3.3\text{ V}$ applies to each ADC unless otherwise noted.)

| Parameter | Temp | Test Level | Mil Subgroup | AD10465AZ/BZ/QML-H | | | Unit |
|--|------|------------|--------------|--------------------|-------|------|--------|
| | | | | Min | Typ | Max | |
| RESOLUTION | | | | 14 | | | Bits |
| DC ACCURACY | | | | Guaranteed | | | |
| No Missing Codes | Full | VI | 1, 2, 3 | | | | |
| Offset Error | 25°C | I | 1 | -2.2 | ±0.02 | +2.2 | % FS |
| | Full | VI | 2, 3 | -2.2 | ±1.0 | +2.2 | % FS |
| Offset Error Channel Match | Full | V | | -1 | ±1.0 | +1 | % |
| Gain Error ¹ | 25°C | I | 1 | -3 | -1.0 | +1 | % FS |
| | Full | VI | 2, 3 | -5 | ±2.0 | +5 | % FS |
| Gain Error Channel Match | 25°C | I | 1 | -1.5 | ±0.5 | +1.5 | % |
| | Max | I | 2 | -3 | ±1.0 | +3 | % |
| | Min | I | 3 | -5 | | +5 | % |
| ANALOG INPUT (A_{IN}) | | | | | | | |
| Input Voltage Range | | | | | | | |
| A_{IN1} | Full | V | | | ±0.5 | | V |
| A_{IN2} | Full | V | | | ±1.0 | | V |
| A_{IN3} | Full | V | | | ±2 | | V |
| Input Resistance | | | | | | | |
| A_{IN1} | Full | IV | 12 | 99 | 100 | 101 | Ω |
| A_{IN2} | Full | IV | 12 | 198 | 200 | 202 | Ω |
| A_{IN3} | Full | IV | 12 | 396 | 400 | 404 | Ω |
| Input Capacitance ² | 25°C | IV | 12 | 0 | 4.0 | 7.0 | pF |
| Analog Input Bandwidth ³ | Full | V | | | 100 | | MHz |
| ENCODE INPUT (ENC, $\overline{\text{ENC}}$) ⁴ | | | | | | | |
| Differential Input Voltage ¹⁷ | Full | IV | | 0.4 | | | V p-p |
| Differential Input Resistance | 25°C | V | | | 10 | | kΩ |
| Differential Input Capacitance | 25°C | V | | | 2.5 | | pF |
| SWITCHING PERFORMANCE | | | | | | | |
| Maximum Conversion Rate ⁵ | Full | VI | 4, 5, 6 | 65 | | | MSPS |
| Minimum Conversion Rate ⁵ | Full | V | 12 | | | 20 | MSPS |
| Aperture Delay (t_A) | 25°C | V | | | 1.5 | | ns |
| Aperture Delay Matching | 25°C | IV | 12 | | 250 | 500 | ps |
| Aperture Uncertainty (Jitter) | 25°C | V | | | 0.3 | | ps rms |
| ENCODE Pulsewidth High | 25°C | IV | 12 | 6.2 | 7.7 | 9.2 | ns |
| ENCODE Pulsewidth Low | 25°C | IV | 12 | 6.2 | 7.7 | 9.2 | ns |
| Output Delay (t_{OD}) | Full | V | | | 6.8 | | ns |
| Encode, Rising to Data Ready, Rising Delay (T_{E_DR}) | Full | | | | 11.5 | | ns |
| SNR ⁶ | | | | | | | |
| Analog Input @ 4.98 MHz | 25°C | V | | | 70 | | dBFS |
| Analog Input @ 9.9 MHz | 25°C | I | 4 | 69 | 70 | | dBFS |
| | Full | II | 5, 6 | 68 | 70 | | dBFS |
| Analog Input @ 19.5 MHz | 25°C | I | 4 | 68 | 70 | | dBFS |
| | Full | II | 5, 6 | 67 | 70 | | dBFS |
| Analog Input @ 32.1 MHz | 25°C | I | 4 | 67 | 69 | | dBFS |
| | Full | II | 5, 6 | 67 | 69 | | dBFS |
| SINAD ⁷ | | | | | | | |
| Analog Input @ 4.98 MHz | 25°C | V | | | 70 | | dB |
| Analog Input @ 9.9 MHz | 25°C | I | 4 | 67.5 | 69 | | dB |
| | Full | II | 5, 6 | 67.5 | 69 | | dB |
| Analog Input @ 19.5 MHz | 25°C | I | 4 | 65 | 68 | | dB |
| | Full | II | 5, 6 | 65 | 68 | | dB |
| Analog Input @ 32.1 MHz | 25°C | I | 4 | 60 | 63 | | dB |
| | Full | II | 5, 6 | 58 | 61 | | dB |

| Parameter | Temp | Test Level | Mil Subgroup | AD10465AZ/BZ/QML-H | | | Unit |
|---|------|------------|--------------|--------------------|------------------|-------|---------------|
| | | | | Min | Typ | Max | |
| SPURIOUS-FREE DYNAMIC RANGE ⁸ | | | | | | | |
| Analog Input @ 4.98 MHz | 25°C | V | | | 85 | | dBFS |
| Analog Input @ 9.9 MHz | 25°C | I | 4 | 73 | 82 | | dBFS |
| | Full | II | 5, 6 | 70 | 82 | | dBFS |
| Analog Input @ 19.5 MHz | 25°C | I | 4 | 72 | 78 | | dBFS |
| | Full | II | 5, 6 | 70 | 78 | | dBFS |
| Analog Input @ 32.1 MHz | 25°C | I | 4 | 62 | 68 | | dBFS |
| | Full | II | 5, 6 | 60 | 66 | | dBFS |
| TWO-TONE IMD REJECTION ⁹ | | | | | | | |
| $f_{IN} = 10$ MHz and 11 MHz | 25°C | I | 4 | 78 | 87 | | dBFS |
| f_1 and f_2 are -7 dB | | II | 5, 6 | 78 | | | |
| $f_{IN} = 31$ MHz and 32 MHz | 25°C | I | 4 | 68 | 70 | | dBFS |
| f_1 and f_2 Are -7 dB | Full | II | 5, 6 | 60 | | | |
| CHANNEL-TO-CHANNEL ISOLATION ¹⁰ | 25°C | IV | 12 | | 90 | | dB |
| TRANSIENT RESPONSE | 25°C | V | | | 15.3 | | ns |
| OVERVOLTAGE RECOVERY TIME ¹¹ | | | | | | | |
| $V_{IN} = 2.0 \times f_s$ | Full | IV | 12 | | 40 | 100 | ns |
| $V_{IN} = 4.0 \times f_s$ | Full | IV | 12 | | 150 | 200 | ns |
| DIGITAL OUTPUTS ¹² | | | | | | | |
| Logic Compatibility | | | | | CMOS | | |
| $DV_{CC} = 3.3$ V | | | | | | | |
| Logic "1" Voltage | Full | I | 1, 2, 3 | 2.5 | $DV_{CC} - 0.2$ | | V |
| Logic "0" Voltage | Full | I | 1, 2, 3 | | 0.2 | 0.5 | V |
| $DV_{CC} = 5$ V | | | | | | | |
| Logic "1" Voltage | Full | V | | | $DV_{CC} - 0.3$ | | V |
| Logic "0" Voltage | Full | V | | | 0.35 | | V |
| Output Coding | | | | | Two's Complement | | |
| POWER SUPPLY | | | | | | | |
| AV_{CC} Supply Voltage ¹³ | Full | VI | | 4.85 | 5.0 | 5.25 | V |
| I (AV_{CC}) Current | Full | I | | | 270 | 308 | mA |
| AV_{EE} Supply Voltage ¹³ | Full | VI | | -5.25 | -5.0 | -4.75 | V |
| I (AV_{EE}) Current | Full | V | | | 38 | 49 | mA |
| DV_{CC} Supply Voltage ¹³ | Full | VI | | 3.135 | 3.3 | 3.465 | V |
| I (DV_{CC}) Current | Full | V | | | 30 | 46 | mA |
| I_{CC} (Total) Supply Current per Channel | Full | I | 1, 2, 3 | | 338 | 403 | mA |
| Power Dissipation (Total) | Full | I | 1, 2, 3 | | 3.5 | 3.9 | W |
| Power Supply Rejection Ratio (PSRR) | Full | V | | | 0.02 | | % FSR/% V_S |
| Passband Ripple to 10 MHz | | V | | | 0.1 | | dB |
| Passband Ripple to 25 MHz | | V | | | 0.2 | | dB |

NOTES

¹ Gain tests are performed on A_{IN1} input voltage range.

² Input Capacitance spec. combines AD8037 die capacitance and ceramic package capacitance.

³ Full power bandwidth is the frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

⁴ All ac specifications tested by driving \overline{ENCODE} and $ENCODE$ differentially.

⁵ Minimum and maximum conversion rates allow for variation in Encode Duty Cycle of 50% \pm 5%.

⁶ Analog input signal power at -1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed). Encode = 65 MSPS. SNR is reported in dBFS, related back to converter full power.

⁷ Analog input signal power at -1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 65 MSPS.

⁸ Analog input signal power swept from -1 dBFS to -60 dBFS; SFDR is ratio of converter full scale to worst spur.

⁹ Both input tones at -7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermod product.

¹⁰ Channel-to-channel isolation tested with A channel grounded and a full-scale signal applied to B channel.

¹¹ Input driven to 2 \times and 4 \times A_{IN1} range for > four clock cycles. Output recovers inband in specified time with Encode = 65 MSPS.

¹² Digital output logic levels: $DV_{CC} = 3.3$ V, $C_{LOAD} = 10$ pF. Capacitive loads > 10 pF will degrade performance.

¹³ Supply voltage recommended operating range. AV_{CC} may be varied from 4.85 V to 5.25 V. However, rated ac (harmonics) performance is valid only over the range $AV_{CC} = 5.0$ V to 5.25 V.

All specifications guaranteed within 100 ms of initial power-up regardless of sequencing.

Specifications subject to change without notice.

AD10465

ABSOLUTE MAXIMUM RATINGS¹

| Parameter | Min | Max | Units |
|--------------------------------------|-----------------|-----------------|-------|
| ELECTRICAL | | | |
| V _{CC} Voltage | 0 | 7 | V |
| V _{EE} Voltage | −7 | 0 | V |
| Analog Input Voltage | V _{EE} | V _{CC} | V |
| Analog Input Current | −10 | +10 | mA |
| Digital Input Voltage (ENCODE) | 0 | V _{CC} | V |
| ENCODE, ENCODE Differential Voltage | | 4 | V |
| Digital Output Current | −10 | +10 | mA |
| ENVIRONMENTAL² | | | |
| Operating Temperature (Case) | −40 | +85 | °C |
| Maximum Junction Temperature | | 174 | °C |
| Lead Temperature (Soldering, 10 sec) | | 300 | °C |
| Storage Temperature Range (Ambient) | −65 | +150 | °C |

NOTES

¹Absolute maximum ratings are limiting values applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

²Typical thermal impedance for “ES” package: $\theta_{JC} = 2.2^{\circ}\text{C}/\text{W}$; $\theta_{JA} = 24.3^{\circ}\text{C}/\text{W}$.

TEST LEVEL

- I. 100% Production Tested.
- II. 100% Production Tested at 25°C, and sample tested at specified temperatures. AC testing done on sample basis.
- III. Sample Tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at temperature at 25°C, sample tested at temperature extremes.

ORDERING GUIDE

| Model | Temperature Range | Package Description |
|-----------------|-----------------------|-------------------------------------|
| AD10465AZ | −25°C to +85°C (Case) | 68-Lead Ceramic Leaded Chip Carrier |
| AD10465BZ | −40°C to +85°C (Case) | 68-Lead Ceramic Leaded Chip Carrier |
| 5962-9961601HXA | −40°C to +85°C (Case) | 68-Lead Ceramic Leaded Chip Carrier |
| AD10465/PCB | 25°C | Evaluation Board with AD10465AZ |

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD10465 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

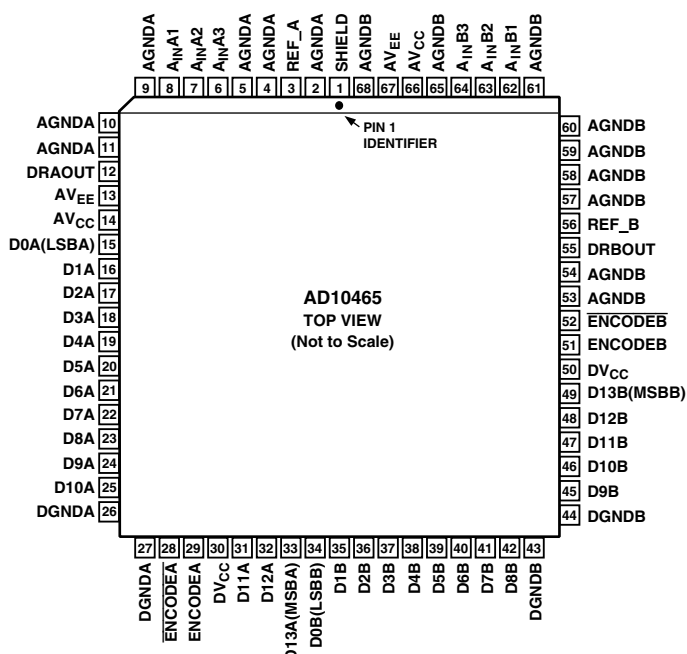


PIN FUNCTION DESCRIPTIONS

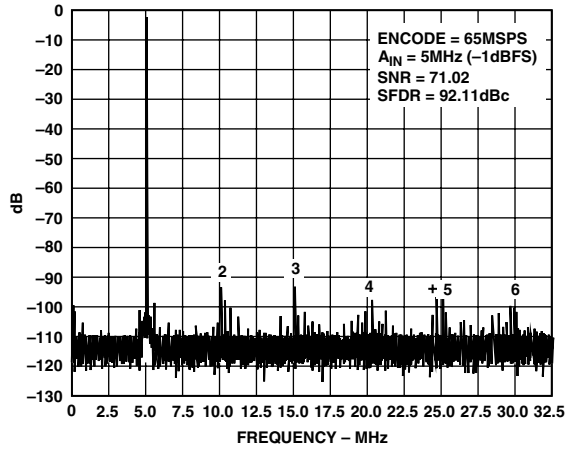
| Pin No. | Name | Function |
|----------------------|-----------------------------|--|
| 1 | SHIELD | Internal Ground Shield between channels. |
| 2, 4, 5, 9–11 | AGNDA | A Channel Analog Ground. A and B grounds should be connected as close to the device as possible. |
| 3 | REF_A | A Channel Internal Voltage Reference. |
| 6 | A _{IN} A1 | Analog Input for A side ADC (nominally ± 0.5 V). |
| 7 | A _{IN} A2 | Analog Input for A side ADC (nominally ± 1.0 V). |
| 8 | A _{IN} A3 | Analog Input for A side ADC (nominally ± 2.0 V). |
| 12 | DRAOUT | Data Ready A Output. |
| 13 | AV _{EE} | Analog Negative Supply Voltage (nominally -5.0 V or -5.2 V). |
| 14 | AV _{CC} | Analog Positive Supply Voltage (nominally 5.0 V). |
| 26, 27 | DGNDA | A Channel Digital Ground. |
| 15–25, 31–33 | D0A–D13A | Digital Outputs for ADC A. D0 (LSB). |
| 28 | $\overline{\text{ENCODEA}}$ | $\overline{\text{ENCODEA}}$ is complement of ENCODE. |
| 29 | ENCODEA | Data conversion initiated on rising edge of ENCODE input. |
| 30 | DV _{CC} | Digital Positive Supply Voltage (nominally 5.0 V/ 3.3 V). |
| 43, 44 | DGNDB | B Channel Digital Ground. |
| 34–42, 45–49 | D0B–D13B | Digital Outputs for ADC B. D0 (LSB). |
| 53–54, 57–61, 65, 68 | AGNDB | B Channel Analog Ground. A and B grounds should be connected as close to the device as possible. |
| 50 | DV _{CC} | Digital Positive Supply Voltage (nominally 5.0 V/ 3.3 V). |
| 51 | ENCODEB | Data conversion initiated on rising edge of ENCODE input. |
| 52 | $\overline{\text{ENCODEB}}$ | $\overline{\text{ENCODEB}}$ is complement of ENCODE. |
| 55 | DRBOUT | Data Ready B Output. |
| 56 | REF_B | B Channel Internal Voltage Reference. |
| 62 | A _{IN} B1 | Analog Input for B side ADC (nominally ± 0.5 V). |
| 63 | A _{IN} B2 | Analog Input for B side ADC (nominally ± 1.0 V). |
| 64 | A _{IN} B3 | Analog Input for B side ADC (nominally ± 2.0 V). |
| 66 | AV _{CC} | Analog Positive Supply Voltage (nominally -5.0 V). |
| 67 | AV _{EE} | Analog Negative Supply Voltage (nominally -5.0 V or -5.2 V). |

PIN CONFIGURATION

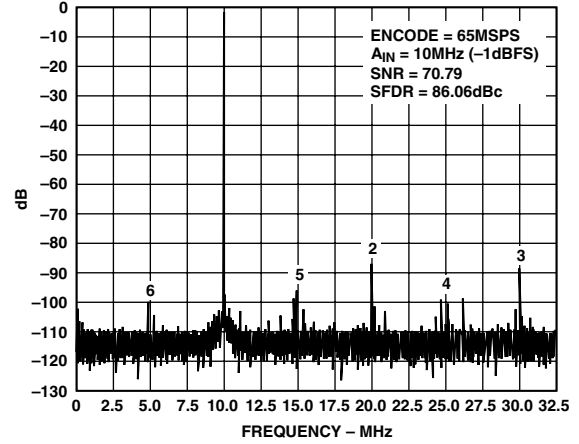
68-Lead Ceramic Leaded Chip Carrier



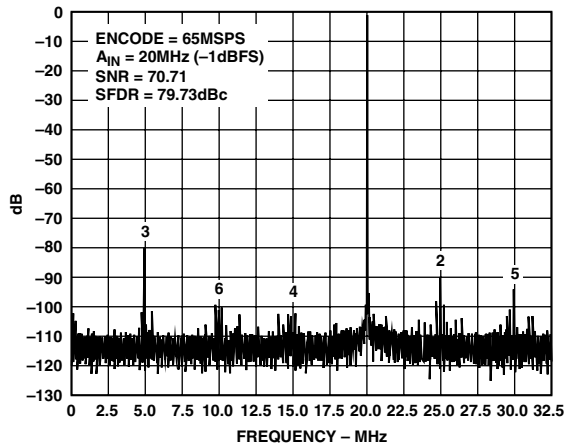
AD10465—Typical Performance Characteristics



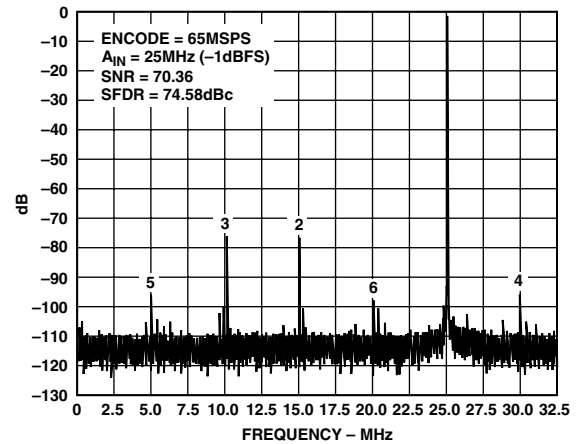
TPC 1. Single Tone @ 5 MHz



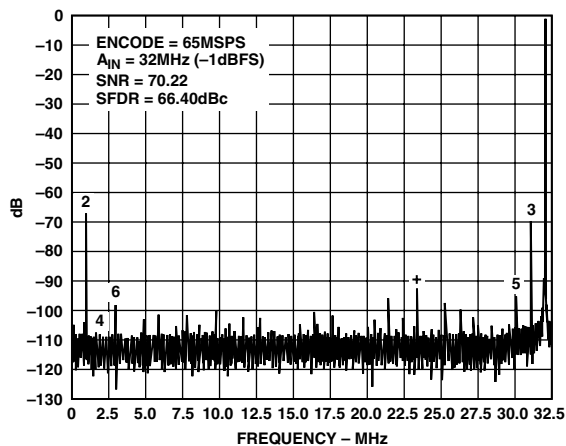
TPC 4. Single Tone @ 10 MHz



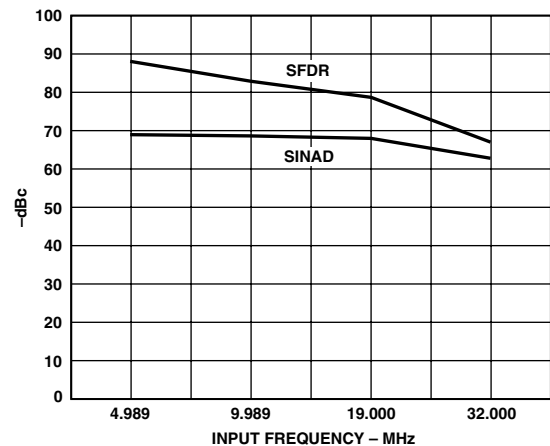
TPC 2. Single Tone @ 20 MHz



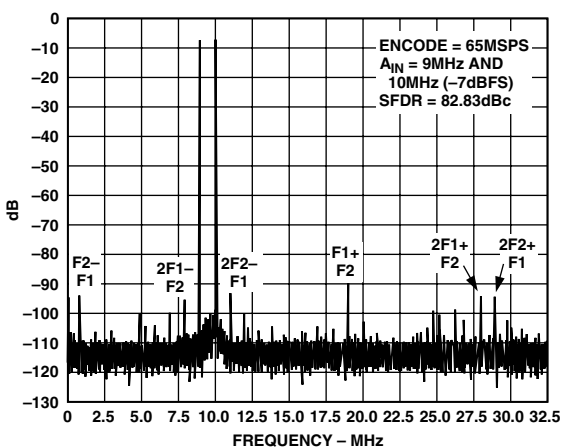
TPC 5. Single Tone @ 25 MHz



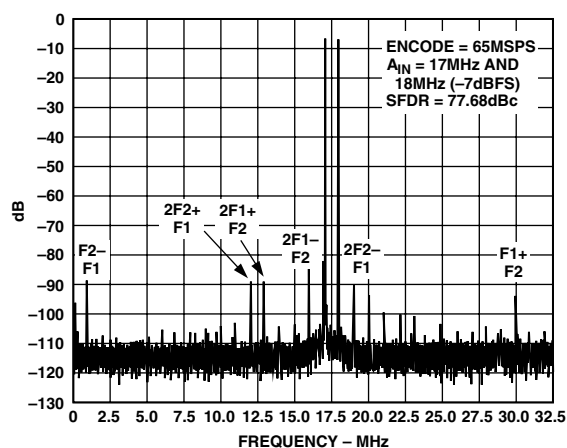
TPC 3. Single Tone @ 32 MHz



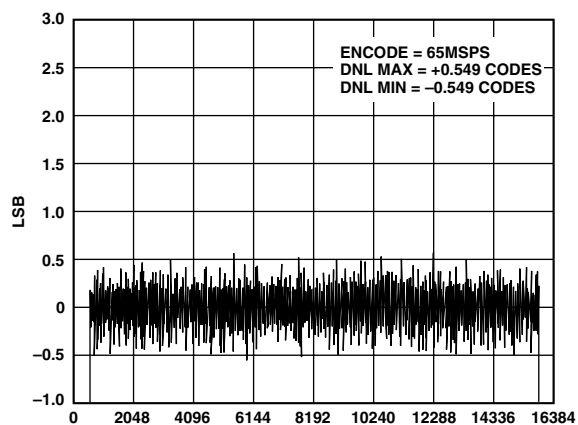
TPC 6. SFDR and SINAD vs. Frequency



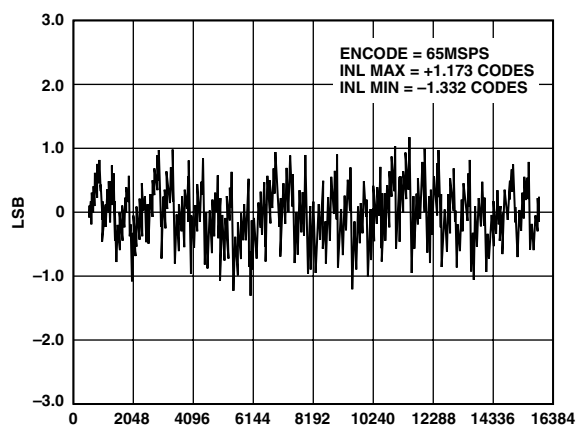
TPC 7. Two Tone @ 9/10 MHz



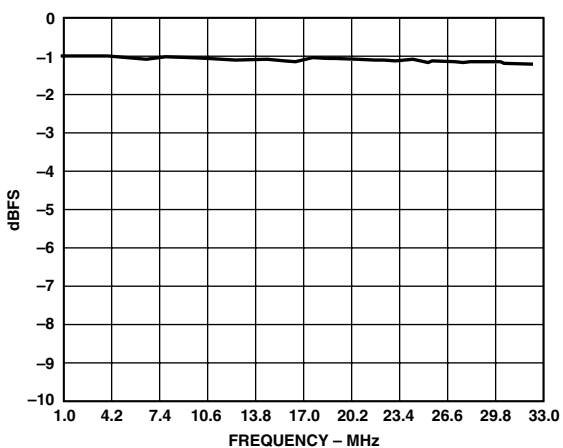
TPC 10. Two Tone @ 17/18 MHz



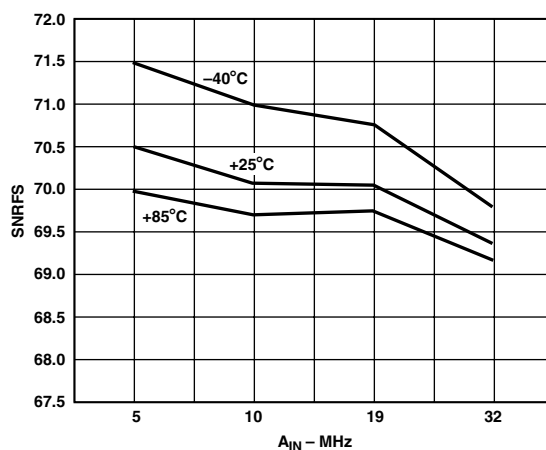
TPC 8. Differential Nonlinearity



TPC 11. Integral Nonlinearity



TPC 9. Gain Flatness

TPC 12. SNR vs. A_{IN} Frequency

AD10465

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Differential Nonlinearity

The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle

Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic “1” state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

Harmonic Distortion

The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a “best straight line” determined by a least square curve fit.

Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The encode rate at which parametric testing is performed, above which converter performance may degrade.

Output Propagation Delay

The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time

The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal of the specified percentage of full scale is reduced to midscale.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc. May be reported in dB (i.e., relative to signal level) or in dBFS (always related back to converter full scale).

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc. May be reported in dB (i.e., relative to signal level) or in dBFS (always related back to converter full scale).

Spurious-Free Dynamic Range

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Transient Response

The time required for the converter to achieve 0.03% accuracy when a one-half full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBFS.

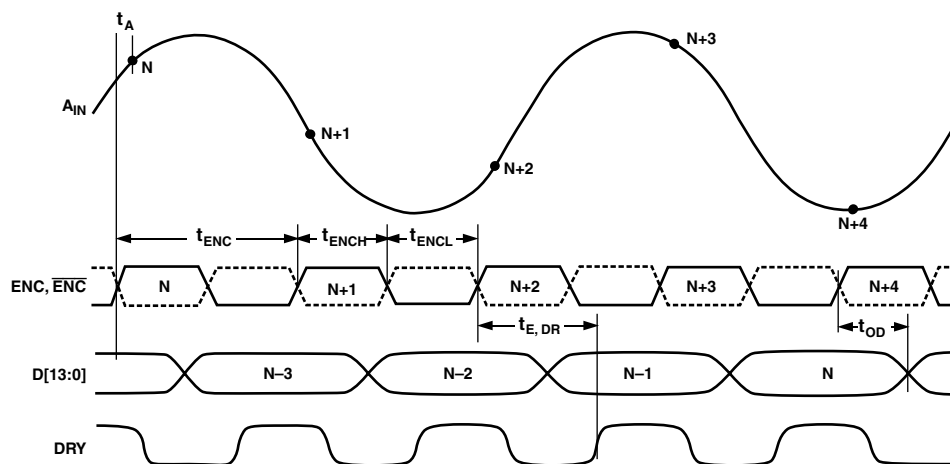


Figure 1. Timing Diagram

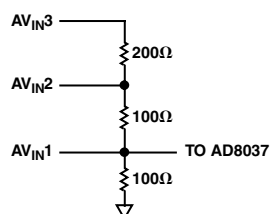


Figure 2. Analog Input Stage

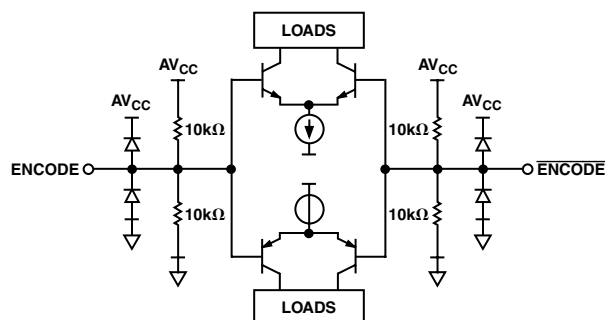


Figure 3. ENCODE Inputs

THEORY OF OPERATION

The AD10465 is a high dynamic range 14-bit, 65 MHz pipeline delay (three pipelines) analog-to-digital converter. The custom analog input section maintains the same input ranges (1 V p-p, 2 V p-p, and 4 V p-p) and input impedance (100 Ω, 200 Ω, and 400 Ω) as the AD10242.

The AD10465 employs four monolithic ADI components per channel (AD8037, AD8138, AD8031, and AD6644), along with multiple passive resistor networks and decoupling capacitors to fully integrate a complete 14-bit analog-to-digital converter.

The input signal is passed through a precision laser-trimmed resistor divider allowing the user to externally select operation with a full-scale signal of ± 0.5 V, ± 1.0 V or ± 2.0 V by choosing the proper input terminal for the application.

The AD10465 analog input includes an AD8037 amplifier featuring an innovative architecture that maximizes the dynamic range capability on the amplifiers inputs and outputs. The AD8037 amplifier provides a high input impedance and gain for driving the AD8138 in a single-ended to differential amplifier configuration. The AD8138 has a -3 dB bandwidth at 300 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier. The AD8138 differential outputs help balance the differential inputs to the AD6644, maximizing the performance of the ADC.

The AD8031 provides the buffer for the internal reference of the AD6644. The internal reference voltage of the AD6644 is designed to track the offsets and drifts of the ADC and is used to ensure matching over an extended temperature range of operation. The reference voltage is connected to the output common mode input on the AD8138. The AD6644 reference voltage sets the output common-mode on the AD8138 at 2.4 V, which is the midsupply level for the AD6644.

The AD6644 has complementary analog input pins, A_{IN} and $\overline{A_{IN}}$. Each analog input is centered at 2.4 V and should swing ± 0.55 V around this reference. Since A_{IN} and $\overline{A_{IN}}$ are 180 degrees out of phase, the differential analog input signal is 2.2 V peak-to-peak. Both analog inputs are buffered prior to the first track-and-hold,

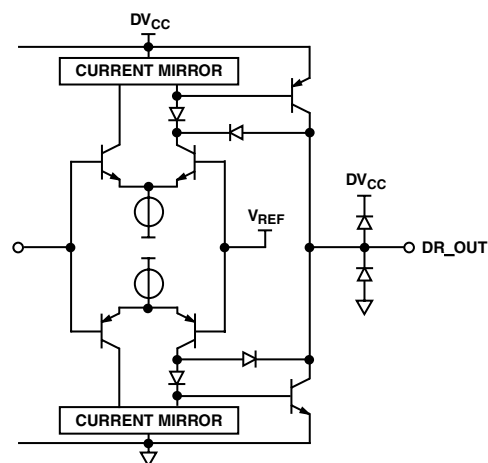


Figure 4. Digital Output Stage

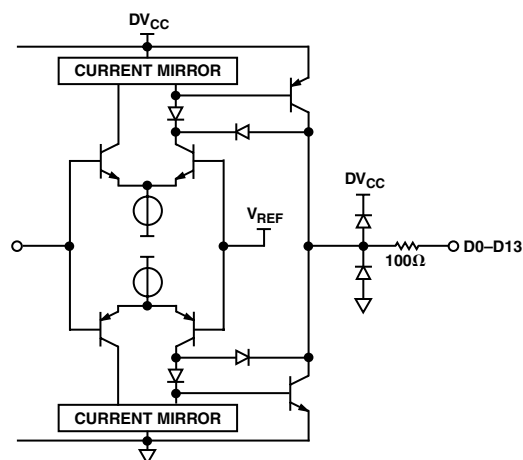


Figure 5. Digital Output Stage

TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of a 5-bit coarse ADC1. The digital output of ADC1 drives 14 bits of precision which is achieved through laser trimming. The output of DAC1 is subtracted from the delayed analog signal at the input of TH3 to generate a first residue signal. TH2 provides an analog pipeline delay to compensate for the digital delay of ADC1.

The first residue signal is applied to a second conversion stage consisting of a 5-bit ADC2, 5-bit DAC2, and pipeline TH4. The second DAC requires 10 bits of precision which is met by the process with no trim. The input to TH5 is a second residue signal generated by subtracting the quantized output of DAC2 from the first residue signal held by TH4. TH5 drives a final 6-bit ADC3.

The digital outputs from ADC1, ADC2, and ADC3 are added together and corrected in the digital error correction logic to generate the final output data. The result is a 14-bit parallel digital CMOS-compatible word, coded as two's complement.

USING THE FLEXIBLE INPUT

The AD10465 has been designed with the user's ease of operation in mind. Multiple input configurations have been included on board to allow the user a choice of input signal levels and input impedance. While the standard inputs are ± 0.5 V, ± 1.0 V and ± 2.0 V, the user can select the input impedance of the

AD10465

AD10465 on any input by using the other inputs as alternate locations for GND or an external resistor. The following chart summarizes the impedance options available at each input location:

- $A_{IN1} = 100\ \Omega$ when A_{IN2} and A_{IN3} are open.
- $A_{IN1} = 75\ \Omega$ when A_{IN3} is shorted to GND.
- $A_{IN1} = 50\ \Omega$ when A_{IN2} is shorted to GND.
- $A_{IN2} = 200\ \Omega$ when A_{IN3} is open.
- $A_{IN2} = 100\ \Omega$ when A_{IN3} is shorted to GND.
- $A_{IN2} = 75\ \Omega$ when A_{IN2} to A_{IN3} has an external resistor of $300\ \Omega$, with A_{IN3} shorted to GND.
- $A_{IN2} = 50\ \Omega$ when A_{IN2} to A_{IN3} has an external resistor of $100\ \Omega$, with A_{IN3} shorted to GND.
- $A_{IN3} = 400\ \Omega$.
- $A_{IN3} = 100\ \Omega$ when A_{IN3} has an external resistor of $133\ \Omega$ to GND.
- $A_{IN3} = 75\ \Omega$ when A_{IN3} has an external resistor of $92\ \Omega$ to GND.
- $A_{IN3} = 50\ \Omega$ when A_{IN3} has an external resistor of $57\ \Omega$ to GND.

APPLYING THE AD10465

Encoding the AD10465

The AD10465 encode signal must be a high quality, extremely low phase noise source, to prevent degradation of performance. Maintaining 14-bit accuracy places a premium on encode clock phase noise. SNR performance can easily degrade by 3 dB to 4 dB with 32 MHz input signals when using a high-jitter clock source. See Analog Devices' Application Note AN-501, "Aperture Uncertainty and ADC System Performance" for complete details. For optimum performance, the AD10465 must be clocked differentially. The encode signal is usually ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Shown below is one preferred method for clocking the AD10465. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD10465 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD10465, and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically $100\ \Omega$) is placed in the series with the primary.

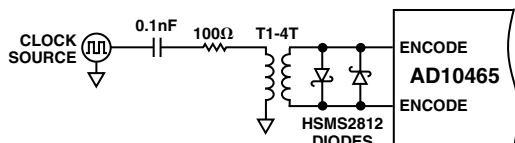


Figure 6. Crystal Clock Oscillator, Differential Encode

If a low jitter ECL/PECL clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown below. A device that offers excellent jitter performance is the MC100LVEL16 (or same family) from Motorola.

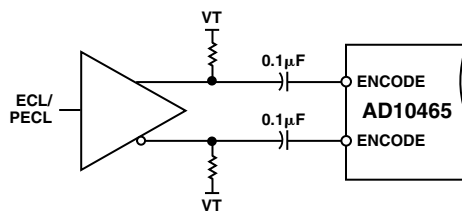


Figure 7. Differential ECL for Encode

Jitter Considerations

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, Equation 1 accurately predicts the SNR based on three terms. These are jitter, average DNL error, and thermal noise. Each of these terms contributes to the noise within the converter.

$$\text{SNR} = -20 \times \log \left[\left(\frac{1 + \epsilon}{2^N} \right)^2 + \left(2 \times \pi \times f_{\text{ANALOG}} \times t_{J \text{ RMS}} \right)^2 + \left(\frac{V_{\text{NOISE RMS}}}{2^N} \right)^2 \right]^{1/2} \quad (1)$$

f_{ANALOG} = analog input frequency.

$t_{J \text{ RMS}}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry).

ϵ = average DNL of the ADC (typically 0.50 LSB).

N = Number of bits in the ADC.

$V_{\text{NOISE RMS}}$ = V rms noise referred to the analog input of the ADC (typically 5 LSB).

For a 14-bit analog-to-digital converter like the AD10465, aperture jitter can greatly affect the SNR performance as the analog frequency is increased. The chart below shows a family of curves that demonstrates the expected SNR performance of the AD10465 as jitter increases. The chart is derived from the above equation.

For a complete discussion of aperture jitter, please consult Analog Devices' Application Note AN-501, "Aperture Uncertainty and ADC System Performance."

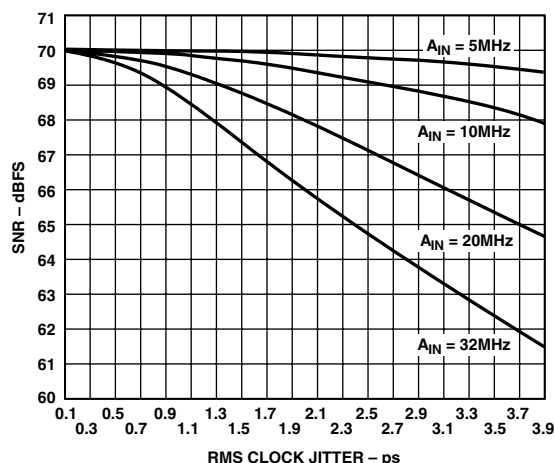


Figure 8. SNR vs. Jitter

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that may be “received” by the AD10465. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 μF chip capacitors.

The AD10465 has separate digital and analog power supply pins. The analog supplies are denoted AV_{CC} and the digital supply pins are denoted DV_{CC} . AV_{CC} and DV_{CC} should be separate power supplies. This is because the fast digital output swings can couple switching current back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 V. The AD10465 is specified for $\text{DV}_{\text{CC}} = 3.3 \text{ V}$ as this is a common supply for digital ASICs.

Output Loading

Care must be taken when designing the data receivers for the AD10465. The digital outputs drive an internal series resistor (e.g., 100 Ω) followed by a gate like 75LCX574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematic shown in Figure 10. The digital outputs of the AD10465 have a constant output slew rate of 1 V/ns. A typical CMOS gate combined with a PCB trace will have a load of approximately 10 pF. Therefore, as each bit switches, 10 mA ($10 \text{ pF} \times 1 \text{ V} / 1 \text{ ns}$) of dynamic current per bit will flow in or out of the device. A full-scale transition can cause up to 140 mA (14 bits \times 10 mA/bit) of current flow through the output stages. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD10465. It should also be noted that extra capacitive loading will increase output timing and invalidate timing specifications. Digital output timing is guaranteed with 10 pF loads.

LAYOUT INFORMATION

The schematic of the evaluation board (Figure 10) represents a typical implementation of the AD10465. The pinout of the AD10465 is very straightforward and facilitates ease of use and the implementation of high frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors can be standard high quality ceramic chip capacitors.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate. Internal circuitry buffers the outputs of the ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.

EVALUATION BOARD

The AD10465 evaluation board (Figure 9) is designed to provide optimal performance for evaluation of the AD10465 analog-to-digital converter. The board encompasses everything needed to insure the highest level of performance for evaluating the AD10465. The board requires an analog input signal, encode clock and power supply inputs. The clock is buffered on-board to provide clocks for the latches. The digital outputs and clocks are available at the standard 40-pin connectors J1 and J2.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the associated components and the analog section of the AD10465. The digital outputs of the AD10465 are powered via banana jacks with 3.3 V. Contact the factory if additional layout or applications assistance is required.

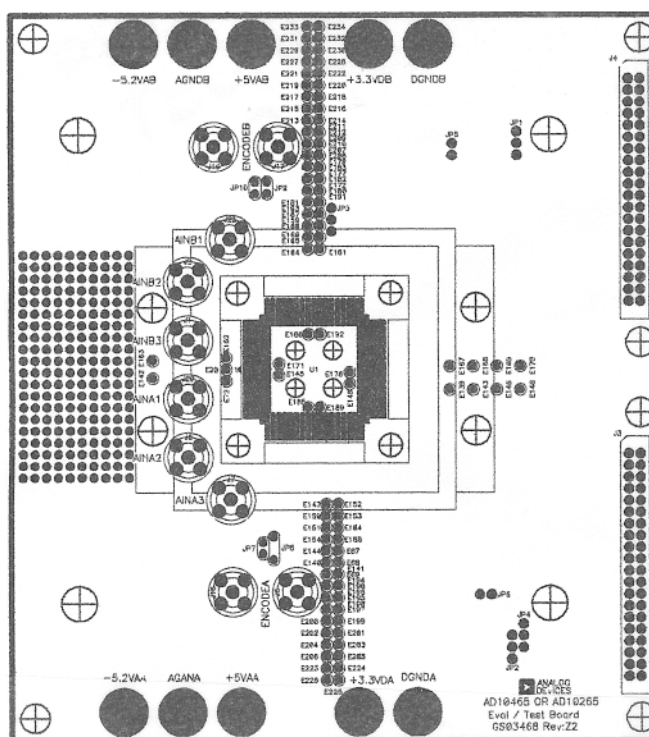


Figure 9a. Evaluation Board Mechanical Layout

AD10465

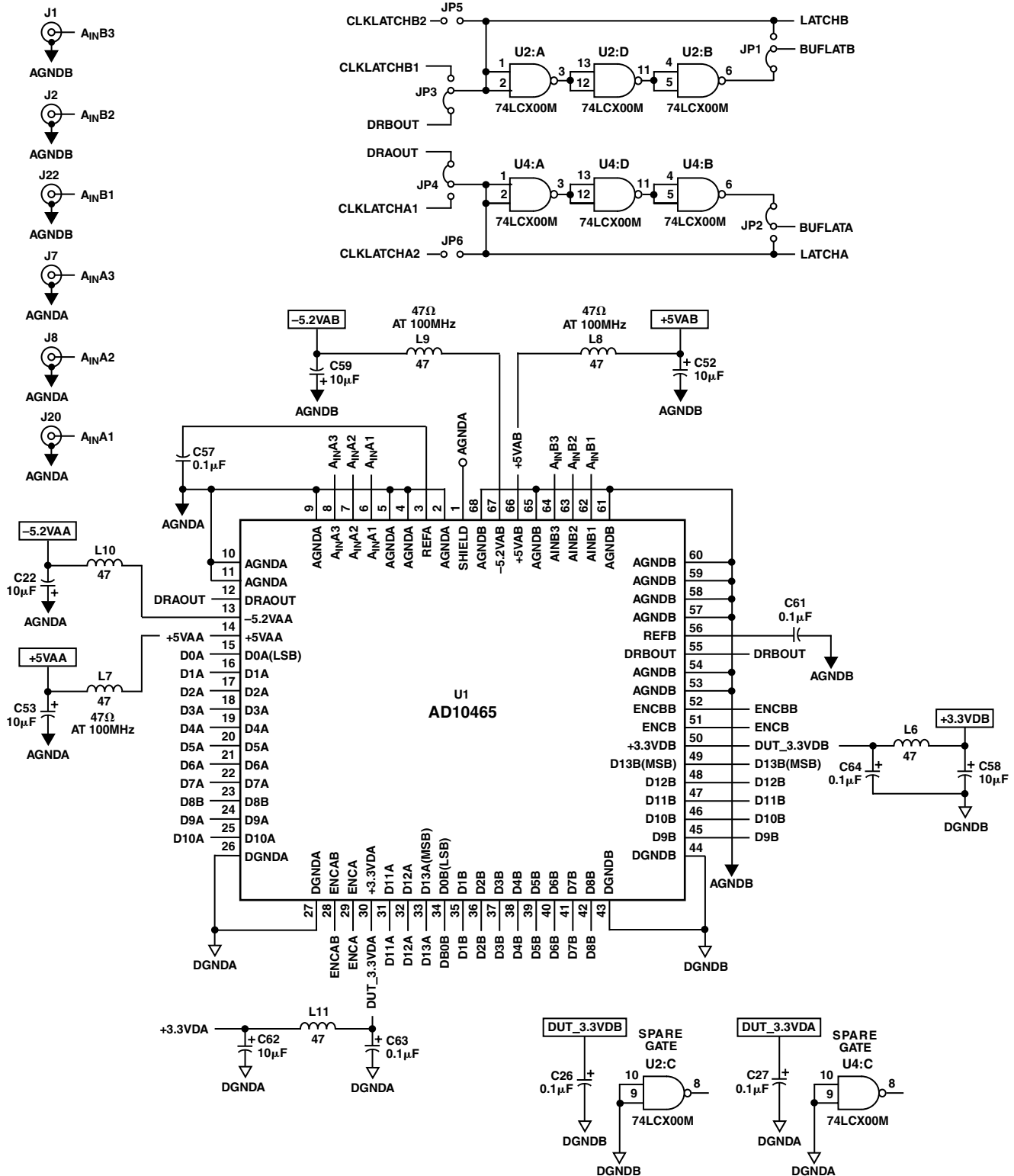


Figure 9b. Evaluation Board

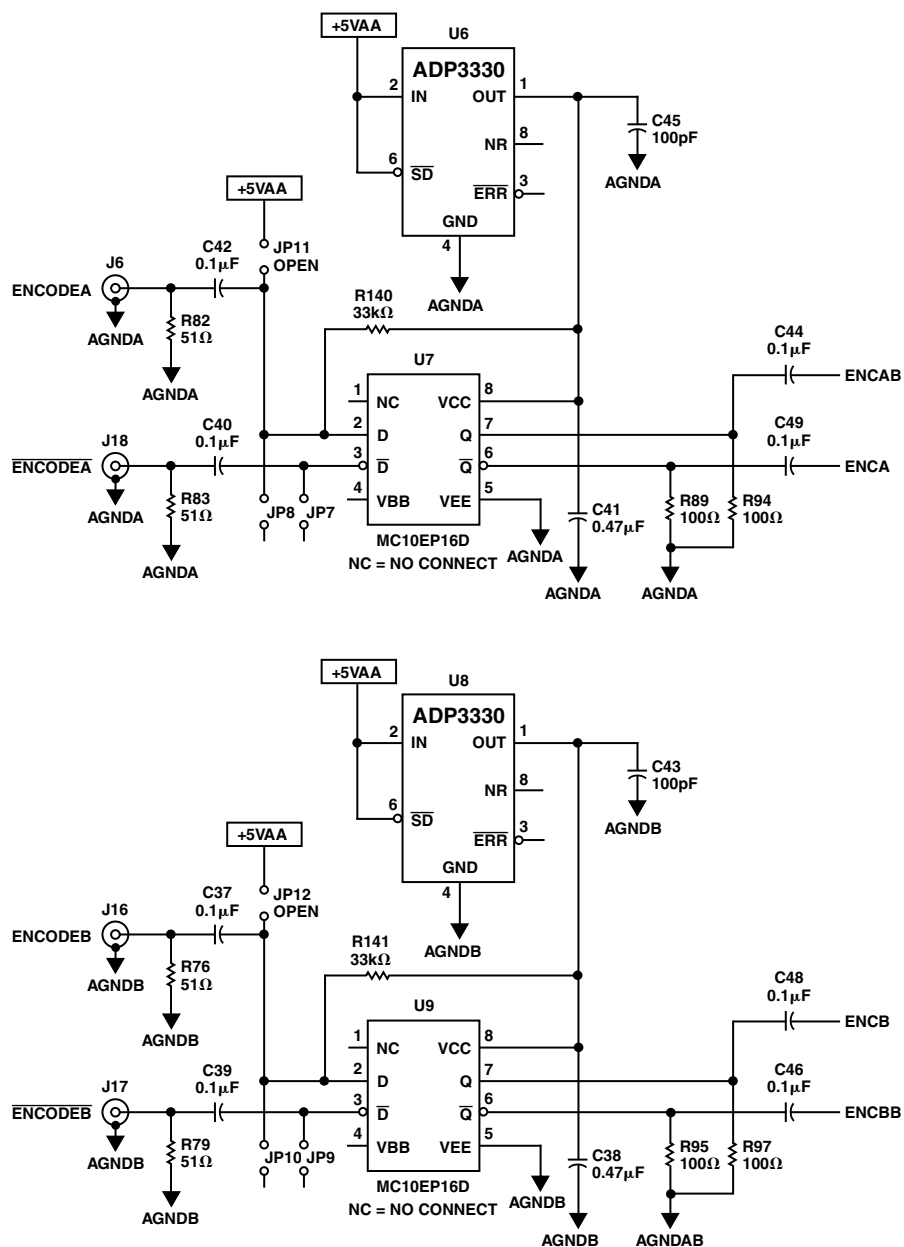


Figure 9c. Evaluation Board

AD10465

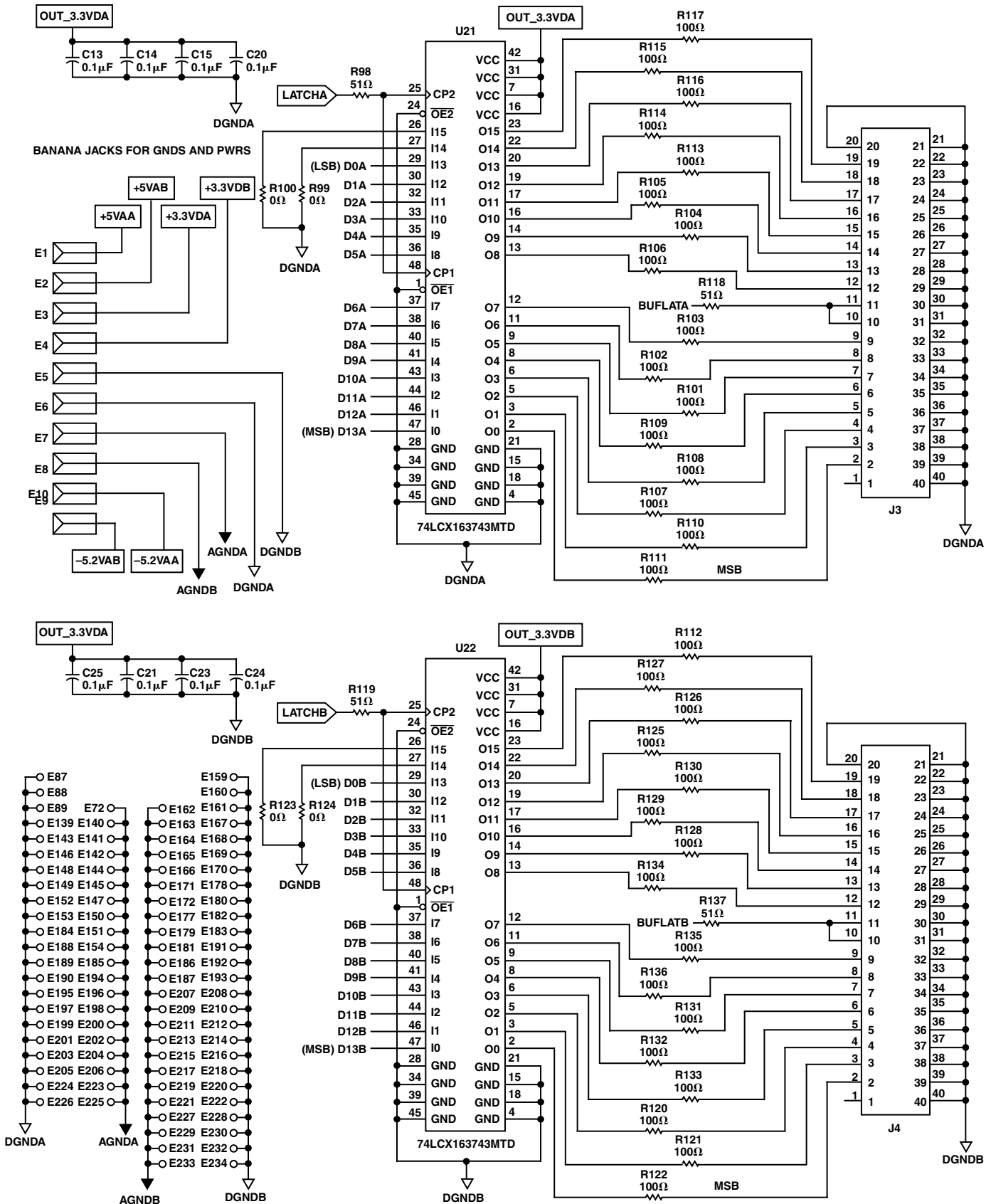


Figure 9d. Evaluation Board

Bill of Materials List for AD10465 Evaluation Board

| Qty | Reference Designator | Value | Description | Manufacturer and Part Number | Component Name |
|-----|--|-----------------|---|------------------------------------|---------------------|
| 2 | U2, U4 | | IC, Low-Voltage Quad 2-Input Nand, SOIC-14 | Toshiba/TC74LCX00FN | 74LCX00M |
| 2 | U21, U22 | | IC, 16-Bit Transparent Latch with Three-State Outputs, TSSOP-48 | Fairchild/74LCX163743MTD | 74LCX163743MTD |
| 1 | U1 | | DUT, IC 14-Bit Analog-to-Digital Converter | ADI/AD10465AZ | ADI/AD10465AZ |
| 2 | U6, U8 | | IC, Voltage Regulator 3.3 V, RT-6 | Analog Devices/ADP3330ART-3, 3-RLT | ADP3330 |
| 10 | E1–E10 | | Banana Jack, Socket | Johnson Components/08-0740-001 | Banana Hole |
| 22 | C13–C15, C20, C21, C23–C27, C37, C39, C40, C42, C44, C46, C48, C49, C57, C61, C63, C64 | 0.1 μ F | Capacitor, 0.1 μ F, 20%, 12 V dc, 0805 | Mena/GRM40X7R104K025BL | CAP 0805 |
| 2 | C38, C41 | 0.47 μ F | Capacitor, 0.47 μ F, 5%, 12 V dc, 1206 | Vitramon/VJ1206U474MFXMB | CAP 1206 |
| 2 | C43, C45 | 100 pF | Capacitor, 100 pF, 10%, 12 V dc, 0805 | Johansen/500R15N101JV4 | CAP 0805 |
| 2 | J3, J4 | | Connector, 40-pin Header Male St. | Samtec/TSW-120-08-G-D | HD40M |
| 6 | L6–L11 | 47 μ H | Inductor, 47 μ H @ 100 MHz, 20%, IND2 | Fair-Rite/2743019447 | IND2 |
| 2 | U7, U9 | | IC, Differential Receiver, SOIC-8 | Motorola/MC10EP16D | MC10EP16D |
| 6 | C22, C50, C52, C53, C59, C62 | 10 μ F | Capacitor, 10 μ F, 20%, 16 V dc, 1812POL | Kemet/T491C106M016A57280 | POLCAP 1812 |
| 4 | R99, R100, R123, R124 | 0.0 Ω | Resistor, 0.0 Ω , 0805 | Panasonic/ERJ-6GEY0R00V | RES2 0805 |
| 2 | R140, R141 | 33,000 Ω | Resistor, 33,000 Ω , 5%, 0.10 Watt, 0805 | Panasonic/ERJ-6GEYJ333V | RES2 0805 |
| 8 | R76, R79, R82, R83, R98, R118, R119, R137 | 51 Ω | Resistor, 51 Ω , 5%, 0.10 Watt, 0805 | Panasonic/ERJ-6GEYJ510V | RES2 0805, RES 0805 |
| 36 | R89, R94, R95, R97, R101–R117, R120–R122, R125–R136 | 100 Ω | Resistor, 100 Ω , 5%, 0.10 Watt, 0805 | Panasonic/ERJ-6GEYJ101V | RES2 0805, RES 0805 |
| 8 | J1, J2, J6–J8, J16–J18, J20, J22 | | Connector, SMA Female St. | Johnson Components/142-0701-201 | SMA |

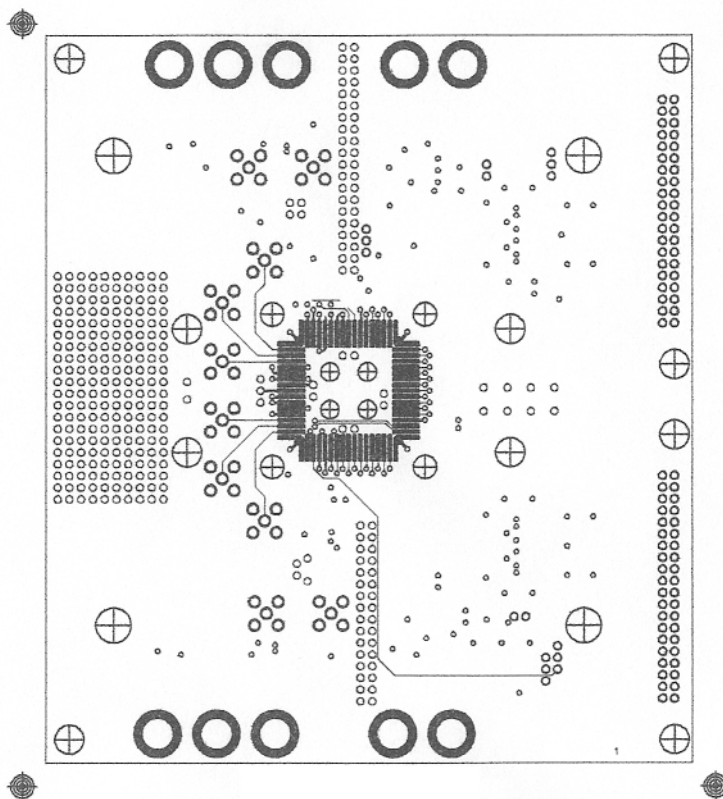


Figure 10a. Top Layer Copper

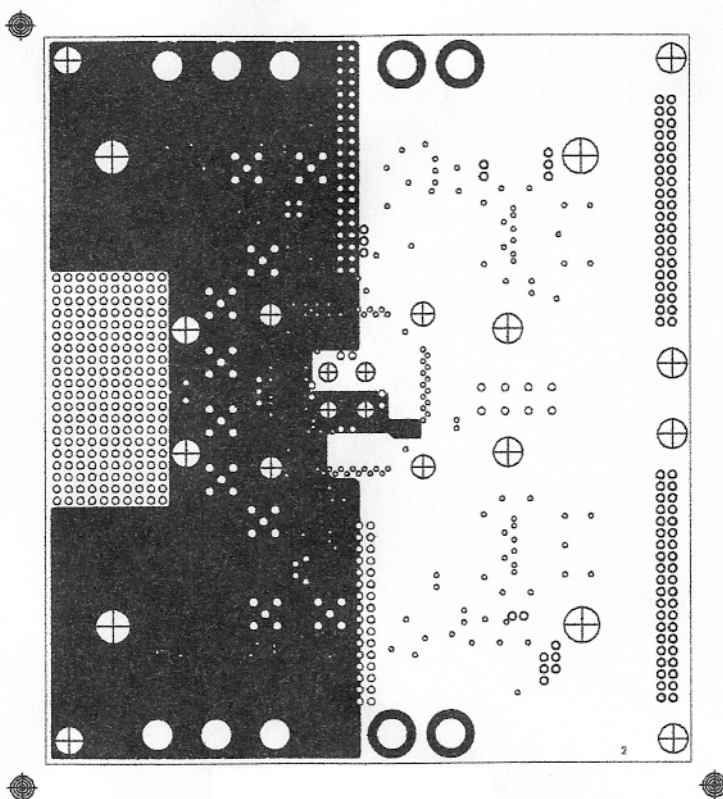


Figure 10b. Second Layer Copper

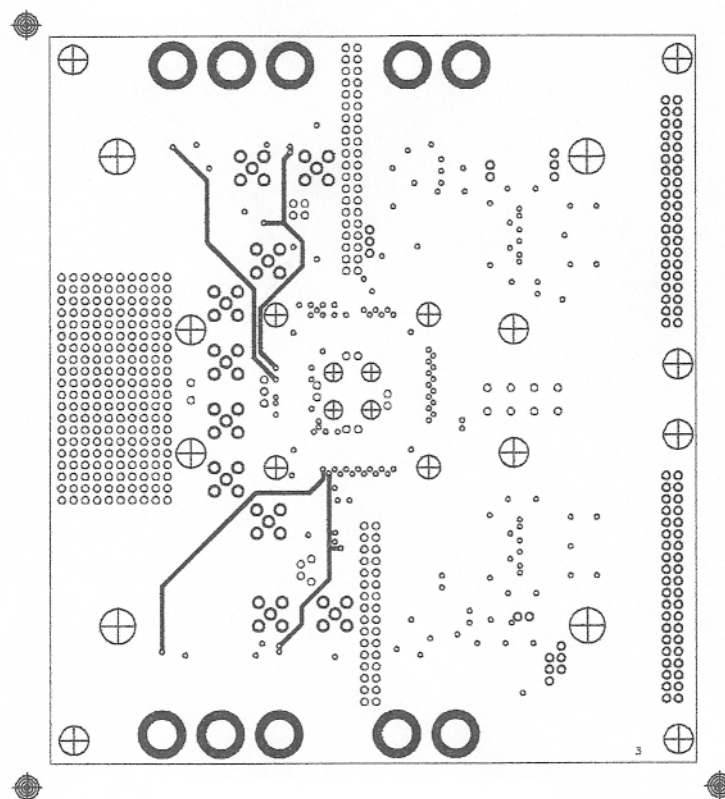


Figure 10c. Third Layer Copper

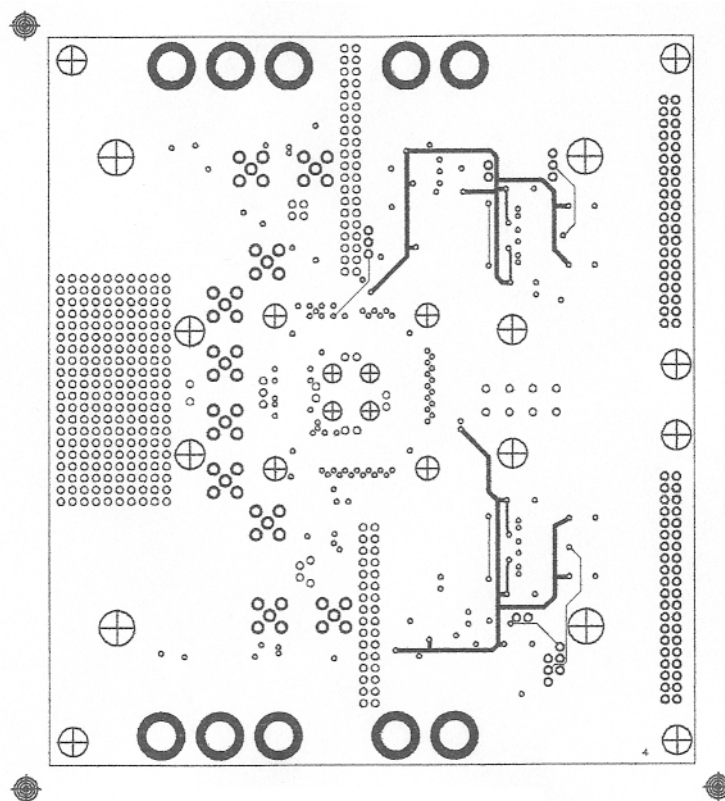


Figure 10d. Fourth Layer Copper

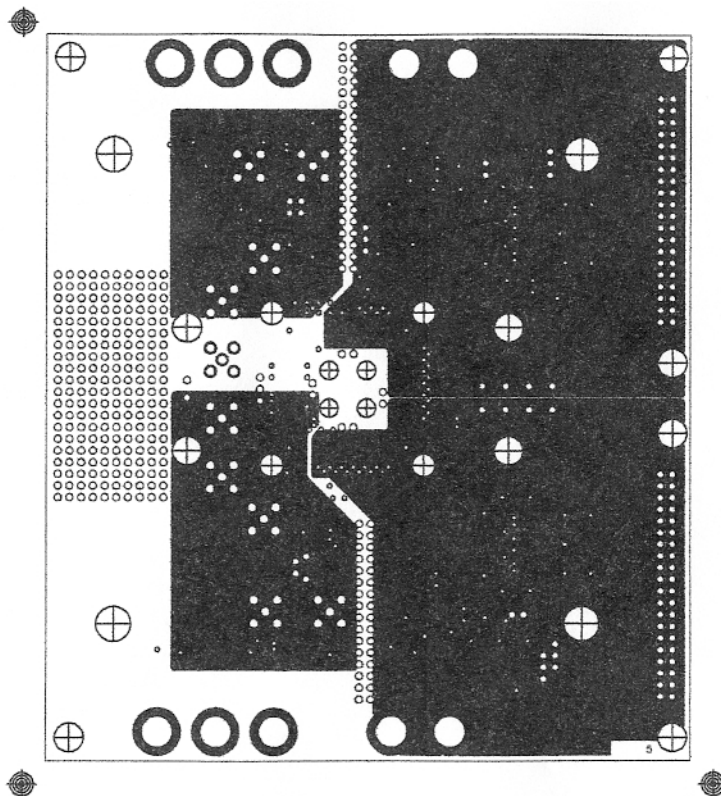


Figure 10e. Fifth Layer Copper

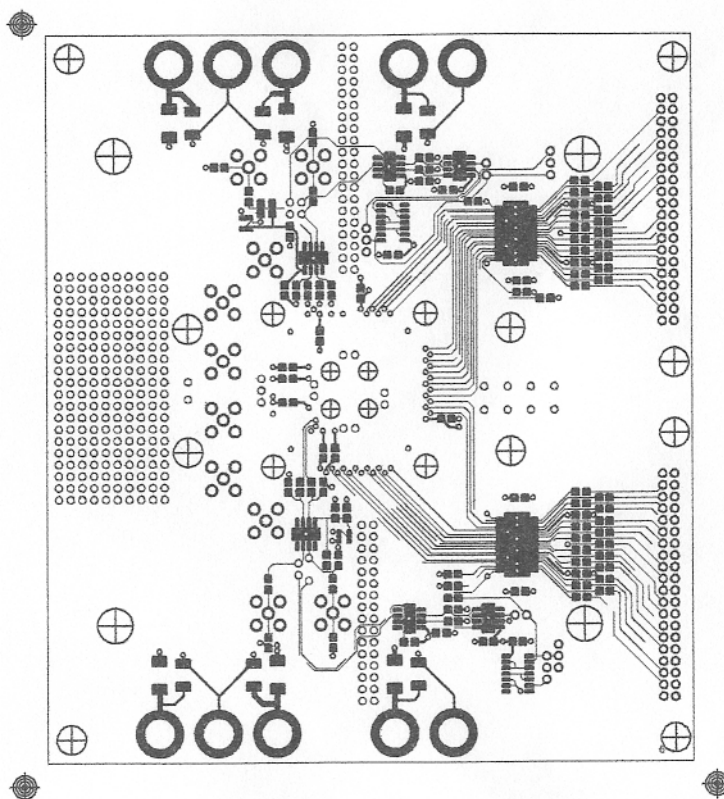


Figure 10f. Bottom Layer Copper

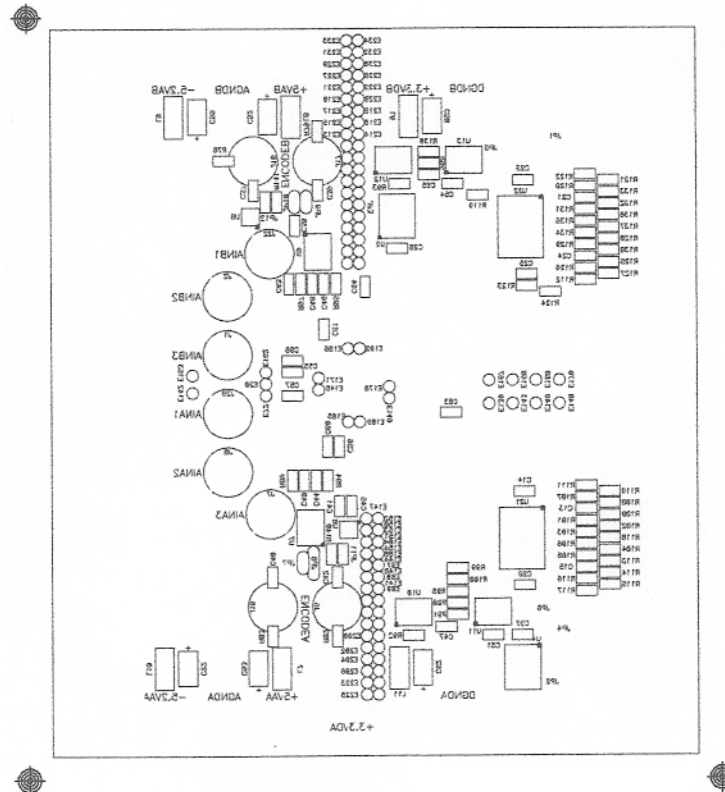


Figure 10g. Bottom Silkscreen

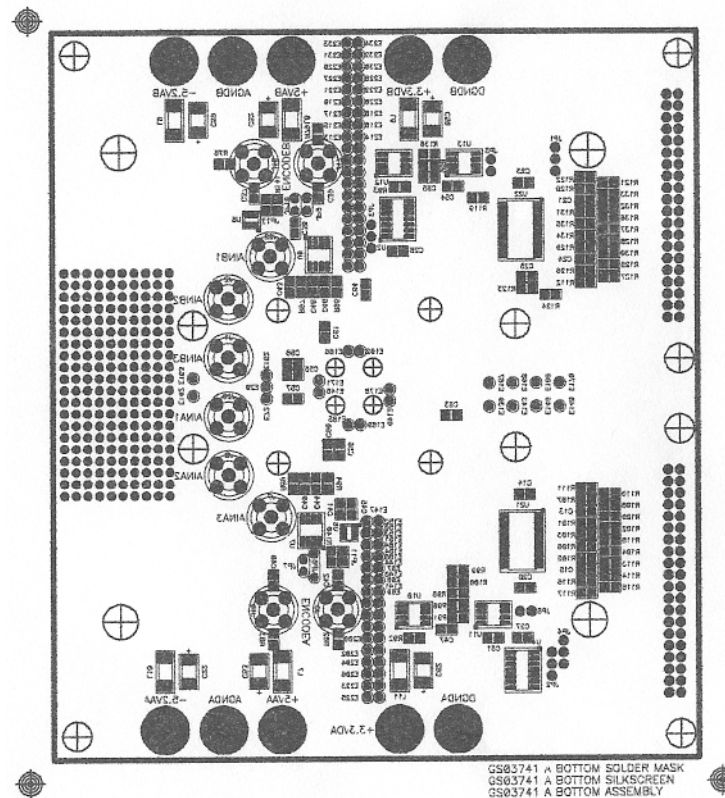
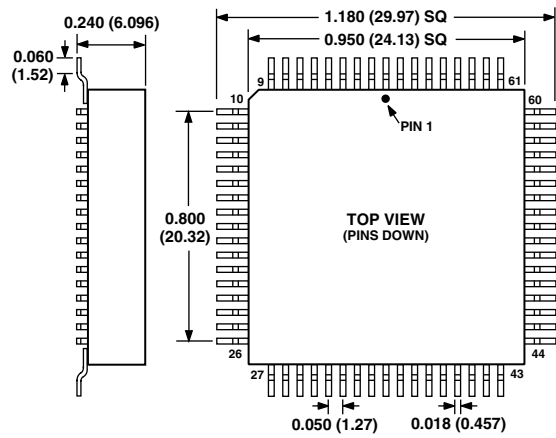


Figure 10h. Bottom Assembly

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

68-Lead Ceramic Leaded Chip Carrier
(ES-68A)



C02356-4.5-1/01 (rev. 0)

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