NID5001N

Preferred Device

Self-protected FET with Temperature and Current Limit

HDPlus devices are an advanced series of power MOSFETs which utilize ON Semicondutor's latest MOSFET technology process to achieve the lowest possible on−resistance per silicon area while incorporating smart features. Integrated thermal and current limits work together to provide short circuit protection. The devices feature an integrated Drain−to−Gate Clamp that enables them to withstand high energy in the avalanche mode. The Clamp also provides additional safety margin against unexpected voltage transients. Electrostatic Discharge (ESD) protection is provided by an integrated Gate−to−Source Clamp.

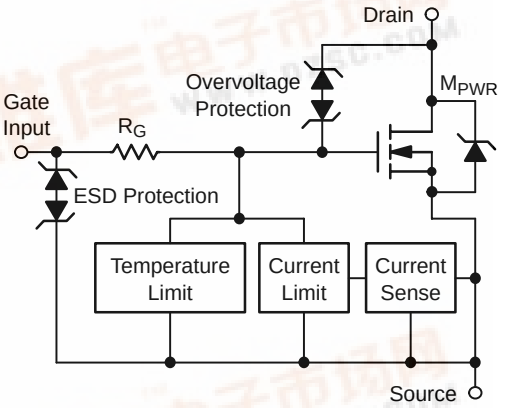
Features

- Low $R_{DS(on)}$
- Current Limitation
- Thermal Shutdown with Automatic Restart
- Short Circuit Protection
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Slew Rate Control for Low Noise Switching
- Overvoltage Clamped Protection

ON Semiconductor®

http://onsemi.com

V_{DSS} (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX (Limited)
42 V	23 mΩ @ 10 V	33 A*



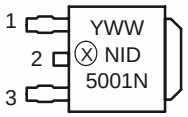
MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	Vdc
Drain−to−Gate Voltage Internally Clamped (R_{GS} = 1.0 MΩ)	V_{DGR}	42	Vdc
Gate−to−Source Voltage	V_{GS}	±14	Vdc
Drain Current Continuous	I_D	Internally Limited	
Total Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 64 1.0 1.56	W
Thermal Resistance − Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.95 120 80	°C/W
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 4.5 Apk, L = 120 mH, R_G = 25 Ω)	E_{AS}	1215	mJ
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

1. Minimum FR4 PCB, steady state.
2. Mounted onto a 2″ square FR4 board (1″ square, 2 oz. Cu 0.06″ thick single−sided, t = steady state).

DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM



NID5001N = Device Code
Y = Year
WW = Work Week
1 = Gate
2 = Drain
3 = Source

ORDERING INFORMATION

Device	Package	Shipping†
NID5001NT4	DPAK	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

*Max current may be limited below this value depending on input conditions.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = 150°C)	$V_{(BR)DSS}$	 42 42	 46 44	 50 50	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}		 1.5 6.5	 5.0	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc)	I_{GSSF}		50	100	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.2 mAdc) Threshold Temperature Coefficient	$V_{GS(th)}$	1.0	1.8 5.0	2.0	Vdc −mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 10 Vdc, I_D = 5.0 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 5.0 Adc, T_J @ 150°C)	$R_{DS(on)}$		 23 43	 29 55	mΩ
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J @ 150°C)	$R_{DS(on)}$		 28 50	 34 60	mΩ
Source−Drain Forward On Voltage (I_S = 5 A, V_{GS} = 0 V)	V_{SD}		0.80	1.1	V
SWITCHING CHARACTERISTICS					
Turn−on Time	V_{GS} = 5.0 V_{dc} V_{DD} = 25 V_{dc} I_D = 1.0 A_{dc} Ext R_G = 2.5 Ω	$T_{(on)}$		32	40	μs
Turn−off Time		$T_{(off)}$		68	75	
Turn−on Time	V_{GS} = 10 V_{dc} V_{DD} = 25 V_{dc} I_D = 1.0 A_{dc} Ext R_G = 2.5 Ω	$T_{(on)}$		11	15	μs
Turn−off Time		$T_{(off)}$		86	95	
Slew Rate On	R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V	$-dV_{DS}/dt_{on}$		0.5		V/μs
Slew−Rate Off	R_L = 4.7 Ω, V_{in} = 10 to 0 V, V_{DD} = 12 V	dV_{DS}/dt_{off}		0.35		V/μs

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Current Limit	(V_{GS} = 5.0 Vdc) V_{DS} = 10 V (V_{GS} = 5.0 Vdc, T_J = 150°C)	I_{LIM}	21 12	30 19	36 30	Adc
	(V_{GS} = 10 Vdc) V_{DS} = 10 V (V_{GS} = 10 Vdc, T_J = 150°C)		29 13	41 24	49 31	Adc
Temperature Limit (Turn−off)	V_{GS} = 5.0 Vdc	$T_{LIM(off)}$	150	175	200	°C
Temperature Limit (Circuit Reset)	V_{GS} = 5.0 Vdc	$T_{LIM(on)}$	135	160	185	°C
Temperature Limit (Turn−off)	V_{GS} = 10 Vdc	$T_{LIM(off)}$	150	165	185	°C
Temperature Limit (Circuit Reset)	V_{GS} = 10 Vdc	$T_{LIM(on)}$	135	150	170	°C

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electro−Static Discharge Capability Human Body Model (HBM) Machine Model (MM)	ESD	 4000 400			V

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

TYPICAL PERFORMANCE CURVES

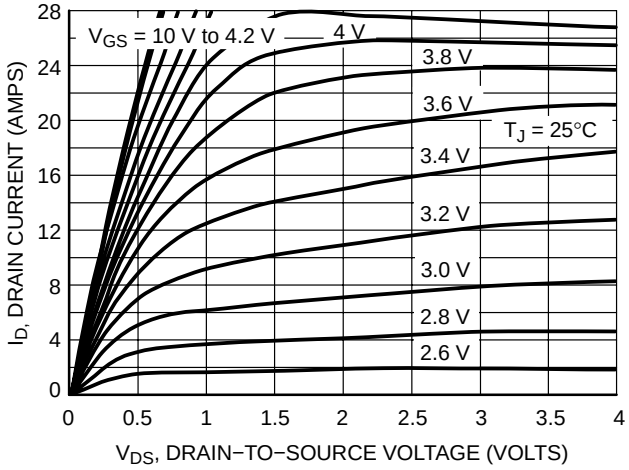


Figure 1. On−Region Characteristics

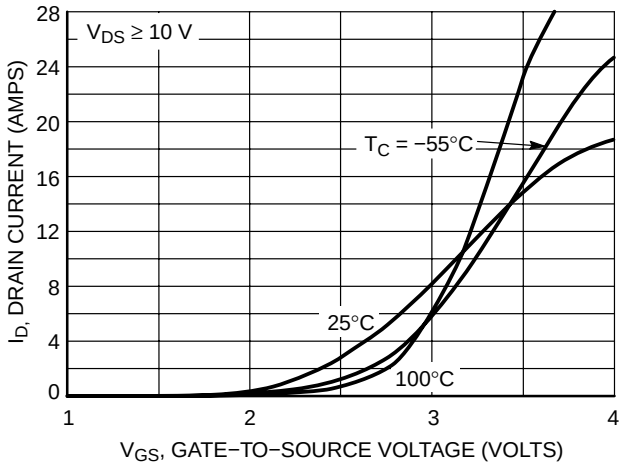


Figure 2. Transfer Characteristics

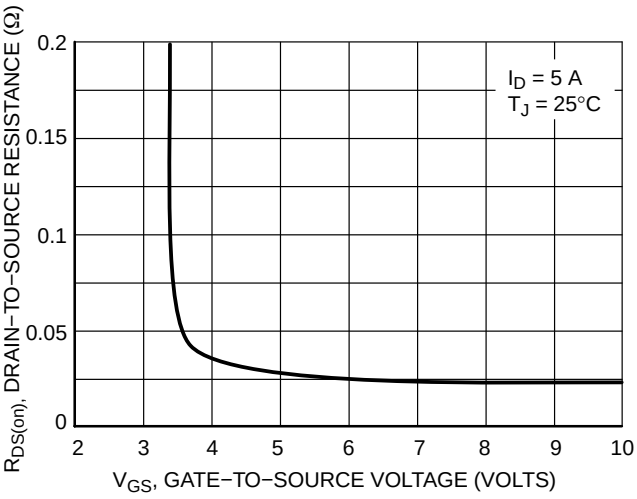


Figure 3. On−Resistance vs. Gate−to−Source Voltage

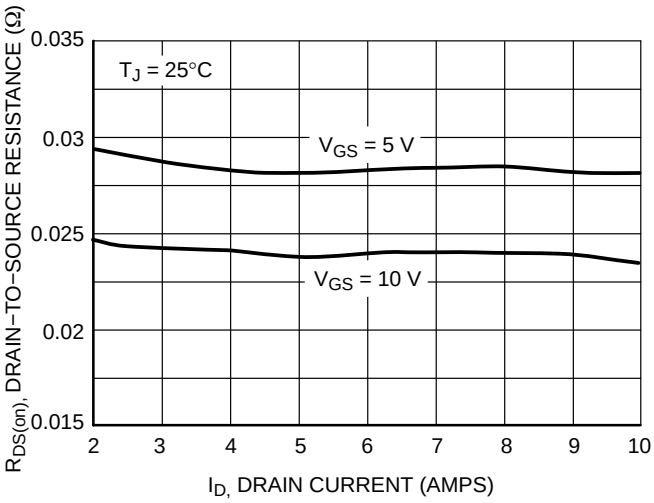


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

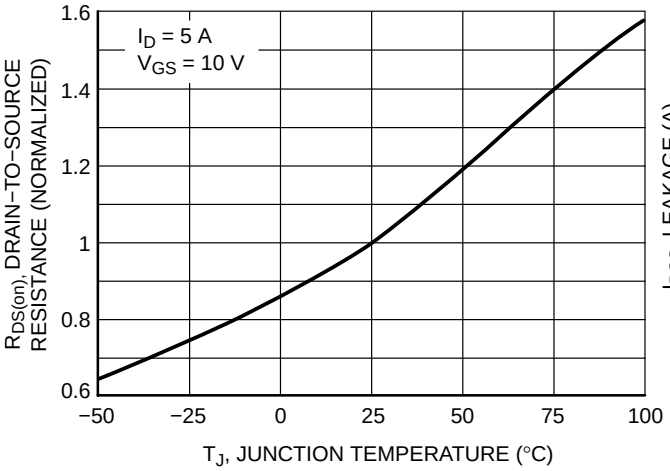


Figure 5. On−Resistance Variation with Temperature

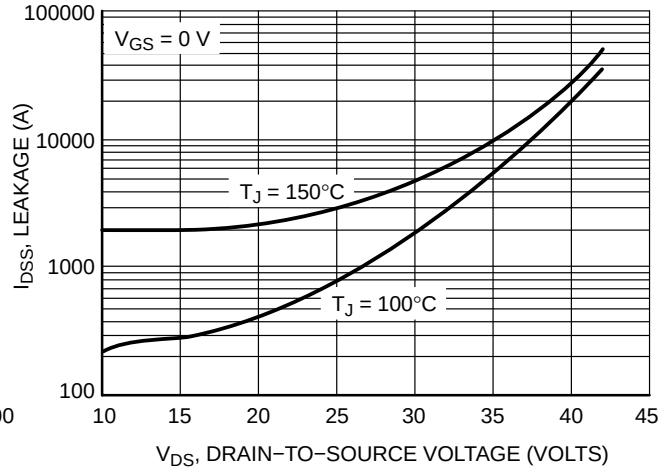


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

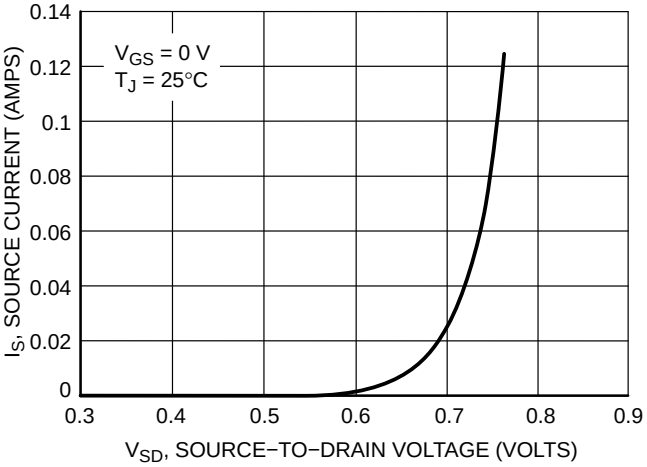


Figure 7. Diode Forward Voltage vs. Current

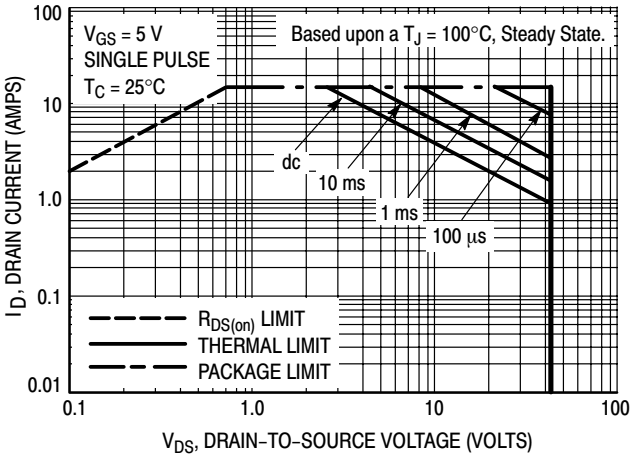
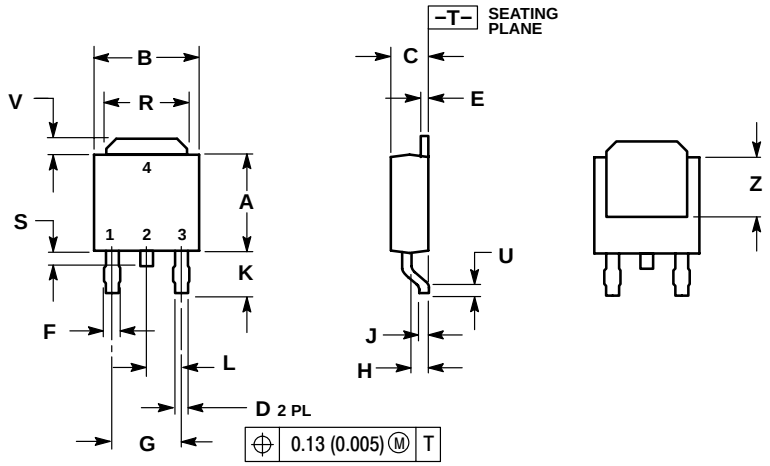


Figure 8. Maximum Rated Forward Biased Safe Operating Area

NID5001N

PACKAGE DIMENSIONS

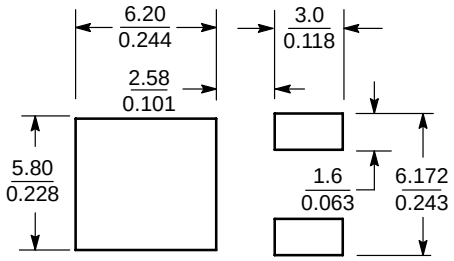
DPAK
CASE 369C−01
ISSUE O



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NID5001N

PUBLICATION ORDERING INFORMATION

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