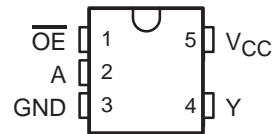


SN74LVC1G240 SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT

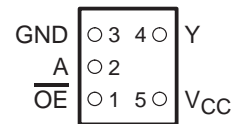
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- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This single buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G240 is a single line driver with a 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE† | ORDERABLE PART NUMBER | TOP-SIDE MARKING‡ |
|---------------|--|-----------------------|-------------------|
| –40°C to 85°C | NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA | SN74LVC1G240YEAR | _ _ _CK_ |
| | NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free) | SN74LVC1G240YZAR | |
| | NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP | SN74LVC1G240YEPR | |
| | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | SN74LVC1G240YZPR | |
| | SOT (SOT-23) – DBV | SN74LVC1G240DBVR | C40_ |
| | | SN74LVC1G240DBVT | |
| | SOT (SC-70) – DCK | SN74LVC1G240DCKR | CK_ |
| | | SN74LVC1G240DCKT | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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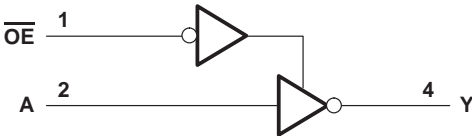
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description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

| FUNCTION TABLE | | |
|-----------------|---|--------|
| INPUTS | | OUTPUT |
| \overline{OE} | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 6.5 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 6.5 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 6.5 V |
| Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Continuous output current, I_O | ±50 mA |
| Continuous current through V_{CC} or GND | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): | |
| DBV package | 206°C/W |
| DCK package | 252°C/W |
| YEA/YZA package | 154°C/W |
| YEP/YZP package | 132°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC1G240

SINGLE BUFFER/DRIVER

WITH 3-STATE OUTPUT

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recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|---|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 |
| | | Data retention only | 1.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | |
| | | V _{CC} = 3 V to 3.6 V | 2 | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | 0.8 | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.3 × V _{CC} | |
| V _I | Input voltage | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | –4 | mA |
| | | V _{CC} = 2.3 V | –8 | |
| | | V _{CC} = 3 V | –16 | |
| | | | –24 | |
| | | V _{CC} = 4.5 V | –32 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | mA |
| | | V _{CC} = 2.3 V | 8 | |
| | | V _{CC} = 3 V | 16 | |
| | | | 24 | |
| | | V _{CC} = 4.5 V | 32 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | 5 | |
| T _A | Operating free-air temperature | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC1G240

SINGLE BUFFER/DRIVER

WITH 3-STATE OUTPUT

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP† | MAX | UNIT |
|------------------|--|-------------------------------|----------------------|------|------|------|
| V _{OH} | I _{OH} = -100 µA | 1.65 V to 5.5 V | V _{CC} -0.1 | | | V |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -8 mA | 2.3 V | 1.9 | | | |
| | I _{OH} = -16 mA | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | | 2.3 | | | |
| | I _{OH} = -32 mA | 4.5 V | 3.8 | | | |
| V _{OL} | I _{OL} = 100 µA | 1.65 V to 5.5 V | | | 0.1 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.3 | |
| | I _{OL} = 16 mA | 3 V | | | 0.4 | |
| | I _{OL} = 24 mA | | | | 0.55 | |
| | I _{OL} = 32 mA | 4.5 V | | | 0.55 | |
| I _I | A or \overline{OE} inputs | V _I = 5.5 V or GND | | | ±5 | µA |
| I _{off} | V _I or V _O = 5.5 V | 0 | | | ±10 | µA |
| I _{OZ} | V _O = 0 to 5.5 V | 3.6 V | | | 10 | µA |
| I _{CC} | V _I = 5.5 V or GND, I _O = 0 | 1.65 V to 5.5 V | | | 10 | µA |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | | | 500 | µA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | 4 | | pF |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|-----------------|--------------|-------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 2.1 | 6.9 | 0.9 | 4.6 | 0.7 | 3.7 | 0.5 | 3.4 | ns |

switching characteristics over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

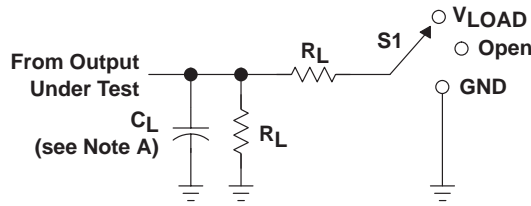
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|------------------|-----------------|-------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 3 | 8.6 | 1.4 | 5.5 | 1.1 | 4.5 | 1 | 4 | ns |
| t _{en} | \overline{OE} | Y | 3.8 | 10 | 2.1 | 6.5 | 1.4 | 5.4 | 1.1 | 5.2 | ns |
| t _{dis} | \overline{OE} | Y | 2.1 | 9.4 | 1 | 4.9 | 1.4 | 5.2 | 1 | 4.1 | ns |

operating characteristics, T_A = 25°C

| PARAMETER | | | TEST CONDITIONS | V _{CC} = 1.8 V ± 0.15 V | V _{CC} = 2.5 V ± 0.2 V | V _{CC} = 3.3 V ± 0.3 V | V _{CC} = 5 V ± 0.5 V | UNIT |
|-----------------|-------------------------------|------------------|-----------------|-------------------------------------|------------------------------------|------------------------------------|----------------------------------|------|
| | | | | TYP | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance | Outputs enabled | f = 10 MHz | 17 | 17 | 18 | 20 | pF |
| | | Outputs disabled | | 1 | 1 | 1 | 3 | |



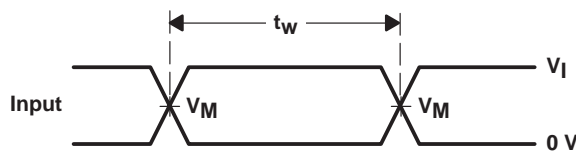
PARAMETER MEASUREMENT INFORMATION



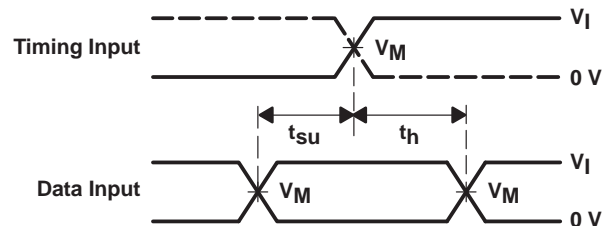
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

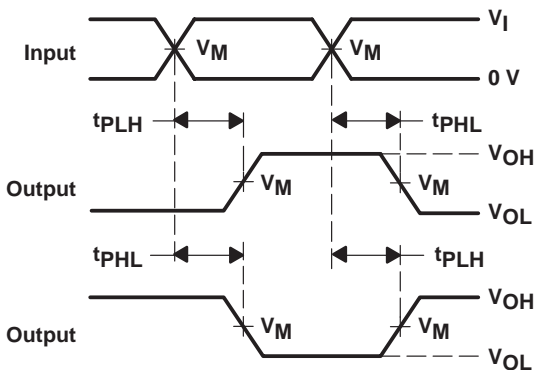
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



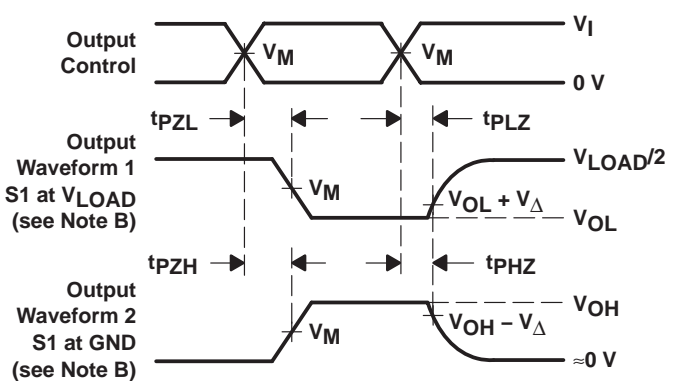
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC1G240

SINGLE BUFFER/DRIVER

WITH 3-STATE OUTPUT

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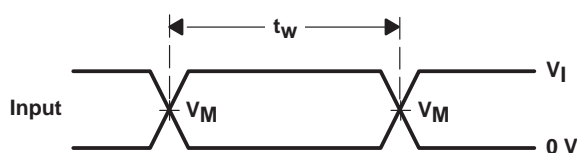
PARAMETER MEASUREMENT INFORMATION



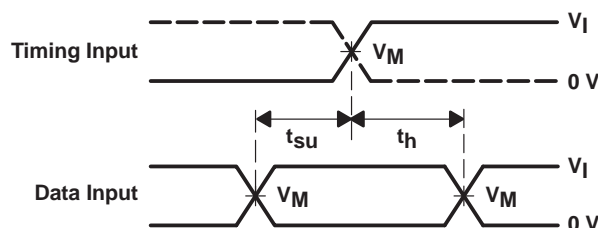
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

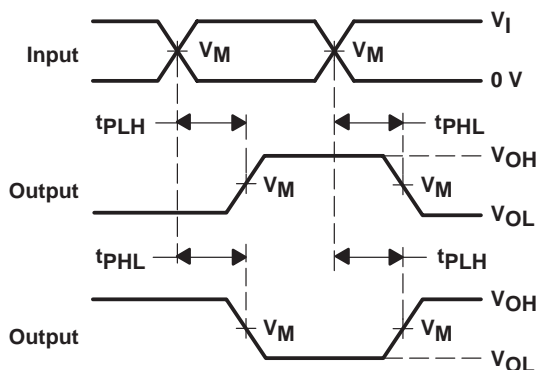
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



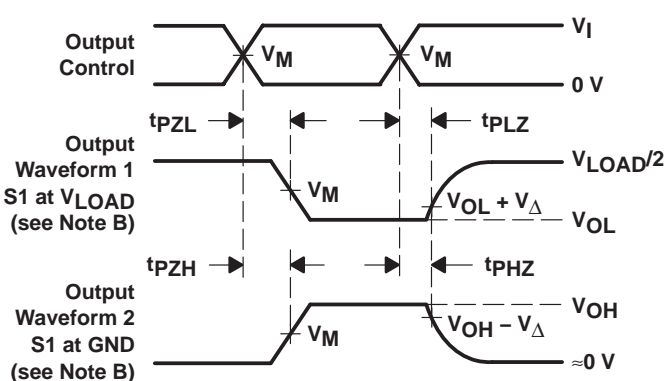
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



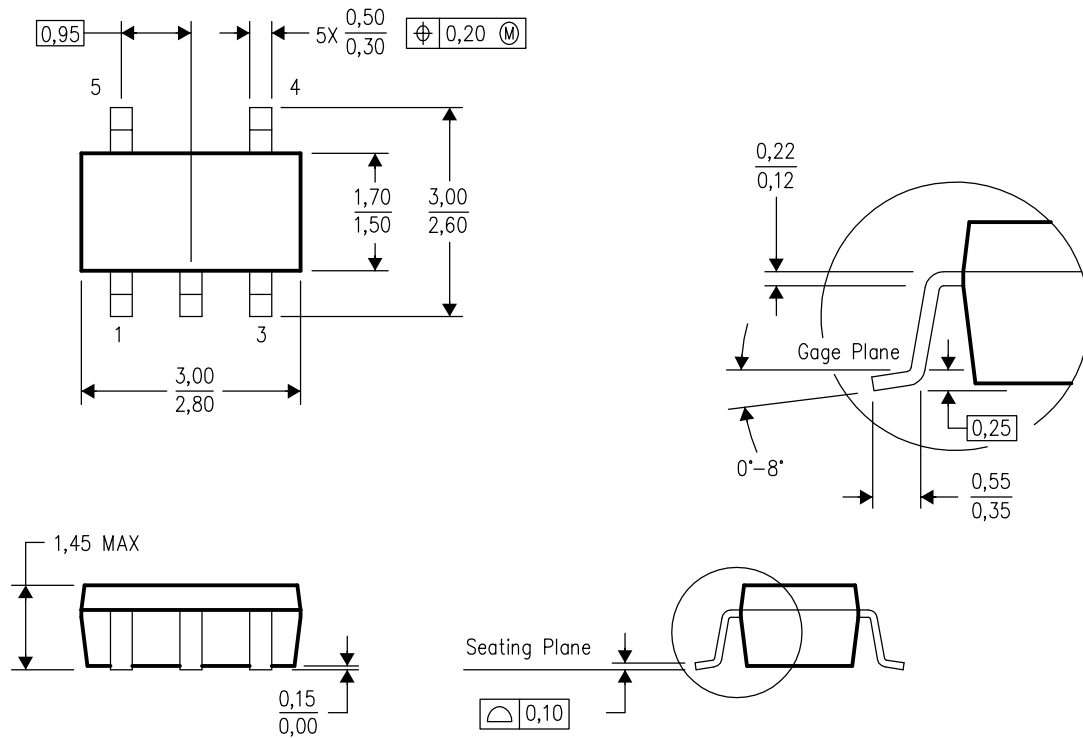
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

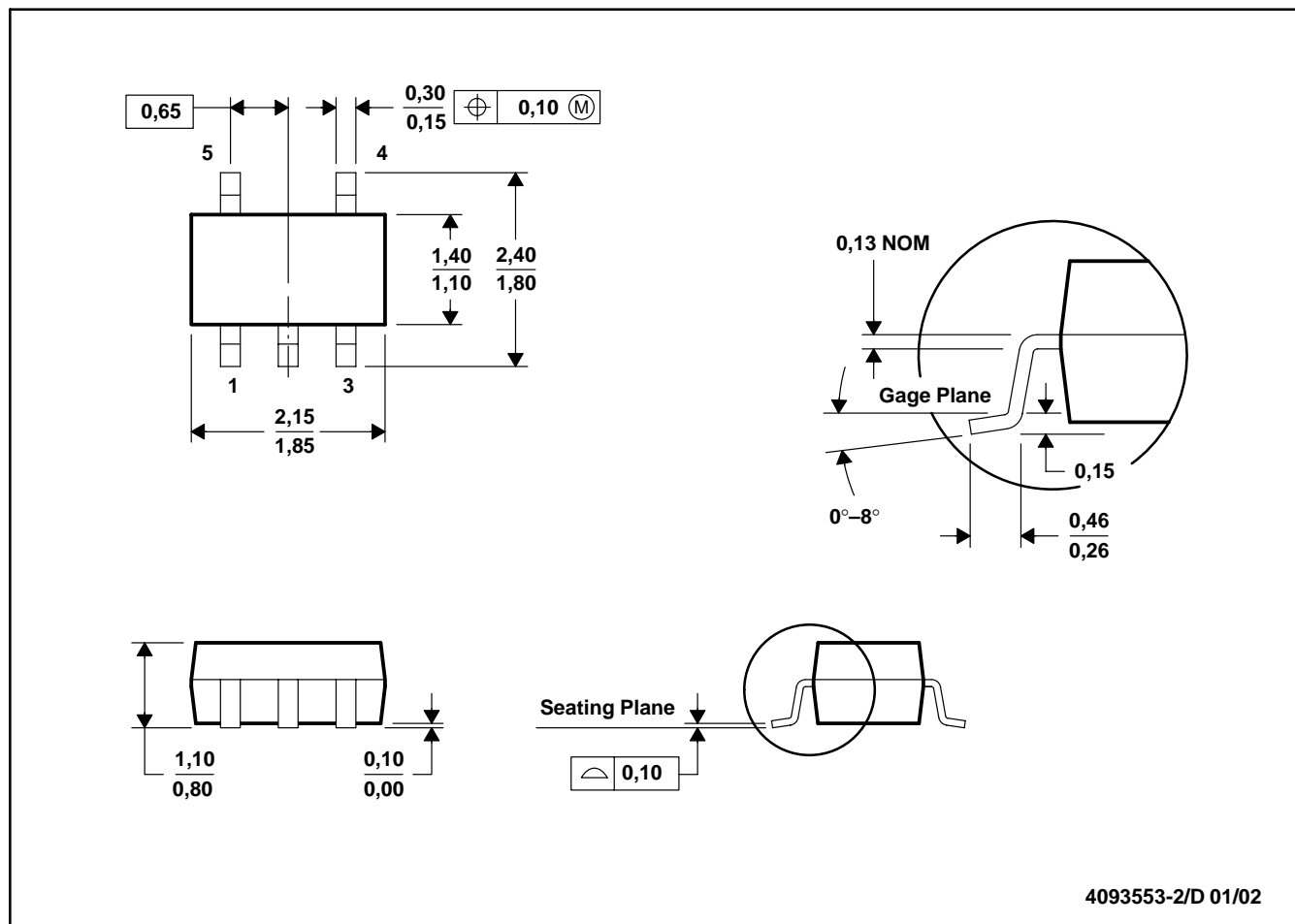


4073253-4/H 10/2003

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178 Variation AA.

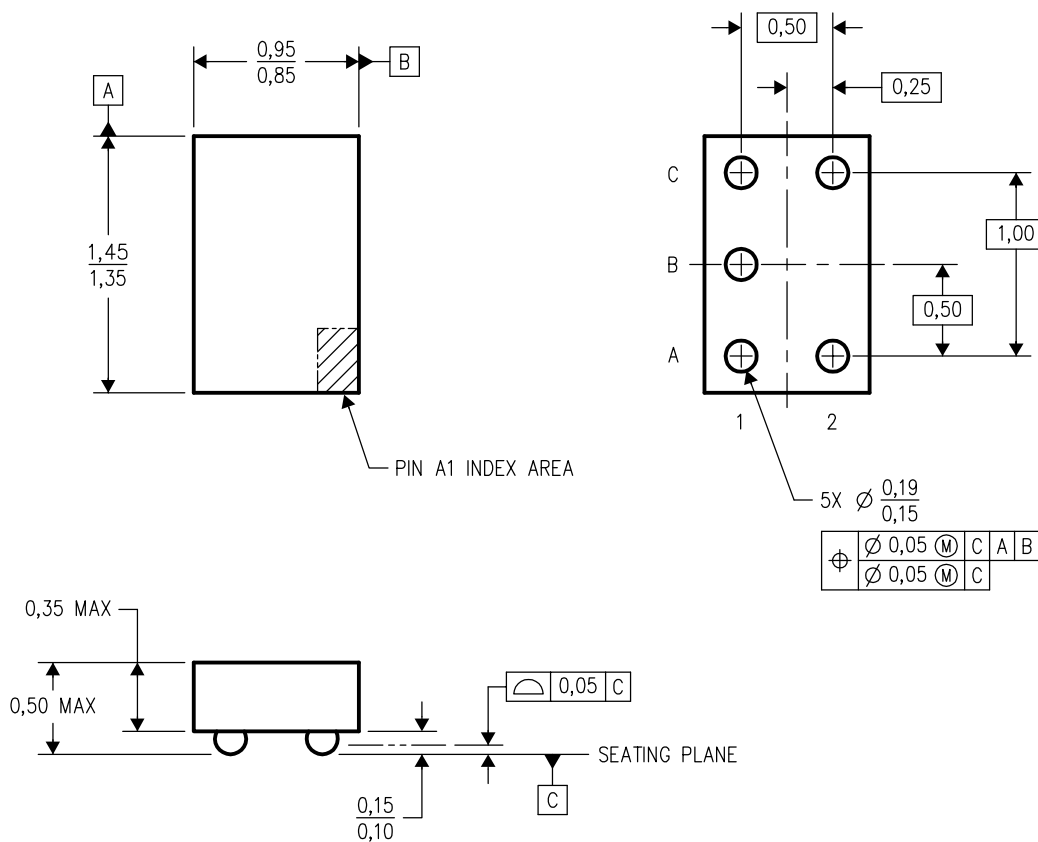
DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



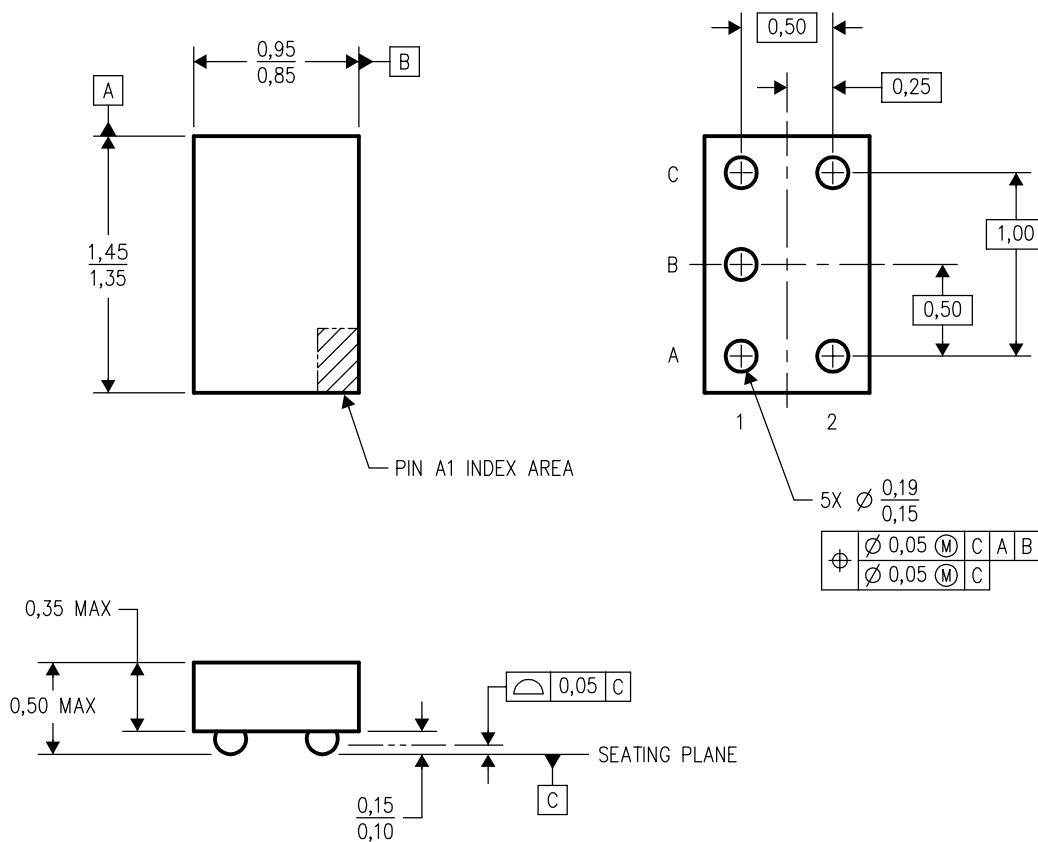
4203167-2/C 04/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



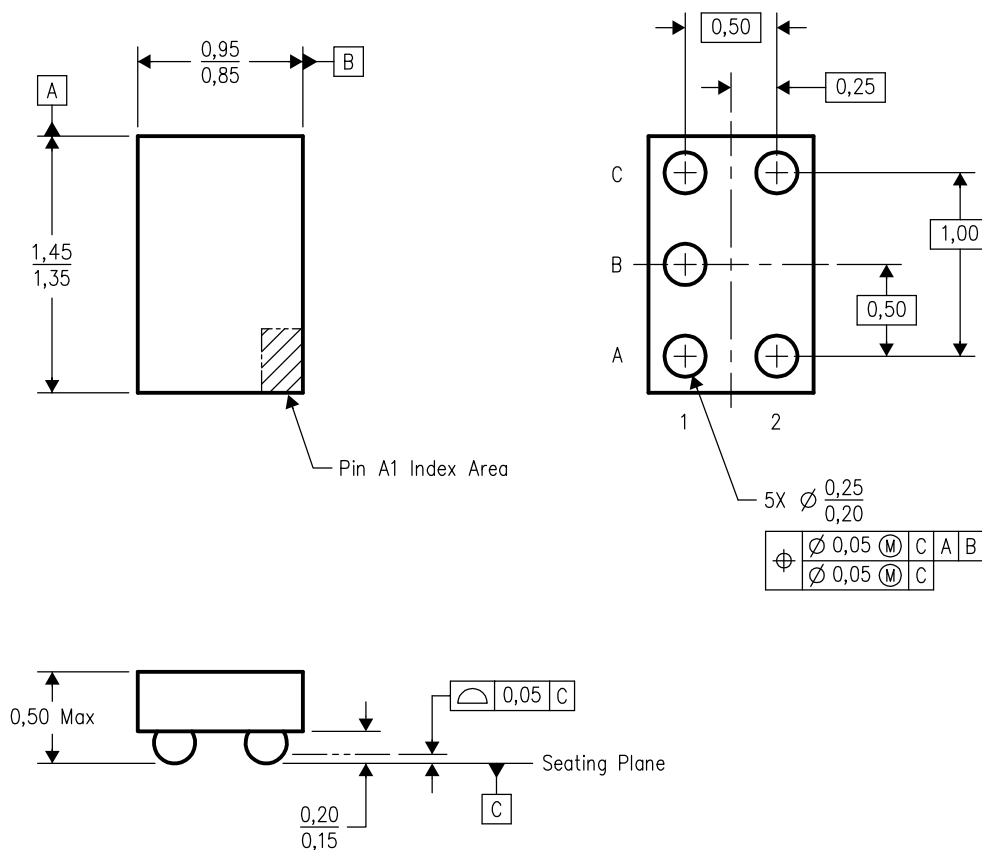
4204151-2/B 03/2002

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - NanoFree™ package configuration.
 - Package complies to JEDEC MO-211 variation EA.
 - This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

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YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



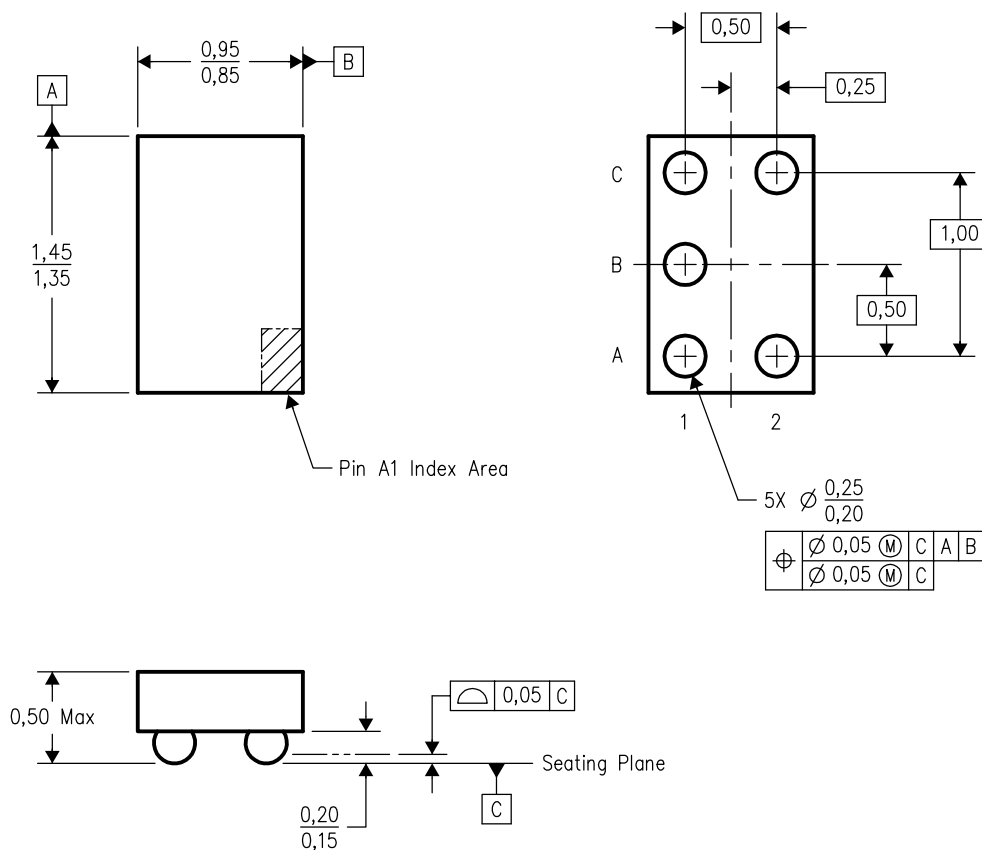
4204741-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

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| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
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