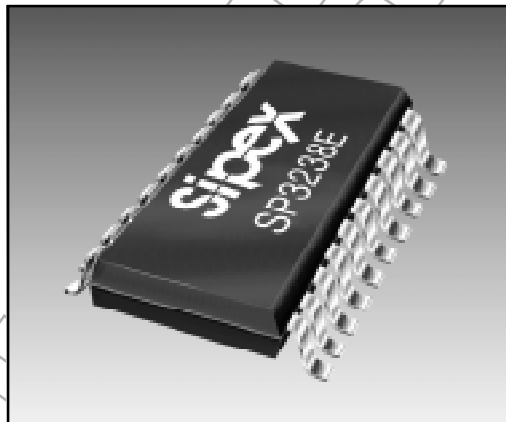


## Intelligent +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- **Auto-Online™** circuitry automatically wakes up from a 1 $\mu$ A shutdown
- Minimum 250Kbps data rate under load
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V<sub>CC</sub> Variations
- Enhanced ESD Specifications:
  - +15KV Human Body Model
  - +15KV IEC1000-4-2 Air Discharge
  - +8KV IEC1000-4-2 Contact Discharge



### DESCRIPTION

The **SP3238E** device is an RS-232 transceiver solution intended for portable or hand-held applications such as notebook and palmtop computers. The **SP3238E** uses an internal high-efficiency, charge-pump power supply that requires only 0.1 $\mu$ F capacitors in 3.3V operation. This charge pump and **Sipex's** driver architecture allow the **SP3238E** device to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.0V. The **SP3238E** is a 5-driver/3-receiver device, ideal for laptop/notebook computer and PDA applications. The **SP3238E** includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown.

The **Auto-Online** feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1 $\mu$ A.

### SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Auto-Online Circuitry	TTL 3-State	No. of Pins
<b>SP3221E</b>	+3.0V to +5.5V	1	1	4 capacitors	YES	YES	16
<b>SP3223E</b>	+3.0V to +5.5V	2	2	4 capacitors	YES	YES	20
<b>SP3243E</b>	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28
<b>SP3238E</b>	+3.0V to +5.5V	5	3	4 capacitors	YES	YES	28

**Applicable U.S. Patents - 5,306,954; and other patents pending.**

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$ .....-0.3V to +6.0V  
 $V+$  (NOTE 1).....-0.3V to +7.0V  
 $V-$  (NOTE 1).....+0.3V to -7.0V  
 $V+ + |V-|$  (NOTE 1).....+13V  
 $I_{CC}$  (DC  $V_{CC}$  or GND current).....+100mA

### Input Voltages

$TxIN$ ,  $\overline{ONLINE}$ ,  
 SHUTDOWN,  $\overline{EN}$  .....-0.3V to +6.0V  
 $RxIN$ .....+15V

### Output Voltages

$TxOUT$ .....+15V  
 $RxOUT$ , STATUS.....-0.3V to ( $V_{CC} + 0.3V$ )

### Short-Circuit Duration

$TxOUT$ .....Continuous  
 Storage Temperature.....-65°C to +150°C

## Power Dissipation per package

28-pin SSOP (derate 11.2mW/°C above +70°C).....900mW  
 28-pin TSSOP (derate 13.2mW/°C above +70°C)....1100mW

**NOTE 1:**  $V+$  and  $V-$  can have maximum magnitudes of 7V, but their absolute difference cannot exceed 15V.

## SPECIFICATIONS

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to +5.5V with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ .  
 Typical values apply at  $V_{CC} = +3.3V$  or +5.0V and  $T_{AMB} = 25^{\circ}C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>DC CHARACTERISTICS</b>					
Supply Current, <i>Auto-Online</i>		1.0	10	$\mu A$	All $RxIN$ open, $\overline{ONLINE} = GND$ , SHUTDOWN = $V_{CC}$
Supply Current, Shutdown		1.0	10	$\mu A$	SHUTDOWN = GND
Supply Current, <i>Auto-Online</i> Disabled		0.4	2.0	mA	$\overline{ONLINE} = \overline{SHUTDOWN} = V_{CC}$ , no load
<b>LOGIC INPUTS AND RECEIVER OUTPUTS</b>					
Input Logic Threshold LOW HIGH	2.4		0.8	V	$V_{CC} = +3.3V$ or +5.0V, $TxIN$ $\overline{ONLINE}$ , SHUTDOWN
Input Leakage Current		$\pm 0.01$	$\pm 1.0$	$\mu A$	$TxIN$ , $\overline{ONLINE}$ , SHUTDOWN $T_{AMB} = 25^{\circ}C$
Output Leakage Current		$\pm 0.05$	$\pm 10$	$\mu A$	Receivers Disabled
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6mA$
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = 1.0mA$

## SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+5.5V$  with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ .  
Typical values apply at  $V_{CC} = +3.3V$  or  $+5.0V$  and  $T_{AMB} = 25^{\circ}C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>DRIVER OUTPUTS</b>					
Output Voltage Swing	$\pm 5.0$	$\pm 5.4$		V	All driver outputs loaded with $3K\Omega$ to GND
Output Resistance	300			$\Omega$	$V_{CC} = V_{+} = V_{-} = 0V$ , $V_{OUT} = \pm 2V$
Output Short-Circuit Current		$\pm 35$ $\pm 70$	$\pm 100$ TBD	mA	$V_{OUT} = GND$ $V_{OUT} = \pm 15V$
Output Leakage Current			$\pm 25$	$\mu A$	$V_{CC} = 0V$ or $3.0V$ to $5.5V$ , $V_{OUT} = \pm 15V$ , Drivers disabled
<b>RECEIVER INPUTS</b>					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	$V_{CC} = 3.3V$
Input Threshold LOW	0.8	1.5		V	$V_{CC} = 5.0V$
Input Threshold HIGH		1.5	2.4	V	$V_{CC} = 3.3V$
Input Threshold HIGH		1.8	2.4	V	$V_{CC} = 5.0V$
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	$k\Omega$	
<b>Auto-Online CIRCUITRY CHARACTERISTICS (ONLINE = GND, SHUTDOWN = <math>V_{CC}</math>)</b>					
STATUS Output Voltage LOW			0.4	V	$I_{OUT} = 1.6mA$
STATUS Output Voltage HIGH	$V_{CC} - 0.6$			V	$I_{OUT} = -1.0mA$
Receiver Threshold to Drivers Enabled ( $t_{ONLINE}$ )		200		$\mu S$	Figure 15
Receiver Positive or Negative Threshold to STATUS HIGH ( $t_{STSH}$ )		0.5		$\mu S$	Figure 15
Receiver Positive or Negative Threshold to STATUS LOW ( $t_{STSL}$ )		20		$\mu S$	Figure 15

## SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for  $V_{CC} = +3.0V$  to  $+5.5V$  with  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ .  
Typical values apply at  $V_{CC} = +3.3V$  or  $+5.0V$  and  $T_{AMB} = 25^{\circ}C$ .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>TIMING CHARACTERISTICS</b>					
Maximum Data Rate	250			kbps	$R_L = 3k\Omega$ , $C_L = 1000pF$ , one driver active
Receiver Propagation Delay $t_{PHL}$ $t_{PLH}$		0.15 0.15		$\mu s$	Receiver input to Receiver output, $C_L = 150pF$
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100	500	ns	$ t_{PHL} - t_{PLH} $ , $T_{AMB} = 25^{\circ}C$
Receiver Skew		200	1000	ns	$ t_{PHL} - t_{PLH} $
Transition-Region Slew Rate			30	V/ $\mu s$	$V_{CC} = 3.3V$ , $R_L = 3k\Omega$ , $T_{AMB} = 25^{\circ}C$ , measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for  $V_{CC} = +3.3V$ , 235Kbps data rate, all drivers loaded with  $3k\Omega$ ,  $0.1\mu F$  charge pump capacitors, and  $T_{AMB} = +25^{\circ}C$ .

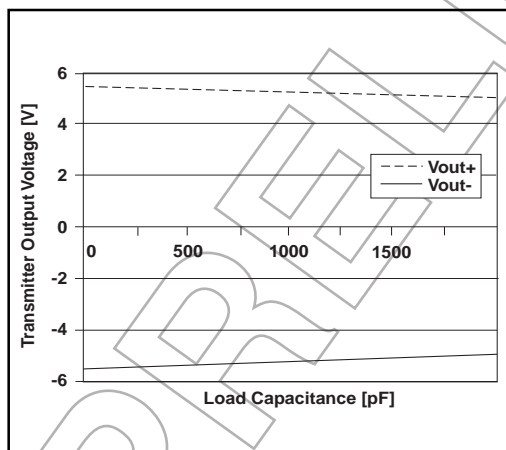


Figure 1. Transmitter Output Voltage VS. Load Capacitance

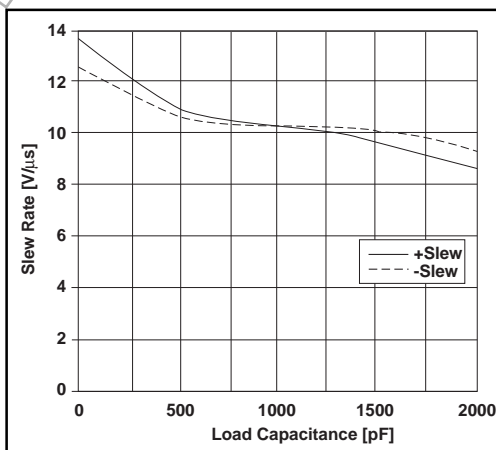


Figure 2. Slew Rate VS. Load Capacitance

NAME	FUNCTION	PIN NO.
C2+	Positive terminal of the inverting charge-pump capacitor.	1
GND	Ground.	2
C2-	Negative terminal of the inverting charge-pump capacitor.	3
V-	Regulated -5.5V output generated by the charge pump.	4
T <sub>1</sub> OUT	RS-232 driver output.	5
T <sub>2</sub> OUT	RS-232 driver output.	6
T <sub>3</sub> OUT	RS-232 driver output.	7
R <sub>1</sub> IN	RS-232 receiver input.	8
R <sub>2</sub> IN	RS-232 receiver input.	9
T <sub>4</sub> OUT	RS-232 driver output.	10
R <sub>3</sub> IN	RS-232 receiver input.	11
T <sub>5</sub> OUT	RS-232 driver output.	12
ONLINE	Apply logic HIGH to override <i>Auto-Online</i> circuitry keeping drivers active (SHUTDOWN must also be logic HIGH, refer to Table 2).	13
SHUTDOWN	Apply logic LOW to shut down drivers and charge pump. This overrides all <i>Auto-Online</i> circuitry and ONLINE (refer to Table 2).	14
STATUS	TTL/CMOS Output indicating online and shutdown status.	15
R <sub>1</sub> OUT	Non-inverting receiver-1 output, active in shutdown.	16
T <sub>5</sub> IN	TTL/CMOS driver input.	17
R <sub>3</sub> OUT	TTL/CMOS receiver output.	18
T <sub>4</sub> IN	TTL/CMOS driver input.	19
R <sub>2</sub> OUT	TTL/CMOS receiver output.	20
R <sub>1</sub> OUT	TTL/CMOS receiver output.	21
T <sub>3</sub> IN	TTL/CMOS driver input.	22
T <sub>2</sub> IN	TTL/CMOS driver input.	23
T <sub>1</sub> IN	TTL/CMOS driver input.	24
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	25
V <sub>CC</sub>	+3.0V to +5.5V supply voltage.	26
V+	Regulated +5.5V output generated by the charge pump.	27
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	28

**Table 1. Device Pin Description**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted, the following performance characteristics apply for  $V_{CC} = +3.3V$ , 235kbps data rate, all drivers loaded with  $3k\Omega$ ,  $0.1\mu F$  charge pump capacitors, and  $T_{AMB} = +25^{\circ}C$ .

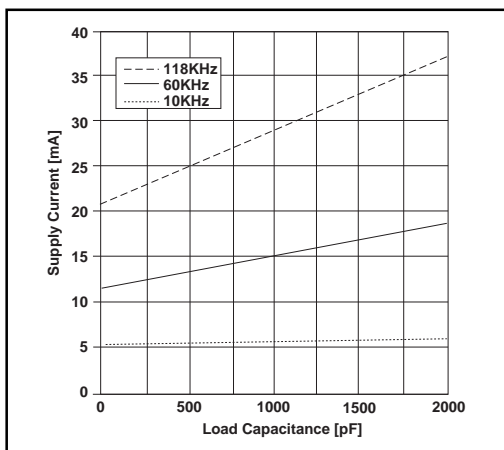


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data

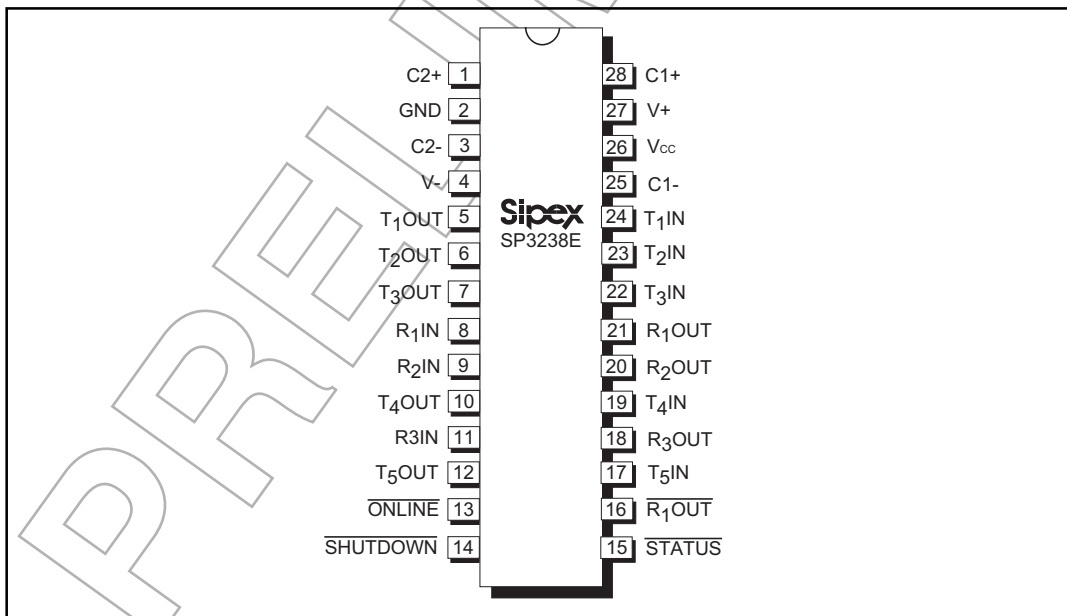


Figure 4. SP3238E Pinout Configuration

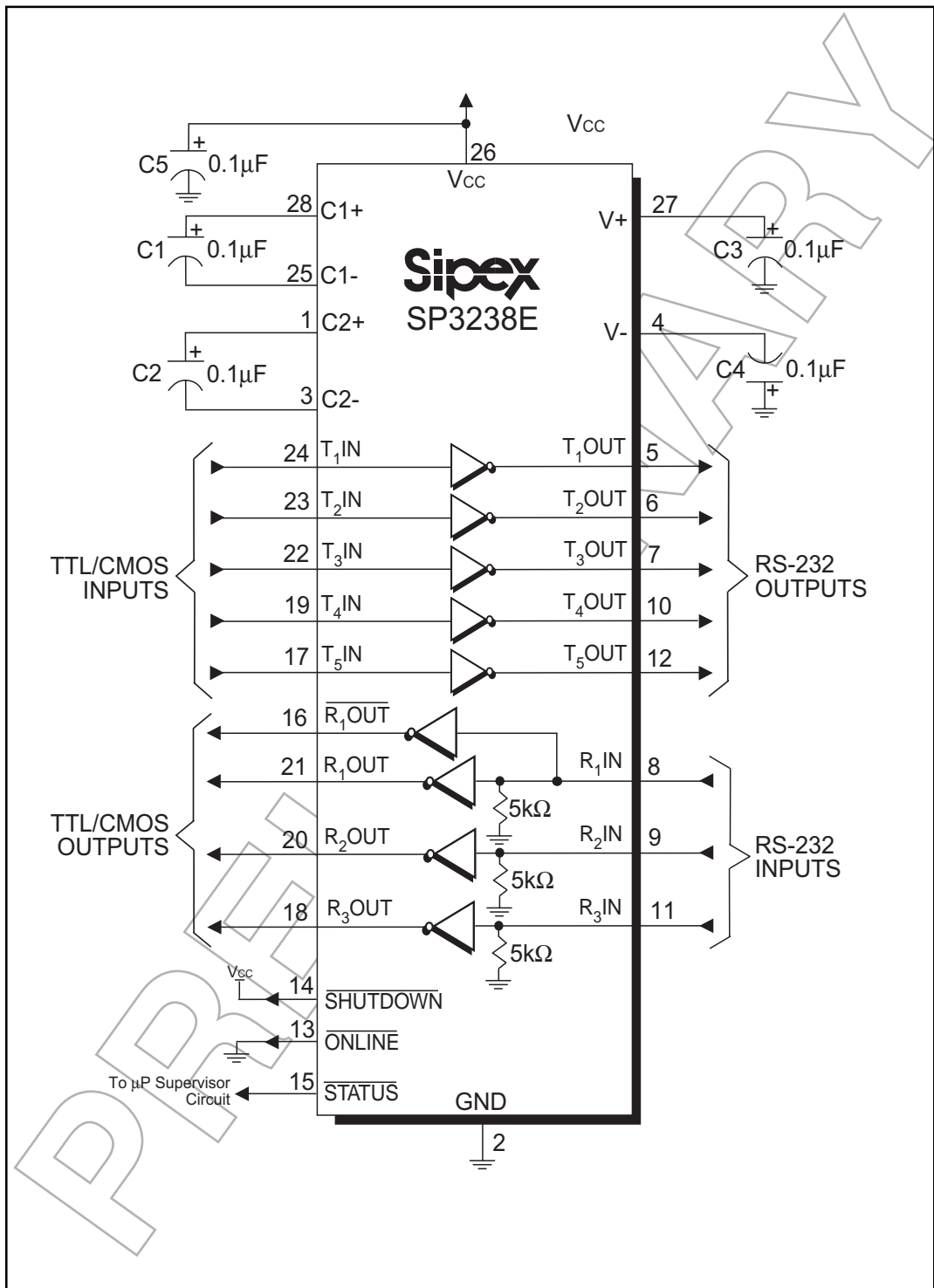
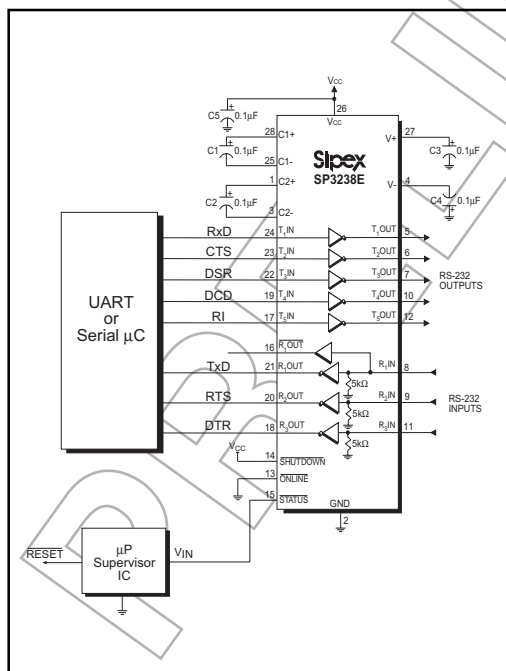


Figure 5. SP3238E Typical Operating Circuit

## DESCRIPTION

The **SP3238E** device meets the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3238E** device features **Sipex's** proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates  $\pm 5.5\text{V}$  RS-232 voltage levels from a single  $+3.0\text{V}$  to  $+5.5\text{V}$  power supply. The **SP3238E** device can operate at a typical data rate of 250kbps fully loaded.

The **SP3238E** is a 5-driver/3-receiver device, ideal for portable or hand-held applications. The **SP3238E** includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where  $V_{CC}$  may be disconnected.



**Figure 6. Interface Circuitry Controlled by Microprocessor Supervisory Circuit**

The **SP3238E** device is an ideal choice for power sensitive designs. The **SP3238E** device features **Auto-Online** circuitry which reduces the power supply drain to a  $1\mu\text{A}$  supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

## THEORY OF OPERATION

The **SP3238E** device is made up of four basic circuit blocks: 1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and 4. **Auto-Online** circuitry.

### Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to  $5.0\text{V}$  EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is  $\pm 5.4\text{V}$  with no load and  $\pm 5\text{V}$  minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions.

The drivers typically can operate at a data rate of 250kbps. The drivers can guarantee a data rate of 120kbps fully loaded with  $3\text{k}\Omega$  in parallel with  $1000\text{pF}$ , ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of  $30\text{V}/\mu\text{s}$  in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

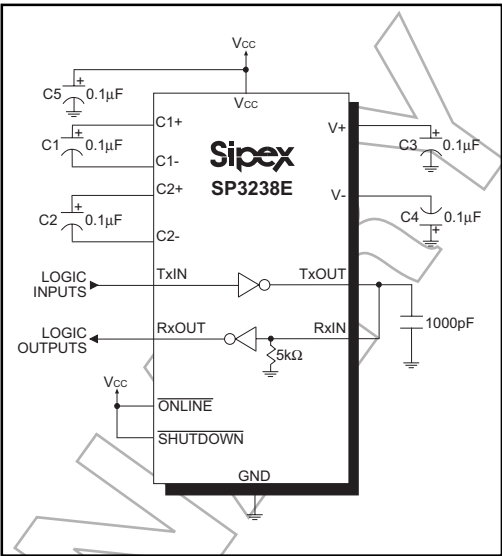


The **SP3238E** drivers can maintain high data rates up to 250kbps fully loaded. *Figure 7* shows a loopback test circuit used to test the RS-232 Drivers. *Figure 8* shows the test results of the loopback circuit with all three drivers active at 120kbps with typical RS-232 loads in parallel with 1000pF capacitors. *Figure 9* shows the test results where one driver was active at 250kbps and all three drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 120kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

### Receivers

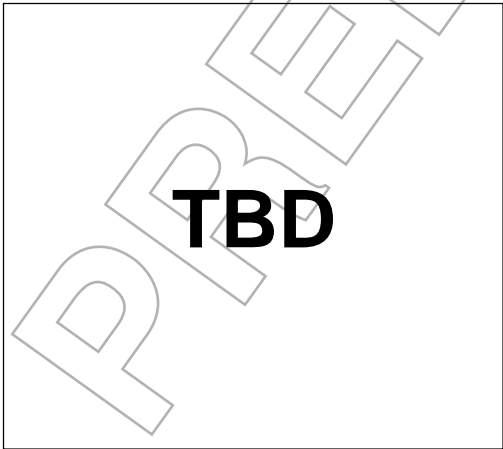
The receivers convert  $\pm 5.0V$  EIA/TIA-232 levels to TTL or CMOS logic output levels. All receivers have an inverting output that can be disabled by using the  $\overline{EN}$  pin.

Receivers are active when the *Auto-Online* circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100 $\mu s$  or when SHUTDOWN is enabled, the device goes into a standby mode where the circuit draws 1 $\mu A$ . The truth table logic of the driver and receiver outputs can be found in *Table 2*.

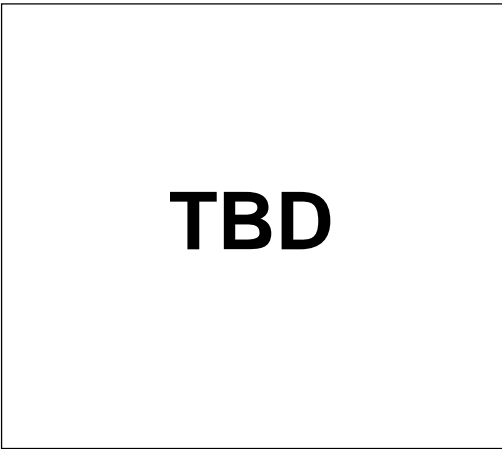


**Figure 7. Loopback Test Circuit for RS-232 Driver Data Transmission Rates**

The **SP3238E** includes an additional non-inverting receiver with an output  $R_I\overline{OUT}$ .  $R_I\overline{OUT}$  is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator (RI) from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.



**Figure 8. Loopback Test Circuit Result at 120kbps (All Drivers Fully Loaded)**



**Figure 9. Loopback Test Circuit result at 235kbps (All Drivers Fully Loaded)**

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

## Charge Pump

The charge pump is a **Sipex**—patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage ( $V_{CC}$ ) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

### Phase 1

—  $V_{SS}$  charge storage — During this phase of the clock cycle, the positive side of capacitors  $C_1$  and  $C_2$  are initially charged to  $V_{CC}$ .  $C_1^+$  is then switched to GND and the charge in  $C_1^-$  is transferred to  $C_2^-$ . Since  $C_2^+$  is connected to  $V_{CC}$ , the voltage potential across capacitor  $C_2$  is now 2 times  $V_{CC}$ .

### Phase 2

—  $V_{SS}$  transfer — Phase two of the clock connects the negative terminal of  $C_2$  to the  $V_{SS}$  storage capacitor and the positive terminal of  $C_2$  to GND. This transfers a negative generated voltage to  $C_3$ . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to  $C_3$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND.

### Phase 3

—  $V_{DD}$  charge storage — The third phase of the clock is identical to the first phase — the charge transferred in  $C_1$  produces  $-V_{CC}$  in the negative terminal of  $C_1$ , which is applied to the negative side of capacitor  $C_2$ . Since  $C_2^+$  is at  $V_{CC}$ , the voltage potential across  $C_2$  is 2 times  $V_{CC}$ .

### Phase 4

—  $V_{DD}$  transfer — The fourth phase of the clock connects the negative terminal of  $C_2$  to GND, and transfers this positive generated voltage across  $C_2$  to  $C_4$ , the  $V_{DD}$  storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to  $C_4$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both  $V^+$  and  $V^-$  are separately generated from  $V_{CC}$ , in a no-load condition  $V^+$  and  $V^-$  will be symmetrical. Older charge pump approaches that generate  $V^-$  from  $V^+$  will show a decrease in the magnitude of  $V^-$  compared to  $V^+$  due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 500kHz. The external capacitors can be as low as 0.1μF with a 16V breakdown voltage rating.

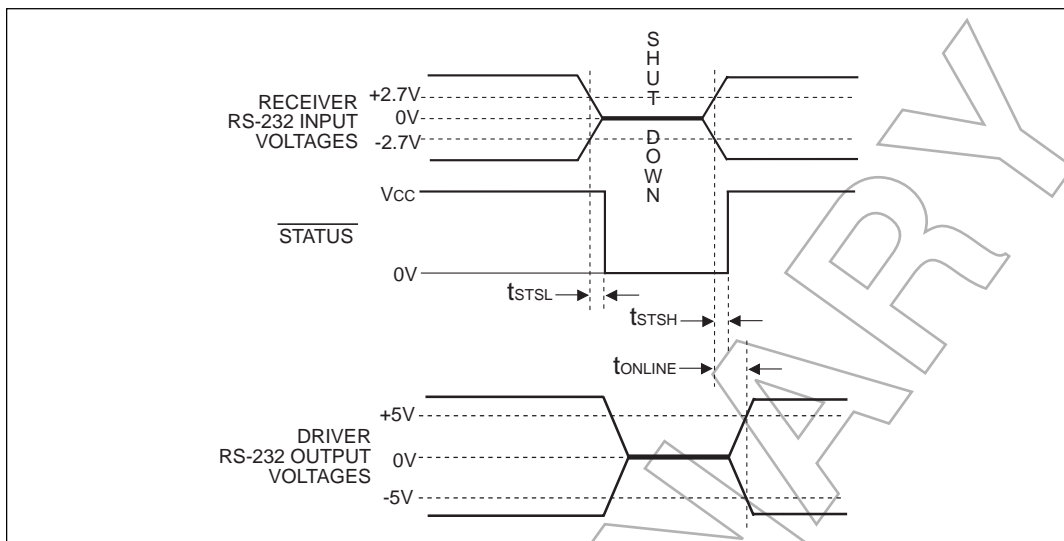


Figure 10. Auto-Online Timing Waveforms

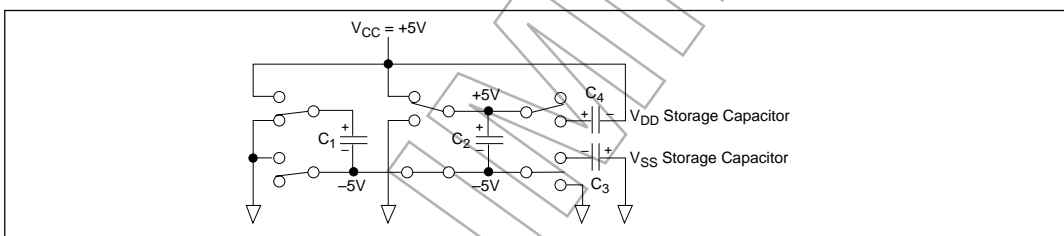


Figure 11. Charge Pump — Phase 1

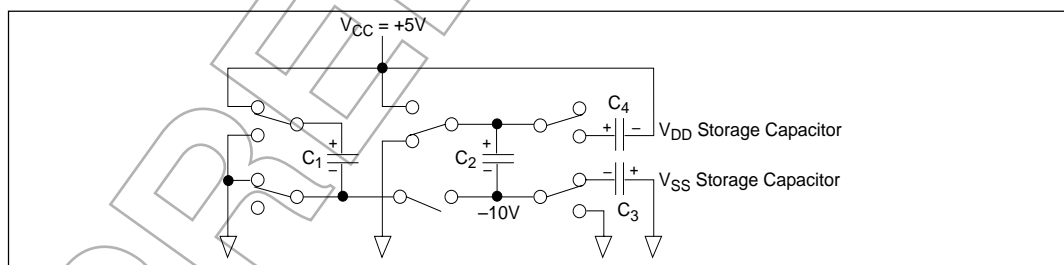


Figure 12. Charge Pump — Phase 2

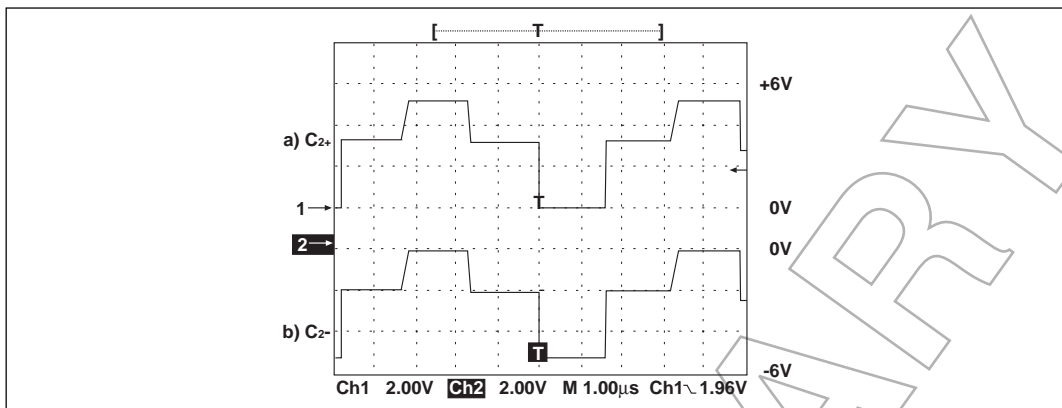


Figure 13. Charge Pump Waveforms

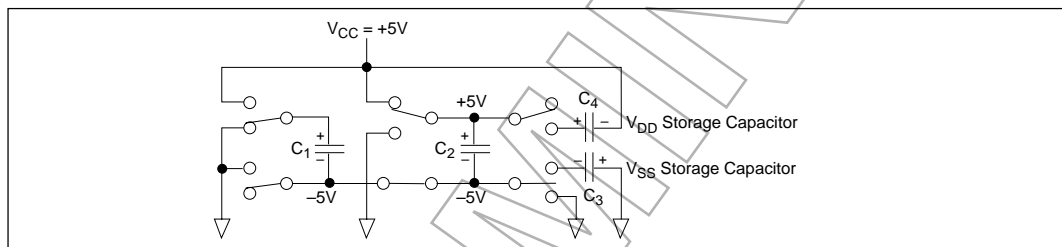


Figure 14. Charge Pump — Phase 3

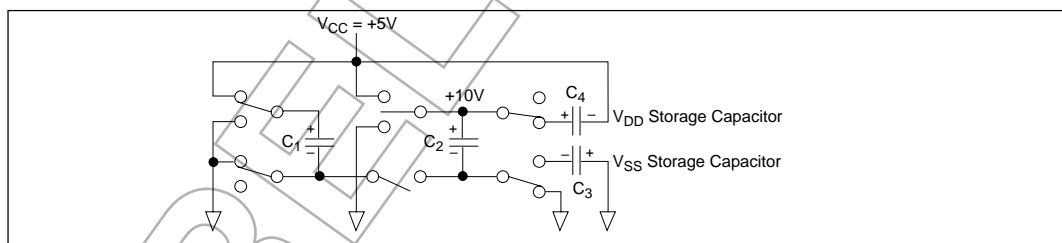
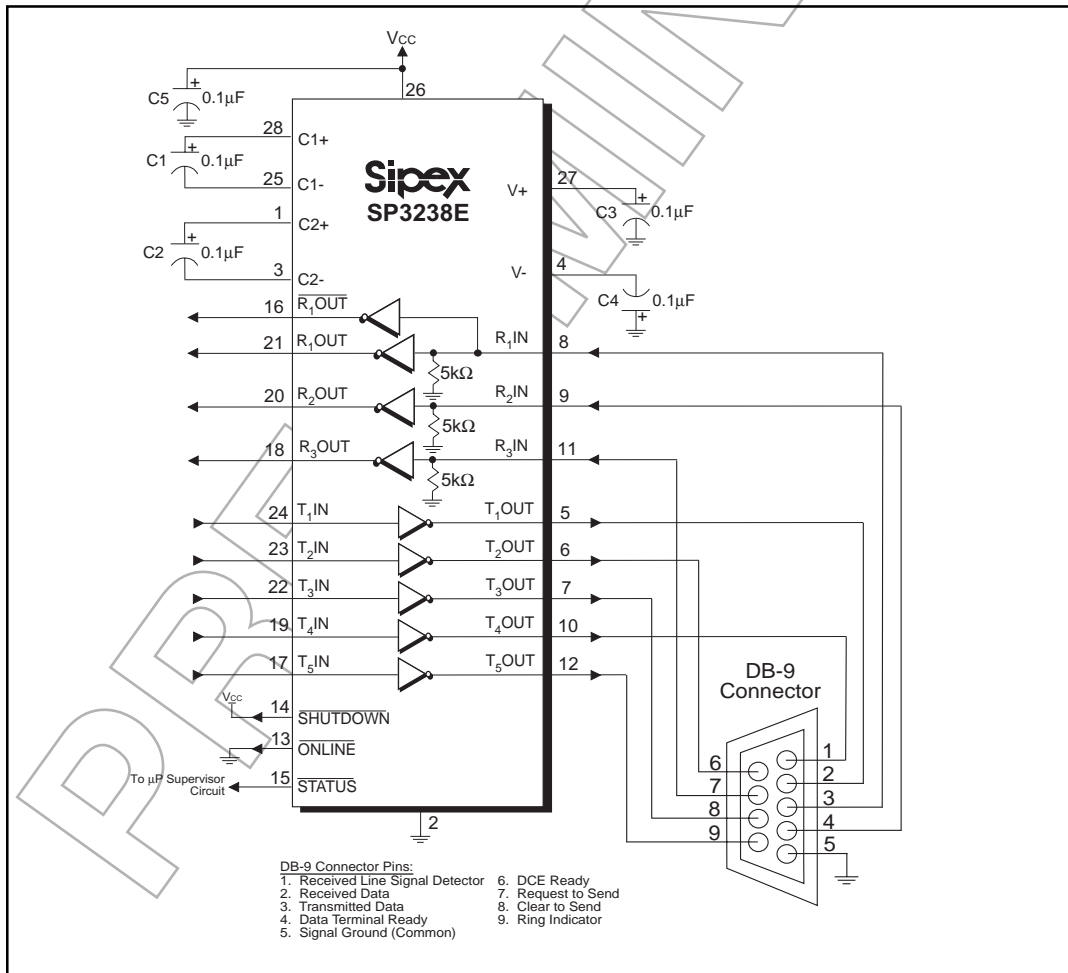


Figure 15. Charge Pump — Phase 4

# TBD

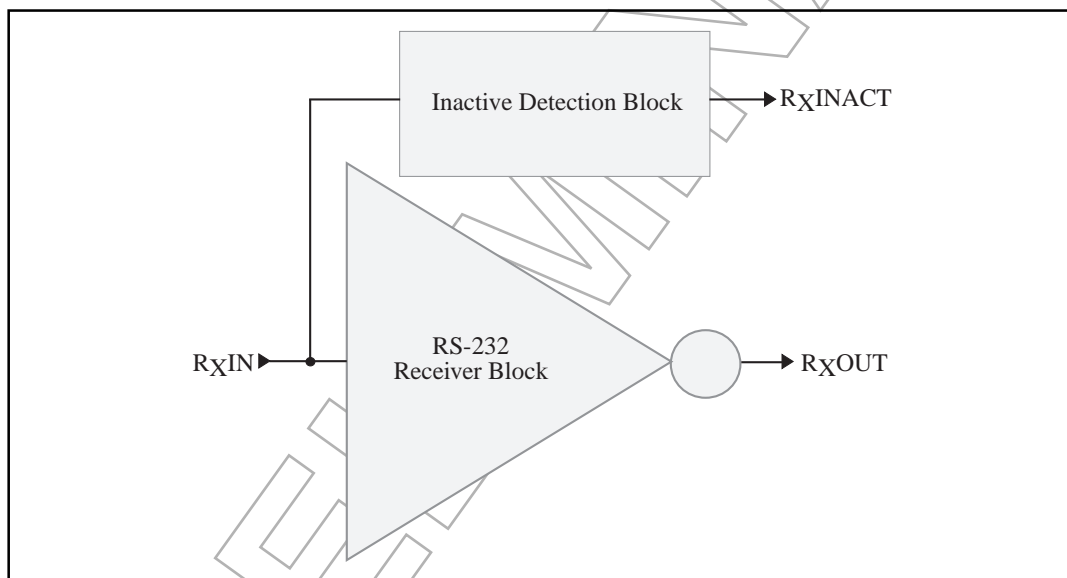
**Figure 16. Driver Output Voltages vs. Load Current per Transmitter**



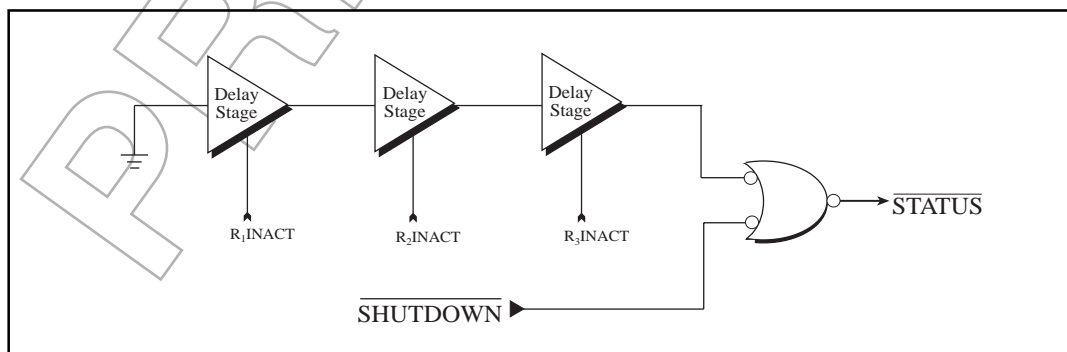
**Figure 17. Circuit for the connectivity of the SP3238E with a DB-9 connector**

SHUTDOWN INPUT	ONLINE INPUT	RS-232 SIGNAL AT RECEIVER INPUT	STATUS OUTPUT	T <sub>x</sub> OUT	R <sub>x</sub> OUT	R <sub>i</sub> OUT	TRANSCEIVER STATUS
HIGH	-	YES	HIGH	Active	Active	Active	Normal Operation
HIGH	HIGH	NO	LOW	Active	Active	Active	Normal Operation
HIGH	LOW	NO (<100μs)	LOW	Active	Active	Active	Normal Operation
HIGH	LOW	NO (>100μs)	LOW	High-Z	High-Z	Active	Shutdown ( <b>Auto-Online</b> )
LOW	-	YES	HIGH	High-Z	High-Z	Active	Shutdown
LOW	-	NO	LOW	High-Z	High-Z	Active	Shutdown

**Table 2. Auto-Online Logic**



**Figure 18. Stage I of Auto-Online Circuitry**



**Figure 19. Stage II of Auto-Online Circuitry**

## Auto-Online Circuitry

The **SP3238E** device has a patent pending **Auto-Online** circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers, and other portable systems.

The **SP3238E** device incorporates an **Auto-Online** circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the **Auto-Online** circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1 $\mu$ A. This function can also be externally controlled by the ONLINE pin. When this pin is tied to a logic LOW, the **Auto-Online** function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least  $\pm 3V$ , which are generated from the transmitters at the other end of the cable with a  $\pm 5V$  minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5k $\Omega$  resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When ONLINE is HIGH, the **Auto-Online** mode is disabled.

The **Auto-Online** circuit has two stages:

- 1) Inactive Detection
- 2) Accumulated Delay

The first stage, shown in *Figure 18*, detects an inactive input. A logic HIGH is asserted on R<sub>x</sub>INACT if the cable is disconnected or the external transmitters are disabled. Otherwise, R<sub>x</sub>INACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the **Auto-Online** circuitry, shown in *Figure 19*, processes all the receiver's R<sub>x</sub>INACT signals with an accumulated delay that disables the device to a 1 $\mu$ A supply current. The STATUS pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the SHUTDOWN pin is invoked. The typical accumulated delay is around 20 $\mu$ s.

When the drivers or internal charge pump are disabled, the supply current is reduced to 1 $\mu$ A. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The **Auto-Online** mode can be disabled by the SHUTDOWN pin. If this pin is a logic LOW, the **Auto-Online** function will not operate regardless of the logic state of the ONLINE pin. *Table 3* summarizes the logic of the **Auto-Online** operating modes. The truth table logic of the driver and receiver outputs can be found in *Table 2*.

The STATUS pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the **SP3238E** device is shut down, the charge pump is turned off. V<sup>+</sup> charge pump output decays to V<sub>CC</sub>, the V<sup>-</sup> output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V<sup>+</sup> and V<sup>-</sup> levels is typically 200 $\mu$ s.

For easy programming, the STATUS can be used to indicate DTR or a Ring Indicator signal. Tying ONLINE and SHUTDOWN together will bypass the **Auto-Online** circuitry so this connection acts like a shutdown input pin.

## ESD TOLERANCE

The **SP3238E** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least  $\pm 15\text{kV}$  without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC1000-4-2 Air-Discharge
- c) IEC1000-4-2 Direct Contact

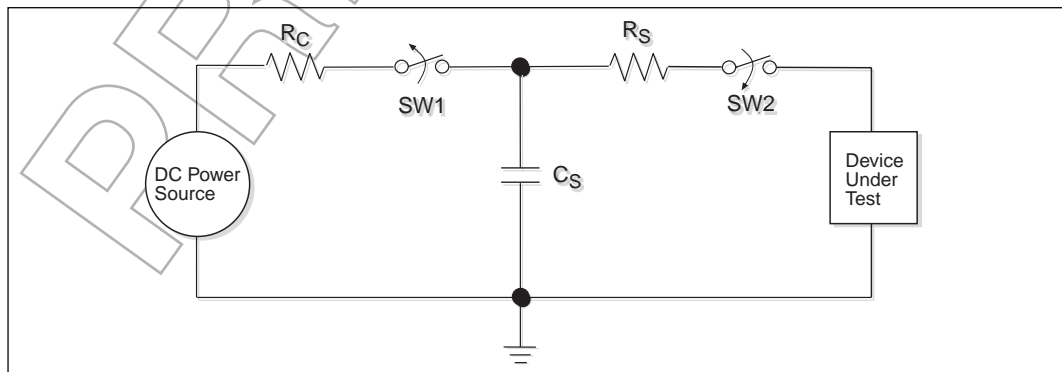
The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 20*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during

normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 21*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.



**Figure 20. ESD Test Circuit for Human Body Model**



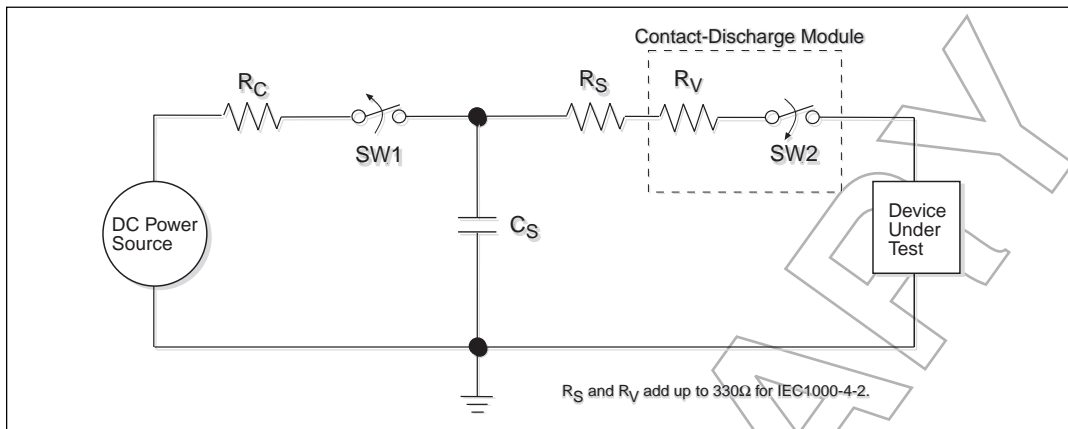


Figure 21. ESD Test Circuit for IEC1000-4-2

The circuit model in Figures 20 and 21 represent the typical ESD testing circuit used for all three methods. The  $C_S$  is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through  $R_S$ , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor ( $R_S$ ) and the source capacitor ( $C_S$ ) are 1.5kΩ an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor ( $R_S$ ) and the source capacitor ( $C_S$ ) are 330Ω an 150pF, respectively.

The higher  $C_S$  value and lower  $R_S$  value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

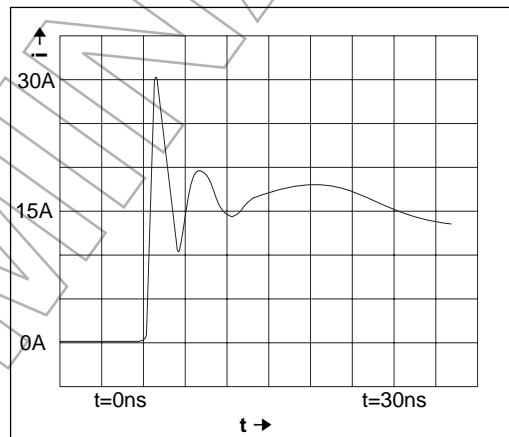
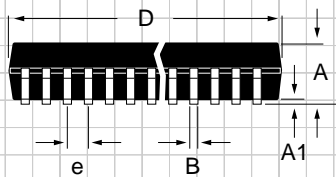
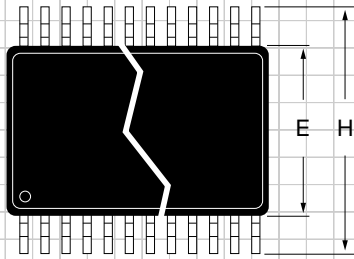


Figure 22. ESD Test Waveform for IEC1000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

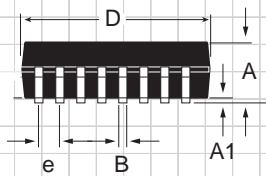
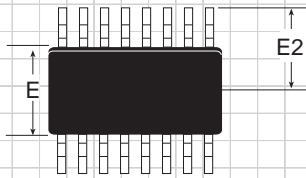
Table 3. Transceiver ESD Tolerance Levels

**PACKAGE: PLASTIC SHRINK  
SMALL OUTLINE  
(SSOP)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	28-PIN
A	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)
D	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)

**PACKAGE: PLASTIC THIN SMALL  
OUTLINE  
(TSSOP)**



DIMENSIONS in inches (mm) Minimum/Maximum	28-PIN
A	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)
D	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)
E2	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)

## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP3238ECA . . . . .	0°C to +70°C . . . . .	. 28-pin SSOP
SP3238ECY . . . . .	0°C to +70°C . . . . .	. 28-pin TSSOP
SP3238EEA . . . . .	-40°C to +85°C . . . . .	. 28-pin SSOP
SP3238EEY . . . . .	-40°C to +85°C . . . . .	. 28-pin TSSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.



SIGNAL PROCESSING EXCELLENCE

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