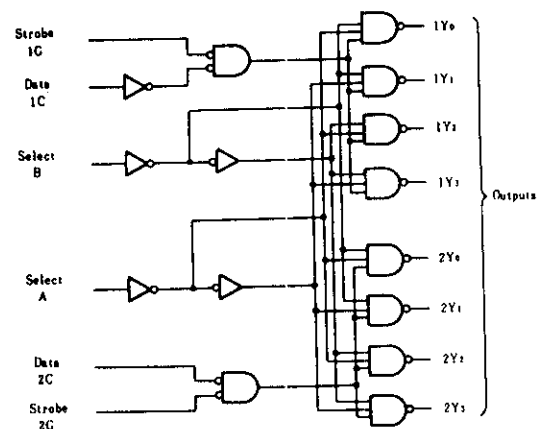


# HD74LS155 • Dual 2-line-to-4-line Decoders/Demultiplexers

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address input. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer with-out external gating.

## ■ BLOCK DIAGRAM



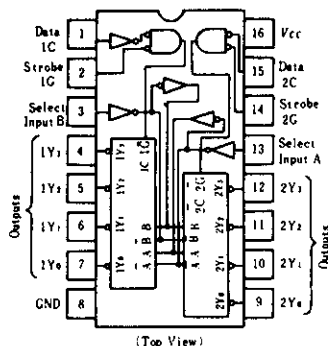
## ■ FUNCTION TABLE

● 2-line-to-4-line Decoder/1-line-to-4-line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data	1Y <sub>0</sub>	1Y <sub>1</sub>	1Y <sub>2</sub>	1Y <sub>3</sub>
B	A	1G	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data	2Y <sub>0</sub>	2Y <sub>1</sub>	2Y <sub>2</sub>	2Y <sub>3</sub>
B	A	2G	2C				
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

## ■ PIN ARRANGEMENT



● 3-line-to-8-line Decoder/1-line-to-8-line Demultiplexer

Inputs				Outputs							
Select			Strobe	Data							
C	B	A	G	2Y <sub>0</sub>	2Y <sub>1</sub>	2Y <sub>2</sub>	2Y <sub>3</sub>	1Y <sub>0</sub>	1Y <sub>1</sub>	1Y <sub>2</sub>	1Y <sub>3</sub>
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

- Notes) 1. C; input 1C and 2C connected together  
 2. G; inputs 1G and 2G connected together  
 3. H; high level, L; low level, X; irrelevant

## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	$V_{IH}$		2.0	—	—	V
	$V_{IL}$		—	—	0.8	V
Output voltage	$V_{OH}$	$V_{CC}=4.75\text{V}$ , $V_{IH}=2\text{V}$ , $V_{IL}=0.8\text{V}$ , $I_{OH}=-400\mu\text{A}$	2.7	—	—	V
	$V_{OL}$	$V_{CC}=4.75\text{V}$ , $V_{IH}=2\text{V}$ , $V_{IL}=0.8\text{V}$	$I_{OL}=4\text{mA}$	—	0.4	V
			$I_{OL}=8\text{mA}$	—	0.5	
Input current	$I_I$	$V_{CC}=5.25\text{V}$ , $V_I=7\text{V}$	—	—	0.1	mA
	$I_{IH}$	$V_{CC}=5.25\text{V}$ , $V_I=2.7\text{V}$	—	—	20	$\mu\text{A}$
	$I_{IL}$	$V_{CC}=5.25\text{V}$ , $V_I=0.4\text{V}$	—	—	-0.4	mA
Short-circuit output current	$I_{OS}$	$V_{CC}=5.25\text{V}$	-5	—	-42	mA
Supply current**	$I_{CC}$	$V_{CC}=5.25\text{V}$	—	6.1	10	mA
Input clamp voltage	$V_{IK}$	$V_{CC}=4.75\text{V}$ , $I_{IN}=-18\text{mA}$	—	—	-1.5	V

\*  $V_{CC}=5\text{V}$ ,  $T_a=25^\circ\text{C}$

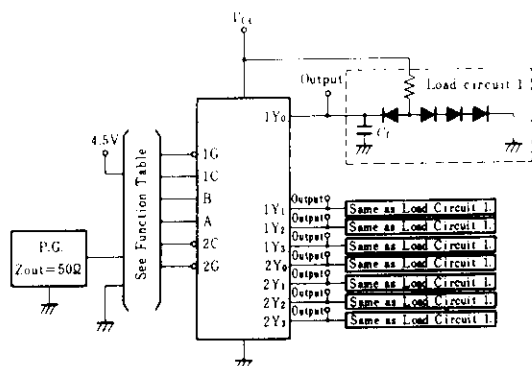
\*\*  $I_{CC}$  is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

## ■ SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}$ , $T_a=25^\circ\text{C}$ )

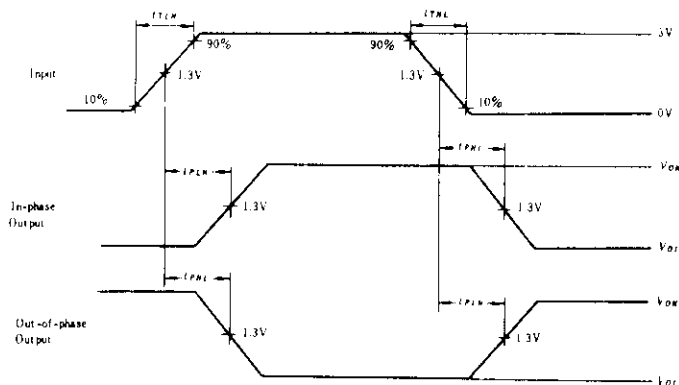
Item	Inputs	Output	Levels of logic	Test Conditions	min	typ	max	Unit
$t_{PLH}$	A, B, 2C	Y	2	$C_L = 15\text{pF}, R_I = 2\text{k}\Omega$	—	10	15	ns
$t_{PHL}$	1G or 2G				—	19	30	ns
$t_{PLH}$	A or B	Y	3		—	17	26	ns
$t_{PHL}$					—	19	30	ns
$t_{PLH}$	1C	Y	3		—	18	27	ns
$t_{PHL}$					—	18	27	ns

## ■ TESTING METHOD

### 1) Test Circuit

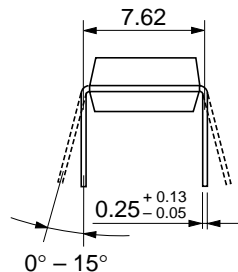
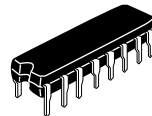
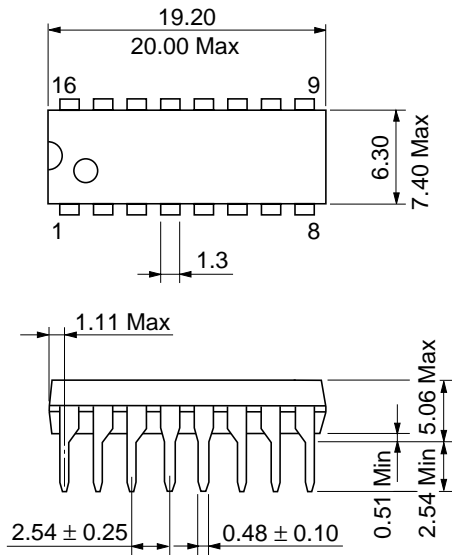


### Waveform

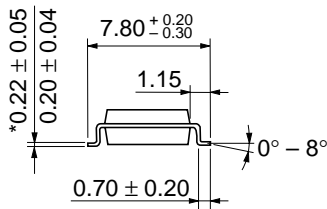
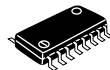
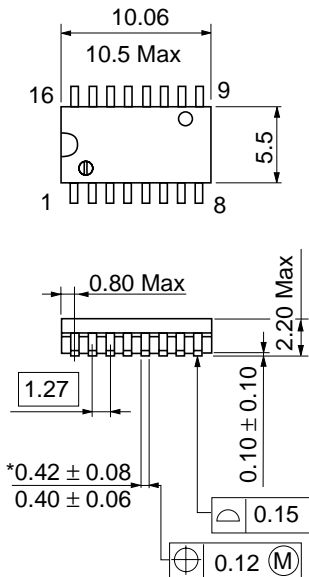


- Notes) 1. Input pulse;  $t_{TLH} \leq 15\text{ns}$ ,  $t_{THL} \leq 6\text{ns}$ ,  $PRR=1\text{MHz}$ , duty cycle=50%  
 2.  $C_L$  includes probe and jig capacitance.  
 3. All diodes are 1S2074 (H).

Unit: mm

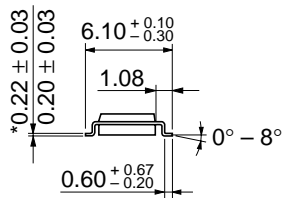
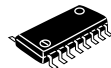
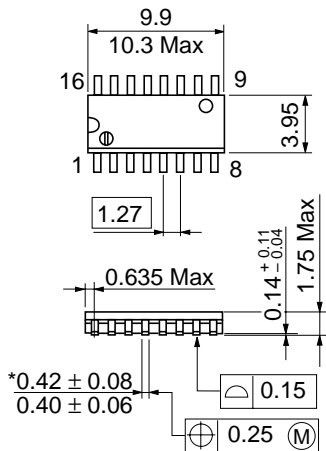


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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