Programmable Reference

FEATURES

- Guaranteed 0.4% Initial Voltage Tolerance
- 0.1Ω Typical Dynamic Output Impedance
- Fast Turn-On
- Sink Current Capability, 1mA to 100mA
- Low Reference Pin Current

APPLICATIONS

- Linear Regulators
- Adjustable Power Supplies
- Switching Power Supplies

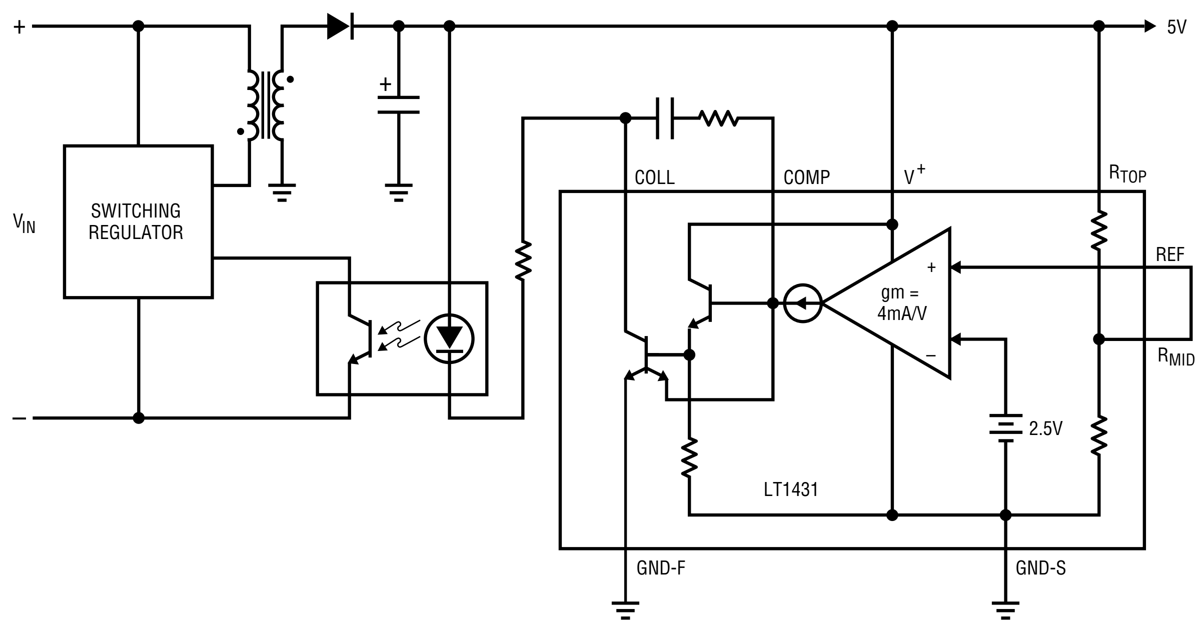
DESCRIPTION

The LT1431 is an adjustable shunt voltage regulator with 100mA sink capability, 0.4% initial reference voltage tolerance, and 0.3% typical temperature stability. On-chip divider resistors allow the LT1431 to be configured as a 5V shunt regulator, with 1% initial voltage tolerance and requiring no additional external components. By adding two external resistors, the output voltage may be set to any value between 2.5V and 36V. The nominal internal current limit of 100mA may be decreased by including one external resistor.

A simplified three pin version, the LT1431Z/IZ, is available for applications as an adjustable reference and is pin compatible with the TL431.

TYPICAL APPLICATION

Isolated 5V Regulator

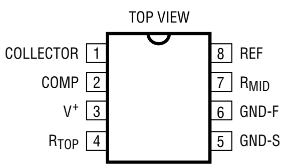
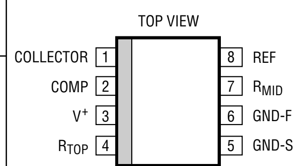
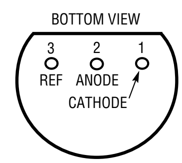


ABSOLUTE MAXIMUM RATINGS

V^+, $V_{COLLECTOR}$ 36V
V_{COMP}, R_{TOP}, R_{MID}, V_{REF} 6V
GND-F to GND-S 0.7V
Ambient Temperature Range
  LT1431M .... −55°C to 125°C
  LT1431I .... −40°C to 85°C
  LT1431C .... 0°C TO 70°C

JunctionTemperature Range
  LT1431M .... −55°C to 150°C
  LT1431I .... −40°C to 100°C
  LT1431C .... 0°C to 100°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER		ORDER PART NUMBER
	LT1431MJ8 LT1431CN8 LT1431IN8		LT1431CS8 LT1431IS8		LT1431CZ LT1431IZ
J8 PACKAGE 8-LEAD CERAMIC DIP; N8 PACKAGE 8-LEAD PLASTIC DIP $T_{J\,MAX}$ = 150°C, θ_{JA} = 100°C/W (J) $T_{J\,MAX}$ = 100°C, θ_{JA} = 130°C/W (N)		S8 PACKAGE 8-LEAD PLASTIC SOIC $T_{J\,MAX}$ = 100°C, θ_{JA} = 170°C/W	PART MARKING LT1431 LT1431I	Z PACKAGE 3-LEAD TO-92 PLASTIC $T_{J\,MAX}$ = 100°C, θ_{JA} = 160°C/W	

ELECTRICAL CHARACTERISTICS T_A = 25°C, I_K = 10mA, unless otherwise specified (Note 1).

SYMBOL	PARAMETER	CONDITIONS		LT1431M/I MIN	LT1431M/I TYP	LT1431M/I MAX	LT1431C MIN	LT1431C TYP	LT1431C MAX	UNITS
V_{REF}	Reference Voltage	V_{KA} = 5V, I_K = 2mA, (Note 2)	 ●	2.490 2.465	2.500	2.510 2.535	2.490 2.480	2.500	2.510 2.520	V V
$\Delta V_{REF}/\Delta T$	Reference Drift	V_{KA} = 5V, I_K = 2mA	●		50			30		ppm/°C
$\Delta V_{REF}/\Delta V_{KA}$	Voltage Ratio, Reference to Cathode (Open-Loop Gain)	I_K = 2mA, V_{KA} = 3V to 36V	●		0.2	0.5		0.2	0.5	mV/V
$\lvert I_{REF}\rvert$	Reference Input Current	V_{KA} = 5V, T_A = 25°C	 ●		0.2	1.0 1.5		0.2	1.0 1.2	μA μA
I_{MIN}	Minimum Operating Current	V_{KA} = V_{REF} to 36V			0.6	1.0		0.6	1.0	mA
$\lvert I_{OFF}\rvert$	Off-State Cathode Current	V_{KA} = 36V, V_{REF} = 0V	 ●			1 15			1 2	μA μA
$\lvert I_{LEAK}\rvert$	Off-State Collector Leakage Current	V_{COLL} = 36V, V^+ = 5V, V_{REF} = 2.4V	 ●			1 5			1 2	μA μA
$\lvert Z_{KA}\rvert$	Dynamic Impedance	V_{KA} = V_{REF}, I_K = 1mA to 100mA, f ≤ 1kHz				0.2			0.2	Ω
I_{LIM}	Collector Current Limit	V_{KA} = V_{REF} + 50mV	●	80		360	100		260	mA
	5V Reference Output	Internal Divider Used, I_K = 2mA		4.950	5.000	5.050	4.950	5.000	5.050	V

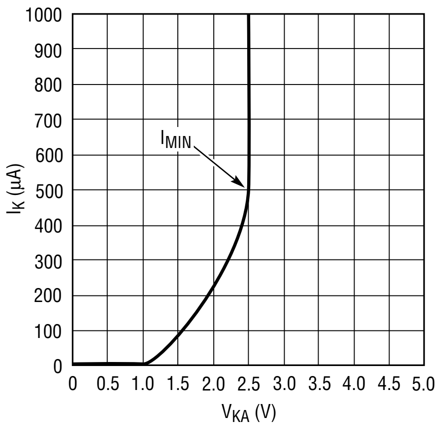
The ● denotes specifications which apply over the operating temperature range.

Note 1: V_{KA} is the cathode voltage of the LT1431CZ/IZ and corresponds to V^+ of the LT1431CN8/MJ8. I_K is the cathode current of the LT1431CZ/IZ and corresponds to $I(V^+) + I_{COLLECTOR}$ of the LT1431CN8/MJ8/IN8.

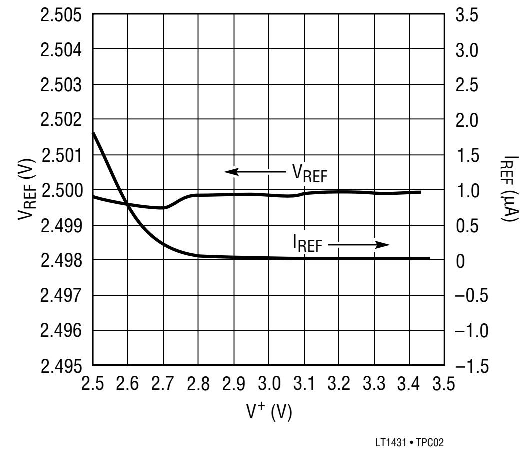
Note 2: The LT1431 has bias current cancellation which is effective only for $V_{KA} \geq 3V$. A slight (≈2mV) shift in reference voltage occurs when V_{KA} drops below 3V. For this reason, these tests are not performed at $V_{KA} = V_{REF}$.

TYPICAL PERFORMANCE CHARACTERISTICS

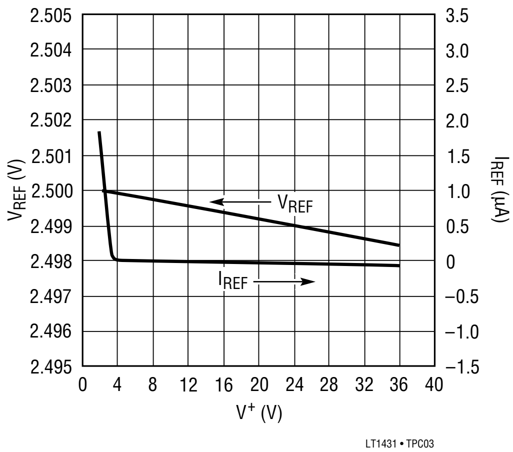
2.5V Reference I_K vs V_{KA}



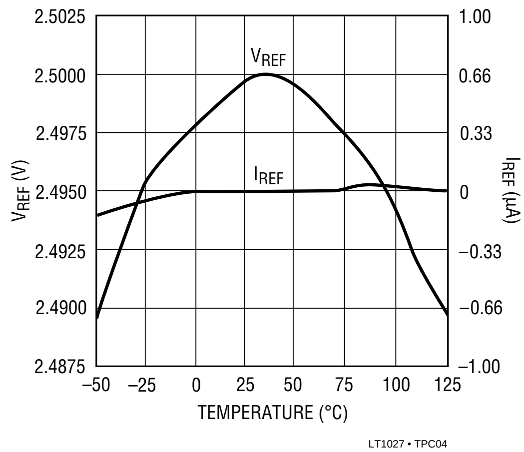
V_{REF} and I_{REF} vs V^+



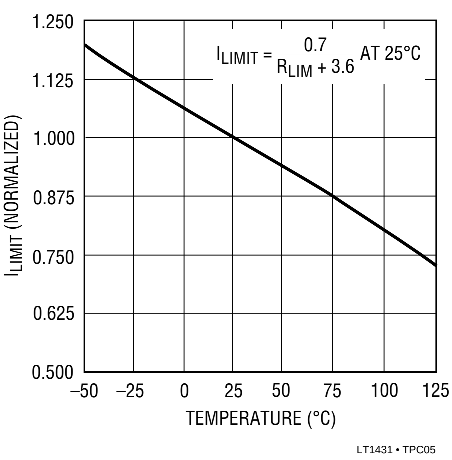
V_{REF} and I_{REF} vs V^+



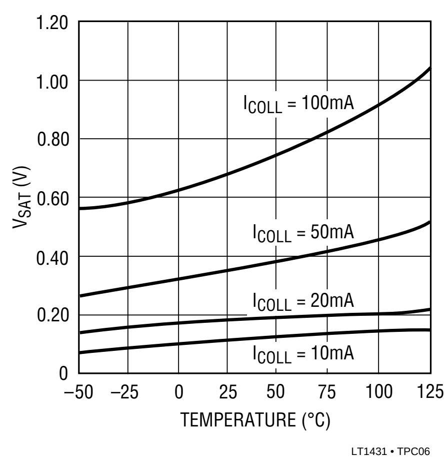
V_{REF} and I_{REF} vs Temperature



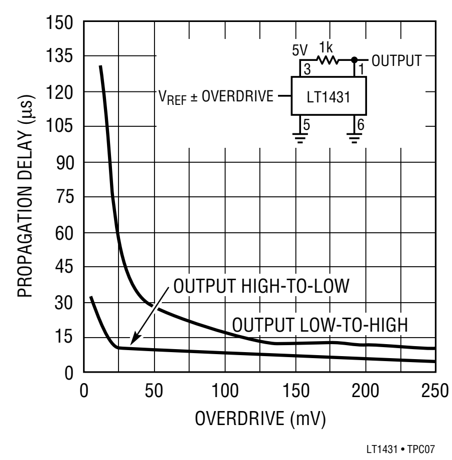
I_{LIMIT} vs Temperature with External Resistor



COLLECTOR V_{SAT} vs Temperature vs Current

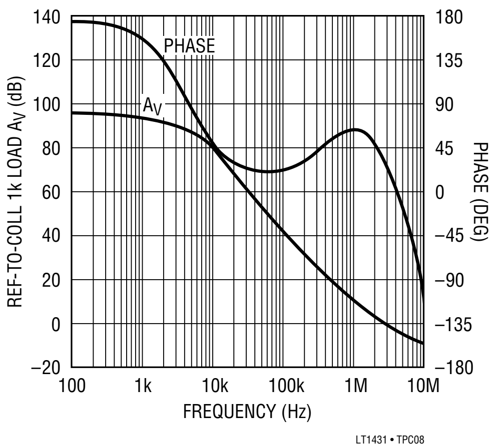


Propagation Delay vs Overdrive

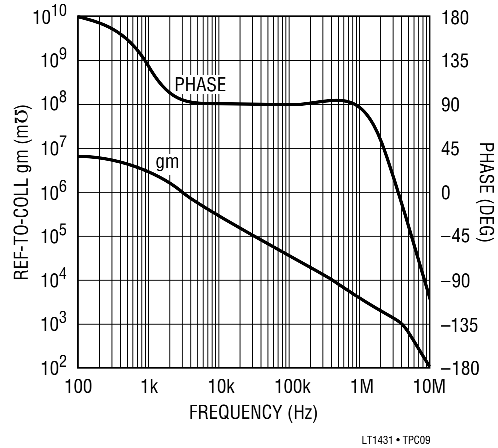


TYPICAL PERFORMANCE CHARACTERISTICS

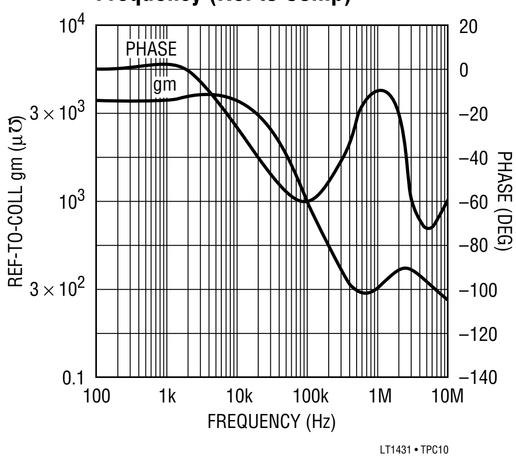
Voltage Gain and Phase vs Frequency



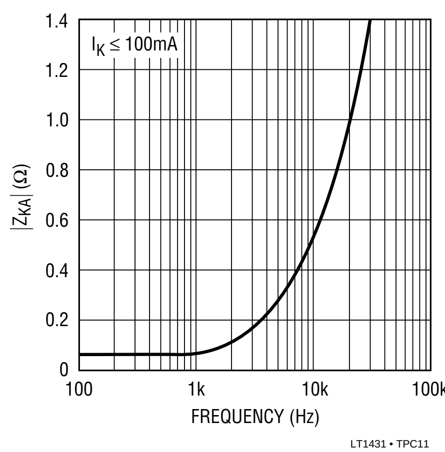
Transconductance and Phase vs Frequency (REF to COLL)



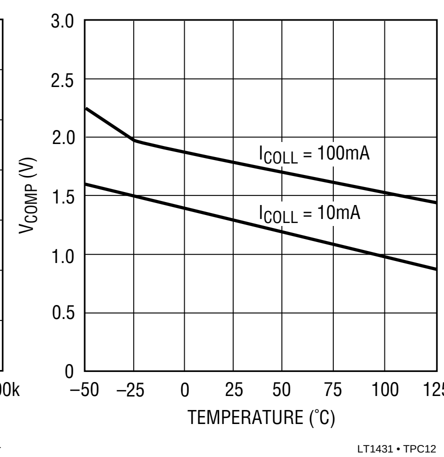
Transconductance and Phase vs Frequency (Ref to Comp)



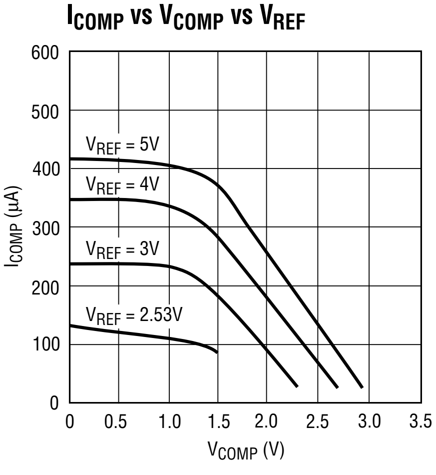
Dynamic Impedance vs Frequency



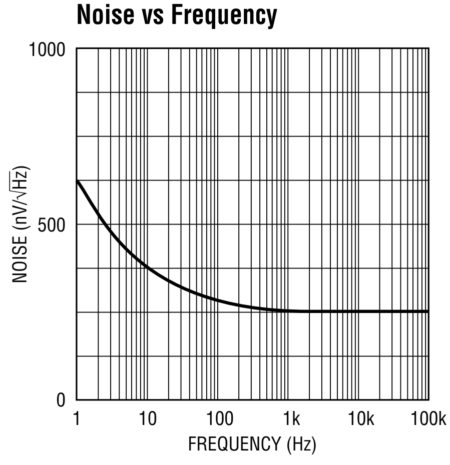
V_{COMP} vs Temperature vs I_{COLL}



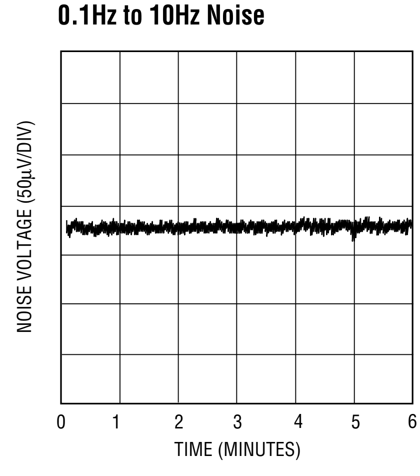
I_{COMP} vs V_{COMP} vs V_{REF}



Noise vs Frequency



0.1Hz to 10Hz Noise



PIN FUNCTIONS

COLL (Pin 1): Open collector of the output transistor. The maximum pin voltage is 26V. The saturation voltage at 100mA is approximately 1V.

COMP (Pin 2): Base of the driver for the output transistor. This pin allows additional compensation for complex feedback systems and shutdown of the regulator. It must be left open if unused.

V^+ (Pin 3): Bias voltage for the entire shunt regulator. The maximum input voltage is 36V and the minimum to operate is equal to V_{REF} (2.5V). The quiescent current is typically 0.6mA.

R_{TOP} (Pin 4): Top of the on-chip 5k-5k resistive divider that guarantees 1% accuracy of operation as a 5V shunt regulator with no external trim. The pin is tied to COLL for self-contained 5V operation. It may be left open if unused. See note on parasitic diodes below.

GND-S (Pin 5): Ground reference for the on-chip resistive divider and shunt regulator circuitry except for the output transistor. This pin allows external current limit of the output transistor with one resistor between GND-F (force) and GND-S (sense).

GND-F (Pin 6): Emitter of the output transistor and substrate connection for the die.

R_{MID} (Pin 7): Middle of the on-chip resistive divider string between R_{TOP} and GND-S. The pin is tied to REF for self-contained 5V operation. It may be left open if unused.

REF (Pin 8): Control pin of the shunt regulator with a 2.5V threshold. If $V^+ > 3V$, input bias current cancellation reduces I_B to 0.2μA typical.

COMP, R_{TOP}, R_{MID}, and REF have static discharge protection circuits that must not be activated on a continuous basis. Therefore, the absolute maximum DC voltage on these pins is 6V, well beyond the normal operating conditions.

As with all bipolar ICs, the LT1431 contains parasitic diodes which must not be forward biased or else anomalous behavior will result. Pin conditions to be avoided are R_{TOP} below R_{MID} in voltage and any pin below GND-F in voltage (except for GND-S).

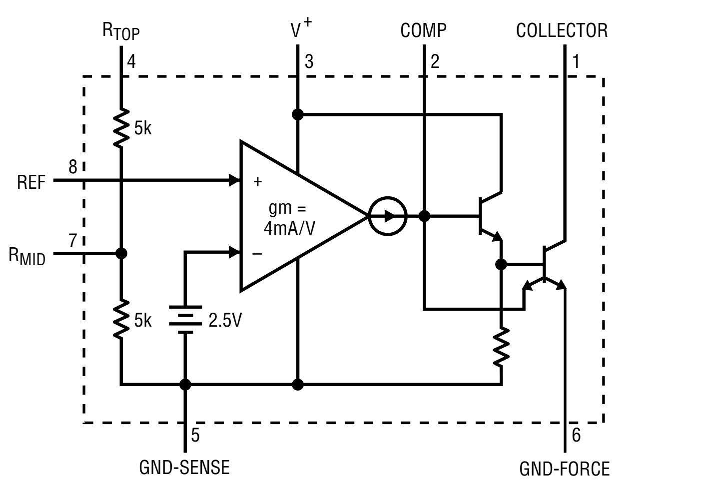
The following pin definitions apply to the Z package.

CATHODE (Pin 1): Corresponds to COLL and V^+ tied together.

ANODE (Pin 2): Corresponds to GND-S and GND-F tied together.

REF (Pin 3): Corresponds to REF.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Frequency Compensation

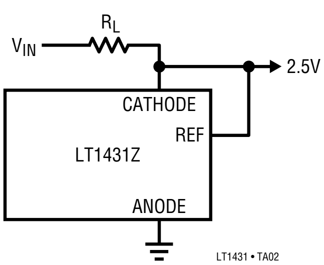
As a shunt regulator, the LT1431 is stable for all capacitive loads on the COLL pin. Capacitive loading between 0.01µF and 18µF causes reduced phase margin with some ringing under transient conditions. Output capacitors should not be used arbitrarily because output noise is not necessarily reduced.

Excess capacitance on the REF pin can introduce enough phase shift to induce oscillation when configured as a reference >2.5V. This can be compensated with capacitance between COLL and REF (phase lead). More complicated feedback loops may require shaping of the frequency response of the LT1431 with dominant pole or pole-zero compensation. This can be accomplished with a capacitor or series resistor and capacitor between COLL and COMP.

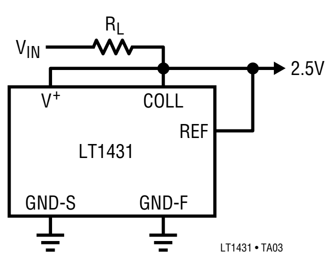
The compensation schemes mentioned above use voltage feedback to stabilize the circuits. There must be voltage gain at the COLL pin for them to be effective, so the COLL pin must see a reasonable AC impedance. Capacitive loading of the COLL pin reduces the AC impedance, voltage gain, and frequency response, thereby decreasing the effectiveness of the compensation schemes, but also decreasing their necessity.

TYPICAL APPLICATIONS

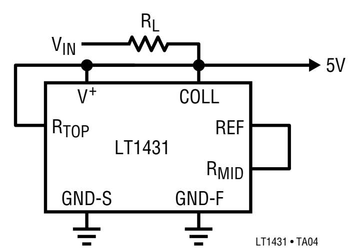
2.5V Reference 3-Pin Package



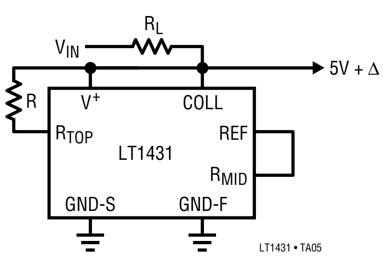
2.5V Reference 8-Pin Package



5V Reference

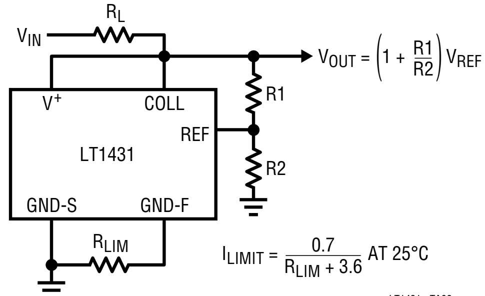


Increasing 5V Reference



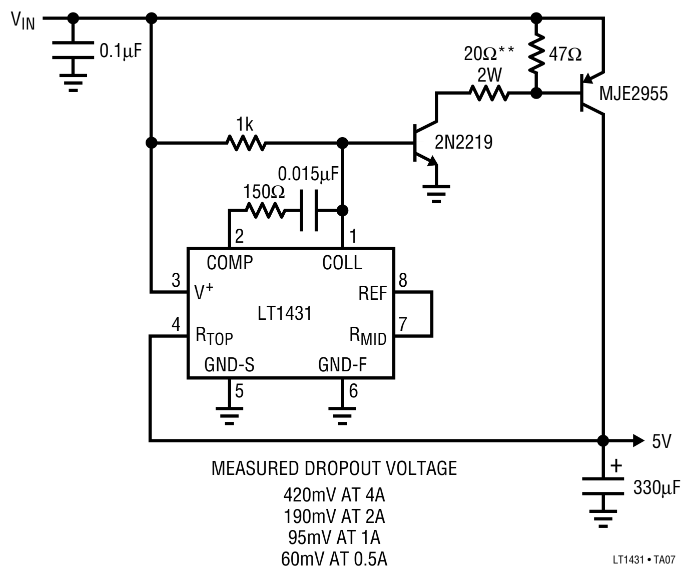
$\Delta = R \times (0.5mA)$ ±25% PROCESS TOLERANCE
$\Delta \le 500mV$

Programmable Reference with Adjustable Current Limit



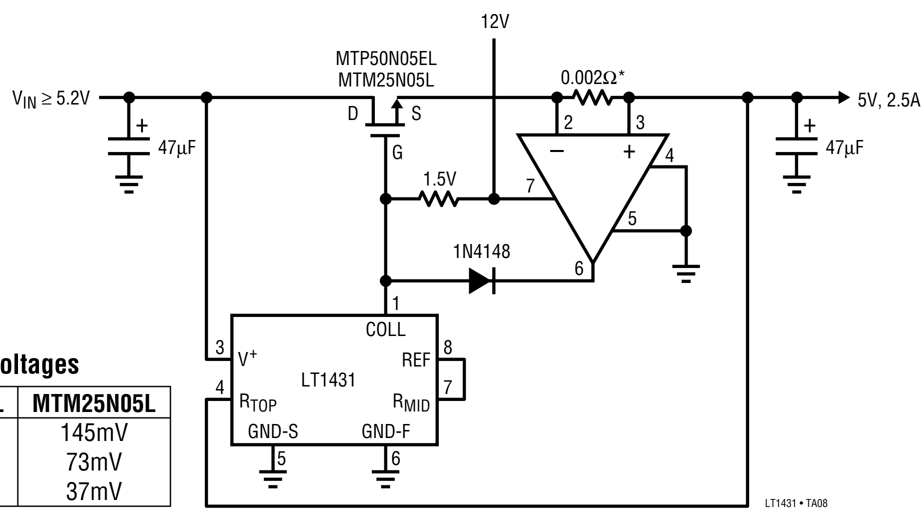
TYPICAL APPLICATIONS

PNP Low Dropout 5V Regulator*



*NO SHORT-CIRCUIT PROTECTION
**MAY BE INCREASED AT LOWER WATTAGE FOR LOWER OUTPUT CURRENTS

FET Low Dropout 5V Regulator with Current Limit



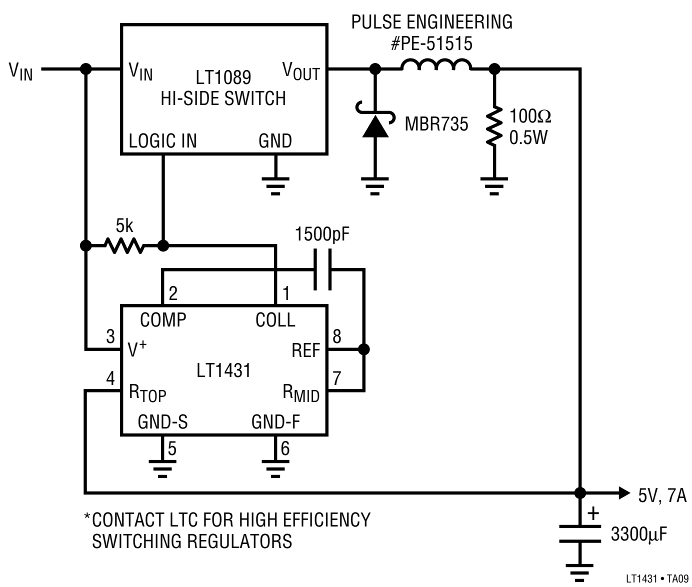
Measured Dropout Voltages

I_{LOAD}	MTP50N05EL	MTM25N05L
2A	47mV	145mV
1A	22mV	73mV
0.5A	11.5mV	37mV

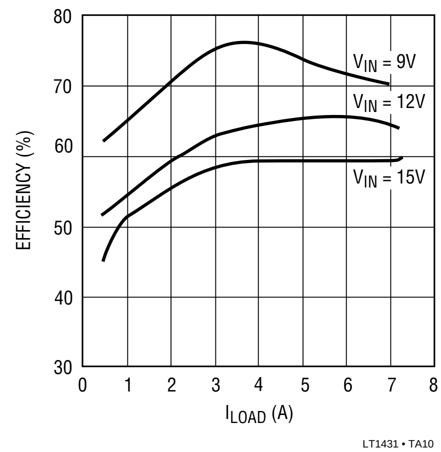
*1.5" #23 SOLID COPPER WIRE
~0.002Ω → 3A LIMIT

TYPICAL APPLICATIO NS

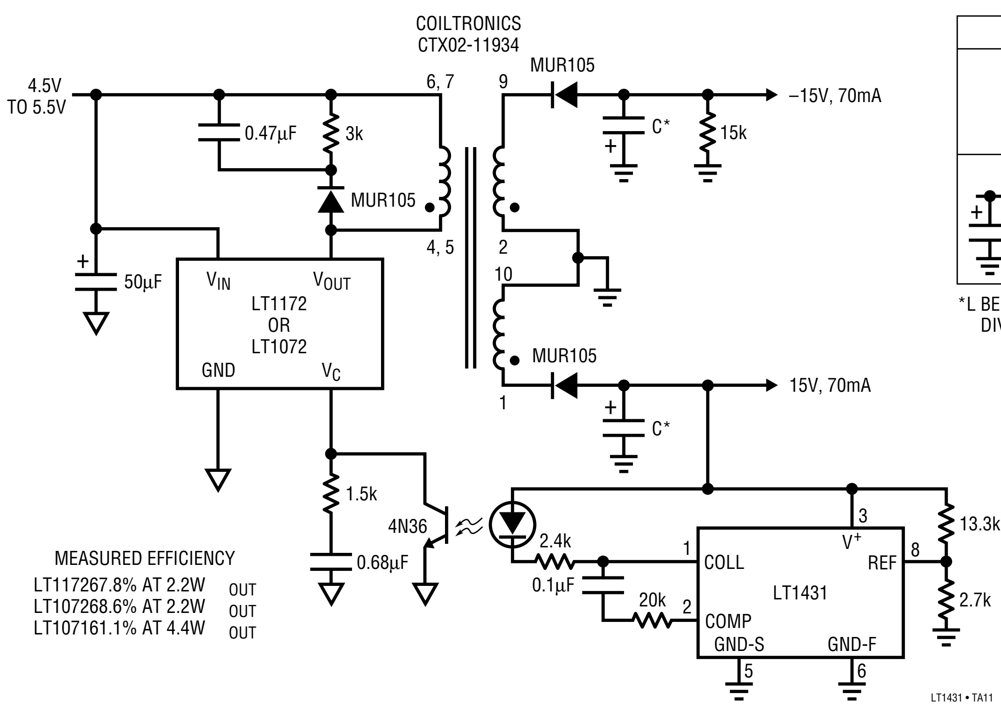
12V to 5V Buck Converter with Foldback Current Limit*



Buck Converter Efficiency



Isolated 5V to ±15V Flyback Converter



Fully Loaded Output Ripple vs Filtering

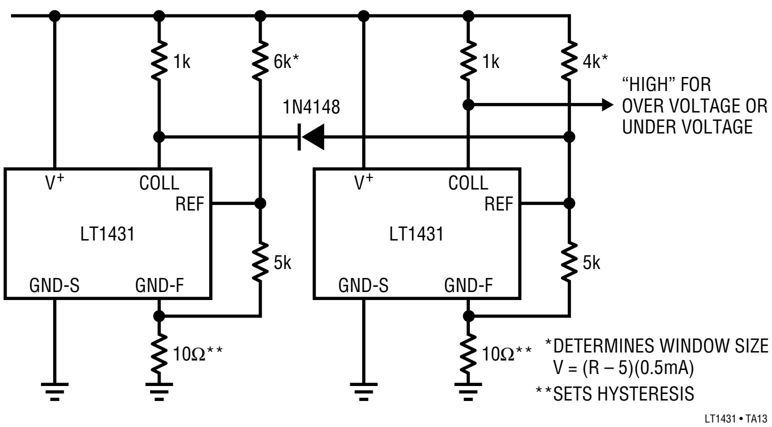
C*	LT1172	LT1072
210µF	30mV$_{P-P}$	40mV$_{P-P}$
L*, 100µF, 100µF	6mV$_{P-P}$	8mV$_{P-P}$

*L BELL INDUSTRIES J.W. MILLER DIVISION 9310-36 10µH, 450mA

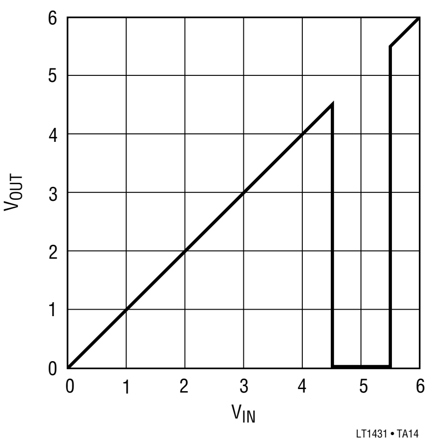
LT1431 • TA12

TYPICAL APPLICATIONS

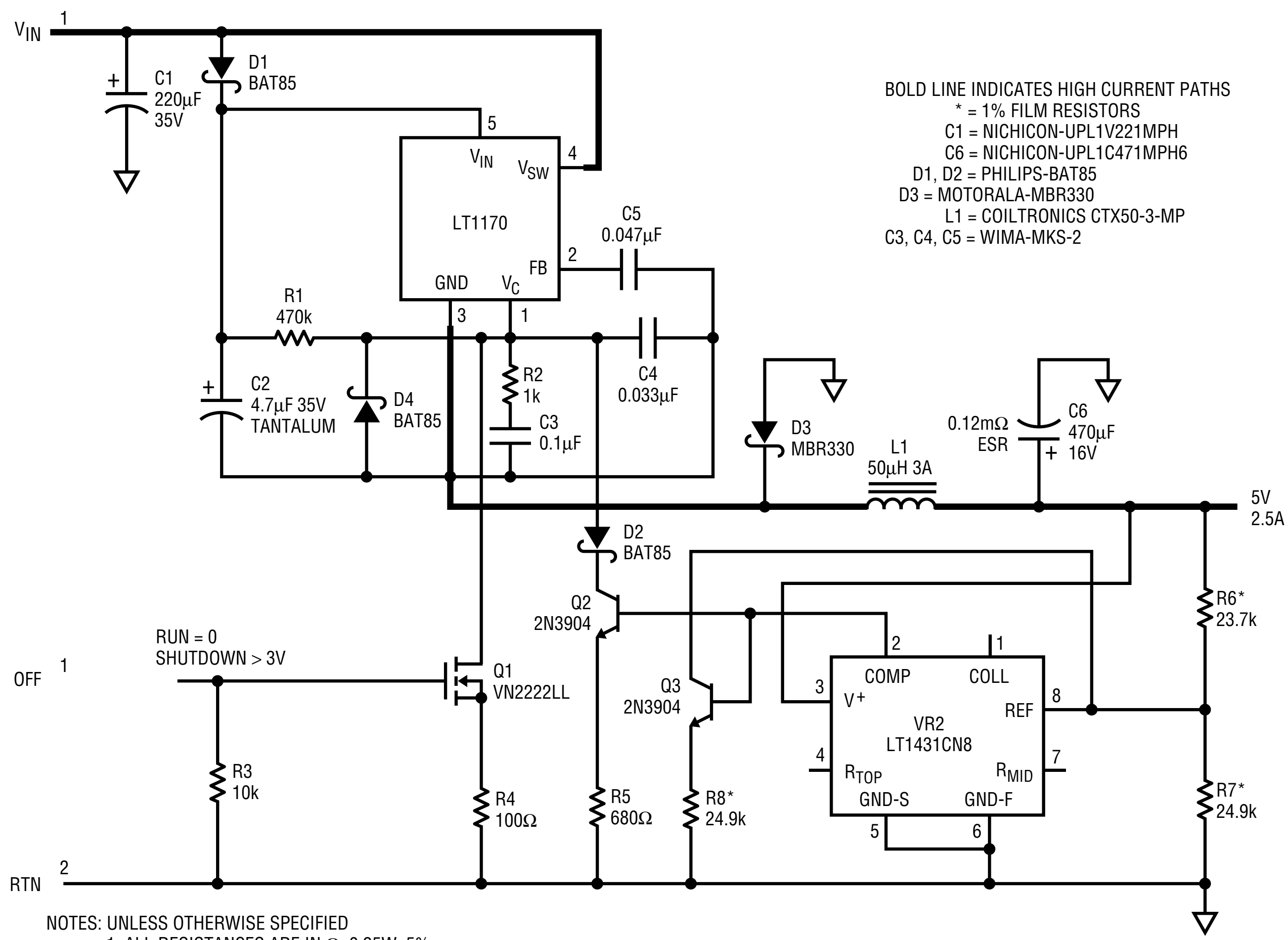
5V Power Supply Monitor with ±500mV Window and 50mV Hysteresis



Transfer Function

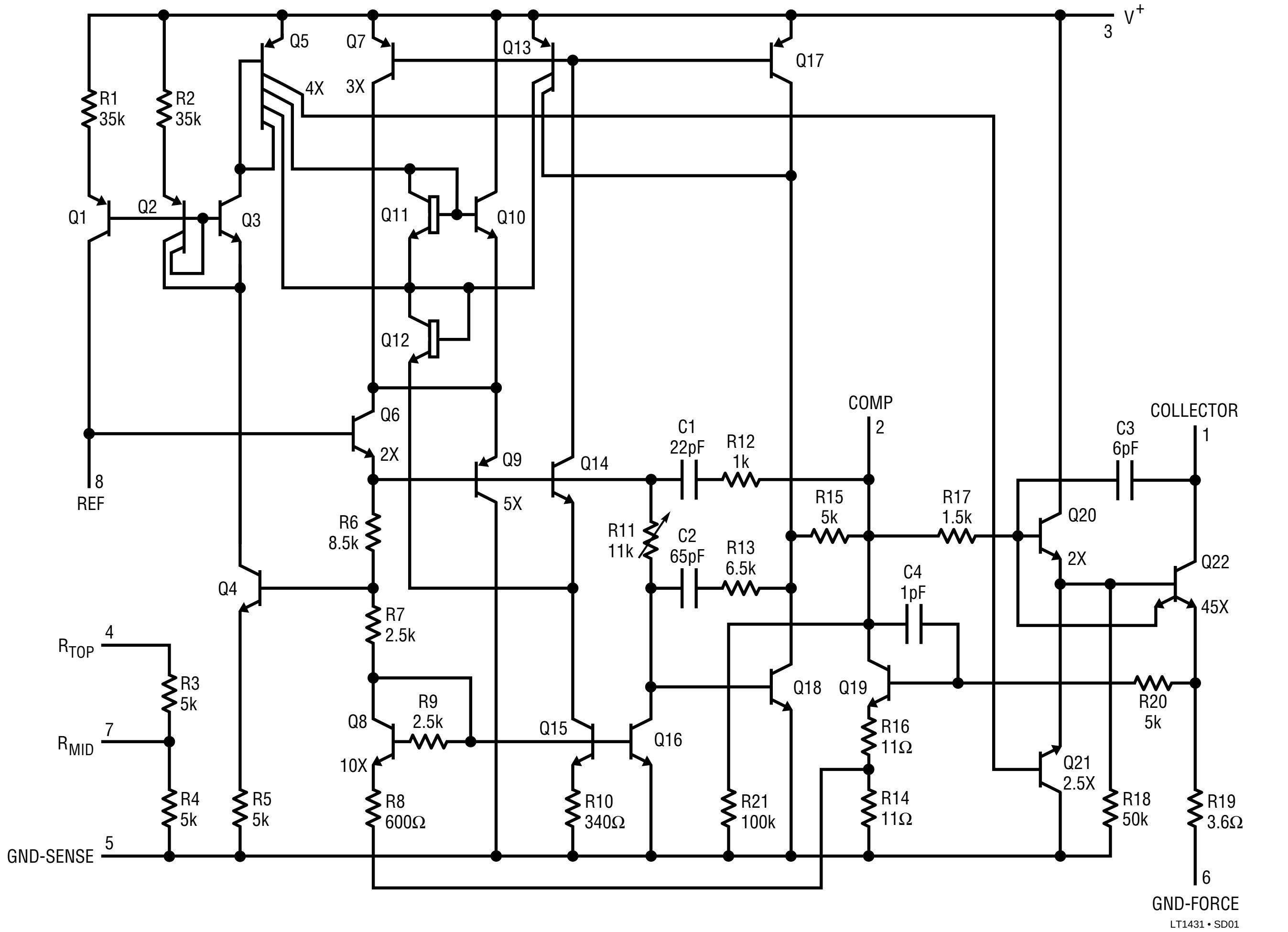


High Efficiency Buck Converter E = 85% to 89%



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN Ω, 0.25W, 5%
2. ALL CAPACITANCES ARE IN µF, 50V, 10%
3. SHUTDOWN LOGIC STATE MUST BE DEFINED BY A LOGIC GATE OR BY TYING TO GND

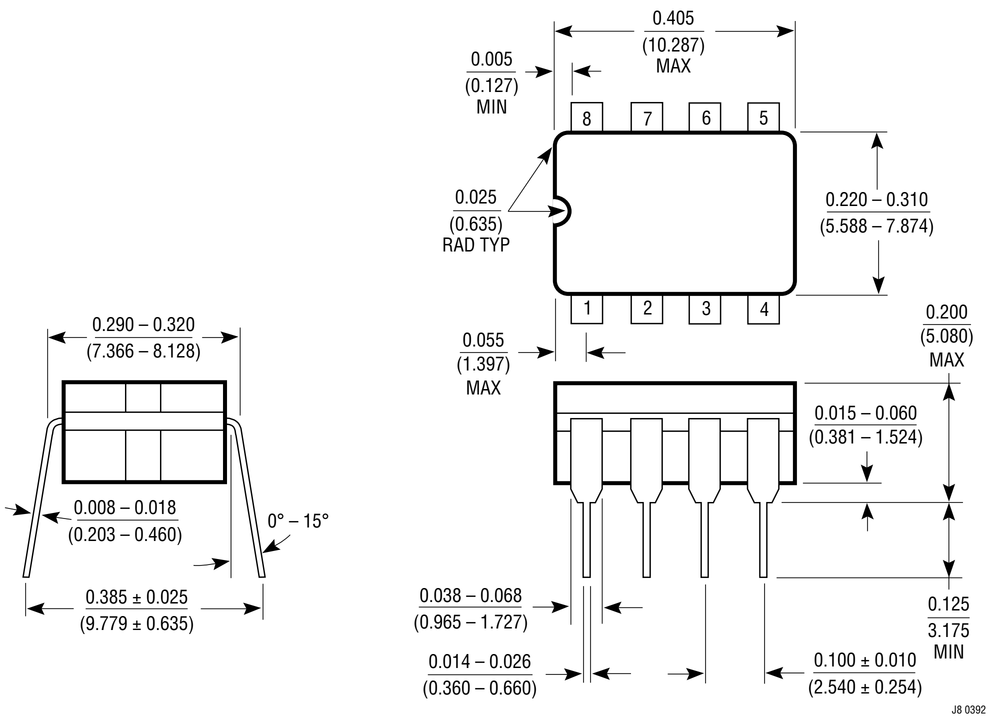
SCHEMATIC DIAGRAM



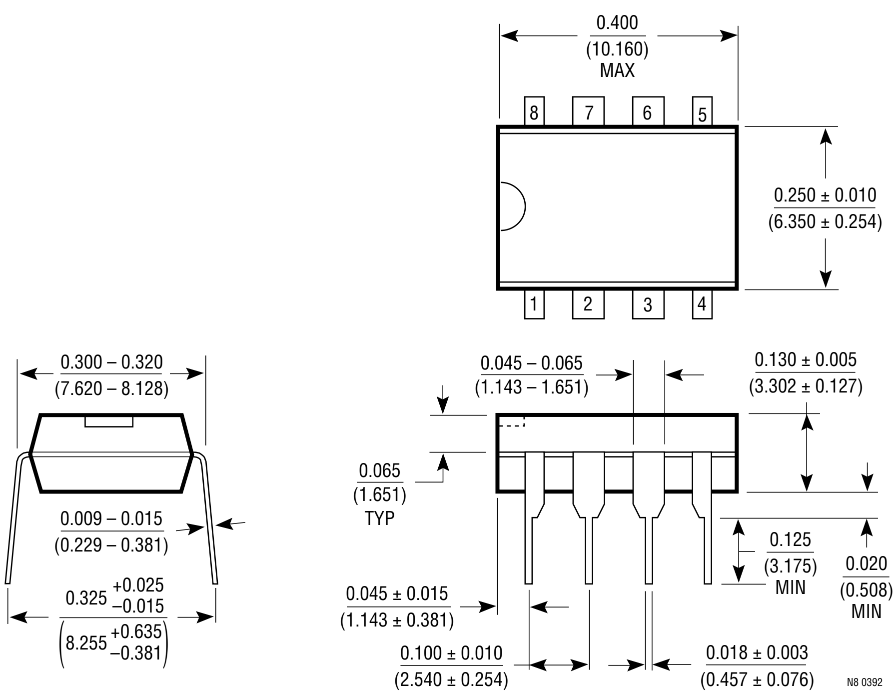
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8-Lead Ceramic DIP

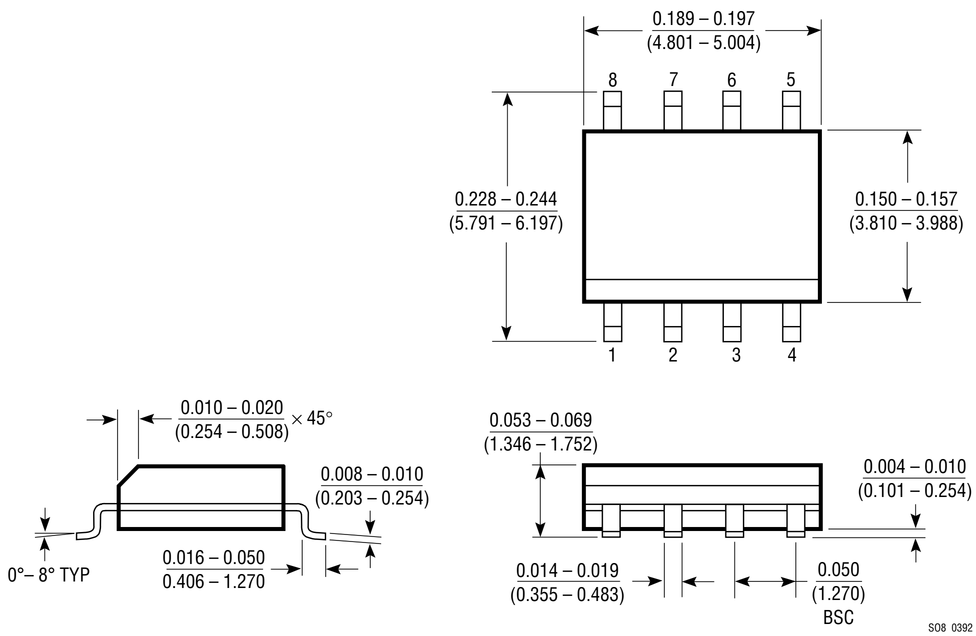


N8 Package
8-Lead Plastic DIP

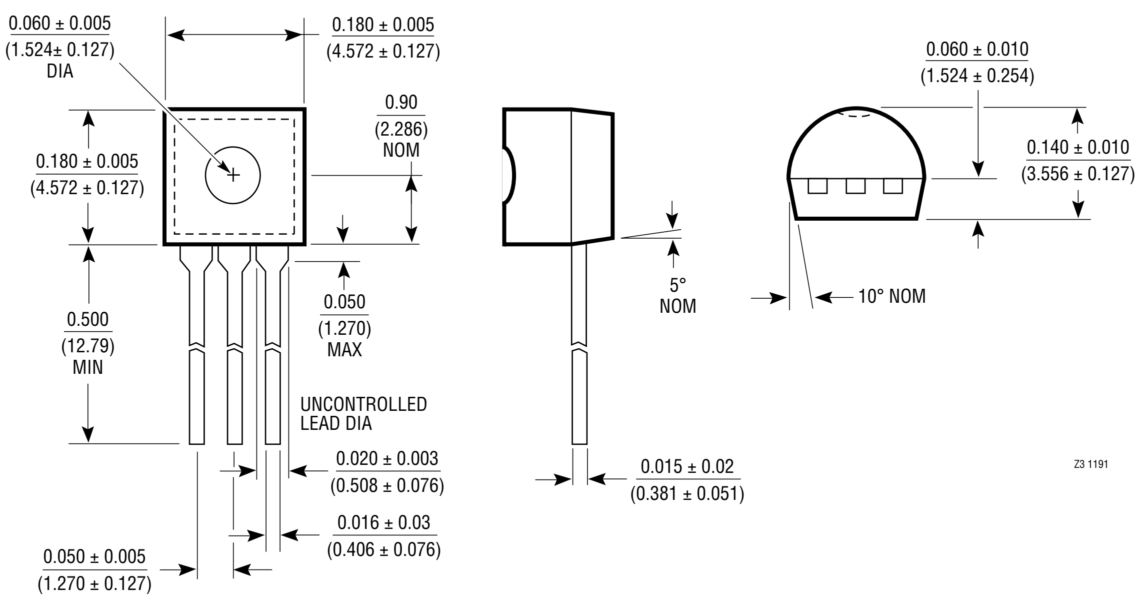


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic SOIC



Z Package
3-Lead TO-92



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LT/GP1292 5K REV B

LINEAR TECHNOLOGY