

## BUS-CONTROLLED VIDEO MATRIX SWITCH

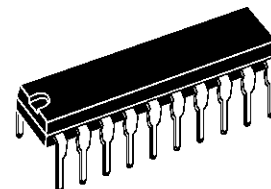
- 20MHz BANDWIDTH
- CASCADABLE WITH ANOTHER TEA6415C (INTERNAL ADDRESS CAN BE CHANGED BY PIN 7 VOLTAGE)
- 8 INPUTS (CVBS, RGB, MAC, CHROMA, ...)
- 6 OUTPUTS
- POSSIBILITY OF MAC OR CHROMA SIGNAL FOR EACH INPUT BY SWITCHING-OFF THE CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- -55dB CROSSTALK AT 5MHz
- FULLY ESD PROTECTED

### DESCRIPTION

The main function of the TEA6415C is to switch 8 video input sources on the 6 outputs.

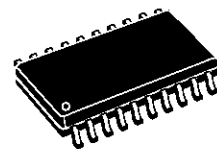
Each output can be switched to only one of the inputs whereas but any same input may be connected to several outputs.

All the switching possibilities are controlled through the I<sup>2</sup>C bus.



**DIP20**  
(Plastic Package)

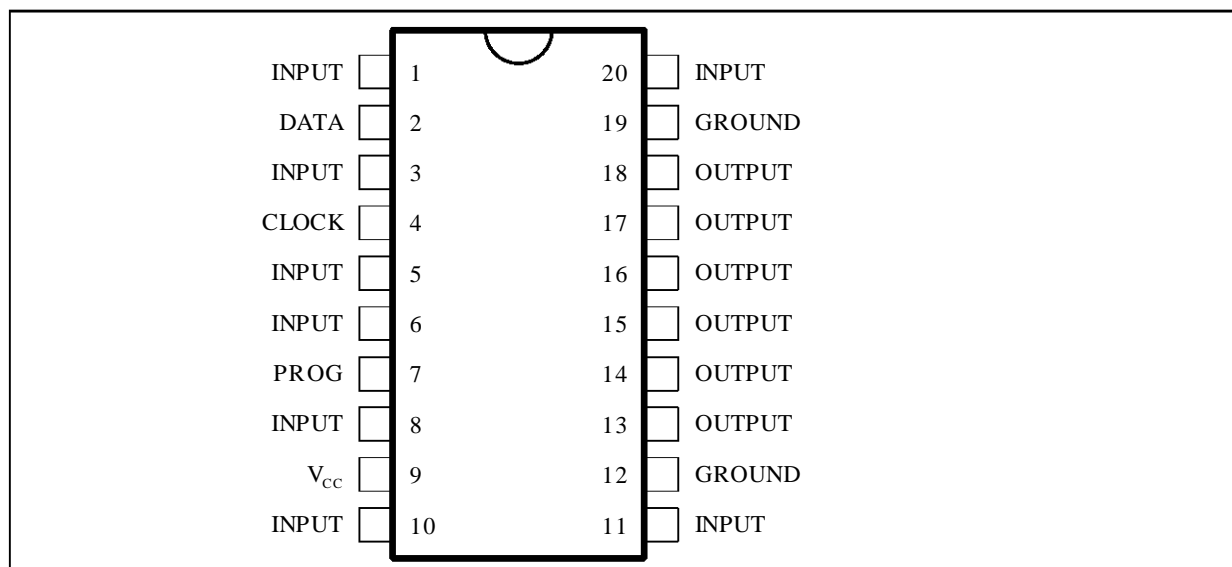
**ORDER CODE : TEA6415C**



**SO20**  
(Plastic Micropackage)

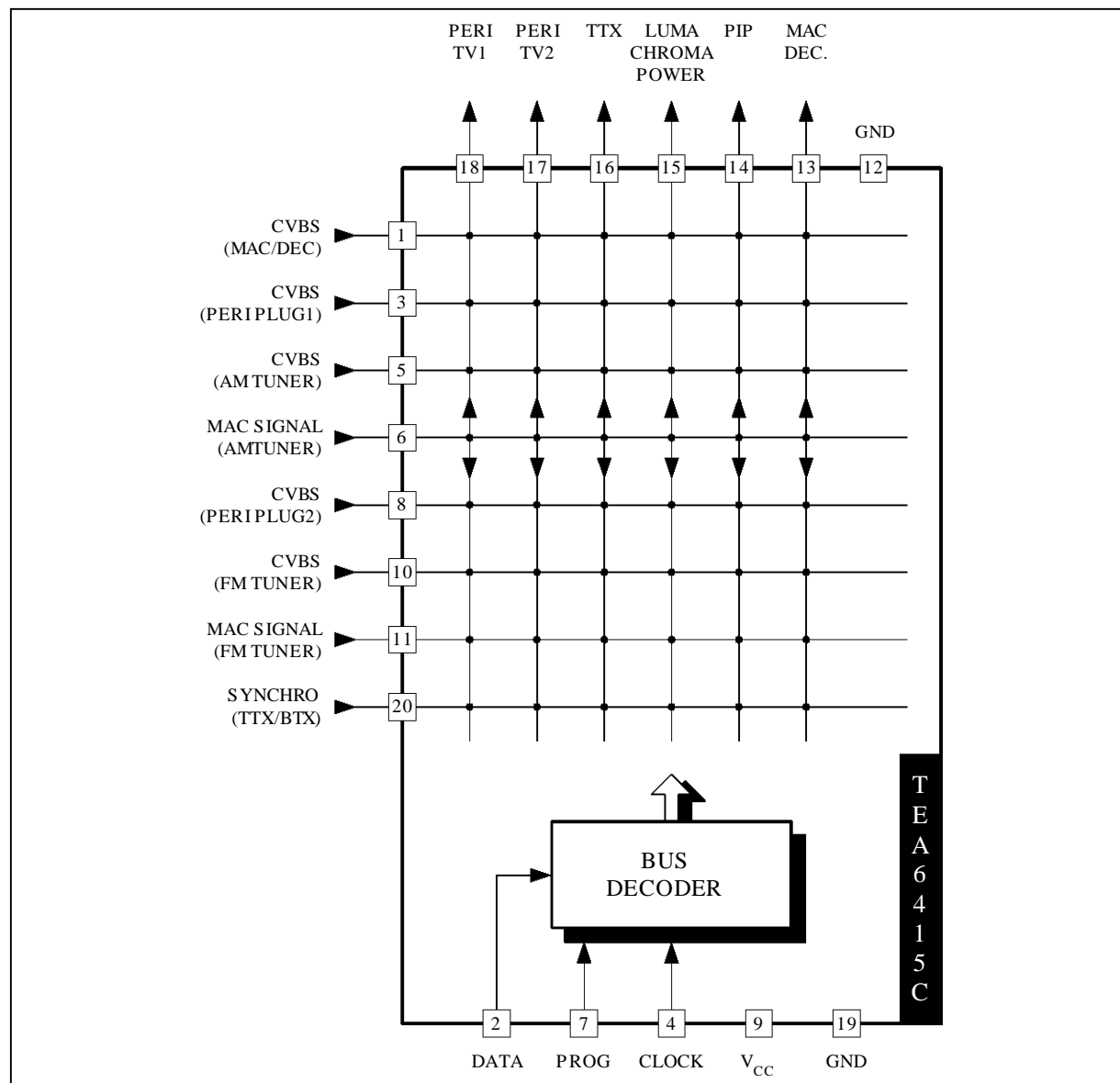
**ORDER CODE : TEA6415CD**

### PIN CONNECTIONS



6415C-01.EPS

## BLOCK DIAGRAM



## GENERAL DESCRIPTION

The main function of the IC is to switch 8 video input sources on 6 outputs.

Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V<sub>DC</sub> on the input. Each input can be used as a normal input or as a MAC or Chroma

input (with external resistor bridge). All the switching possibilities are changed through the BUS.

Driving 75Ω load needs an external transistor.

It is possible to have the same input connected to several outputs.

The starting configuration upon power on (power supply : 0 to 10V) is undetermined.

In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (Pin 9)	12	V
$T_A$	Operating Ambient Temperature	0, +70	°C
$T_{stg}$	Storage Temperature	- 20, +150	°C

6415C-01.TBL

**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	80 100	°C/W °C/W

6415C-02.TBL

**ELECTRICAL CHARACTERISTICS**

$T_A = 25^{\circ}\text{C}$  ,  $V_{CC} = 10\text{V}$  ,  $R_{LOAD} = 10\text{k}\Omega$  ,  $C_{LOAD} = 3\text{pF}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage (Pin 9)	8	10	11	V
$I_{CC}$	Power Supply Current (without load on outputs ; $V_{CC} = 10\text{V}$ )	20	30	40	mA

**INPUTS**

	Signal Amplitude (CVBS signal)			2	$V_{PP}$
	Input Current (per output connected, input voltage = $5V_{DC}$ ) (this current is X6 when all outputs are connected on the input)		1	3	$\mu\text{A}$
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (temperature from 0 to $70^{\circ}\text{C}$ )		5	100	mV

**OUTPUTS** ( $V_{IN} = 1V_{PP}$  for all dynamic tests) Pins 13 - 14 - 15 - 16 - 17 - 18

	Dynamic	4.5	5.5		$V_{PP}$
	Output Impedance		25	50	$\Omega$
	Gain	6	6.5	7	dB
	Bandwidth -1dB attenuation -3dB attenuation	7	15 20		MHz MHz
	Crosstalk $f = 5\text{MHz}$ $f = 3.58\text{MHz}$		- 55 - 60	- 45 - 50	dB dB
	DC level	2.4	2.75	3.1	V

6415C-03.TBL

**I<sup>2</sup>C BUS CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
<b>SCL</b>					
V <sub>IL</sub>	Low Level Input Voltage		- 0.3	+ 1.5	V
V <sub>IH</sub>	High Level Input Voltage		3.0	V <sub>CC</sub> + 0.5	V
I <sub>LI</sub>	Input Leakage Current	V <sub>I</sub> = 0 to V <sub>CC</sub>	- 10	+ 10	μA
f <sub>SCL</sub>	Clock Frequency		0	100	kHz
t <sub>R</sub>	Input Rise Time	1.5V to 3V		1000	ns
t <sub>F</sub>	Input Fall Time	1.5V to 3V		300	ns
C <sub>I</sub>	Input Capacitance			10	pF

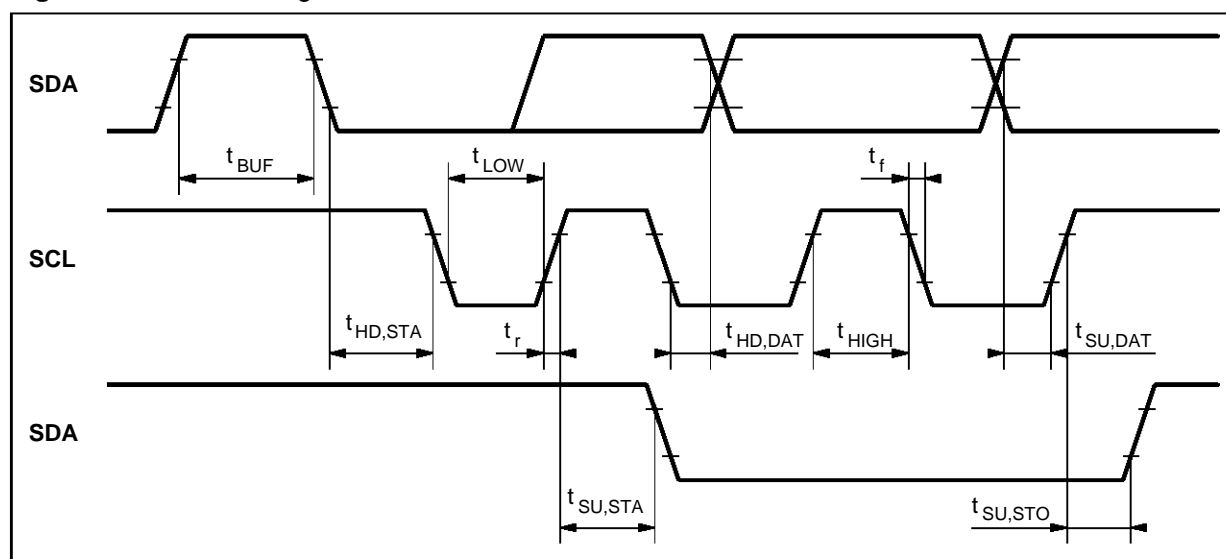
**SDA**

V <sub>IL</sub>	Low Level Input Voltage		- 0.3	+ 1.5	V
V <sub>IH</sub>	High Level Input Voltage		3.0	V <sub>CC</sub> + 0.5	V
I <sub>LI</sub>	Input Leakage Current	V <sub>I</sub> = 0 to V <sub>CC</sub>	- 10	+ 10	μA
C <sub>I</sub>	Input Capacitance			10	pF
t <sub>R</sub>	Input Rise Time	1.5V to 3V		1000	ns
t <sub>F</sub>	Input Fall Time	1.5V to 3V		300	ns
V <sub>OL</sub>	Low Level Output Voltage	I <sub>OL</sub> = 3mA		0.4	V
t <sub>F</sub>	Output Fall Time	3V to 1.5V		250	ns
C <sub>L</sub>	Load Capacitance			400	pF

**TIMING**

t <sub>LOW</sub>	Clock Low Period		4.7		μs
t <sub>HIGH</sub>	Clock High Period		4.0		μs
t <sub>SU, DAT</sub>	Data Set-up Time		250		ns
t <sub>HD, DAT</sub>	Data Hold Time		0	340	ns
t <sub>SU, STO</sub>	Set-up Time from Clock High to Stop		4.0		μs
t <sub>BUF</sub>	Start Set-up Time following a Stop		4.7		μs
t <sub>HD, STA</sub>	Start Hold Time		4.0		μs
t <sub>SU, STA</sub>	Start Set-up Time following Clock Low-to-High Transition		4.7		μs

6415C-06.TBL

**Figure 1 : I<sup>2</sup>C Bus Timing**

6415C-10.EPS

**BUS SELECTIONS (I<sup>2</sup>C-BUS)**

2nd byte of transmission

ADDRESS MSB	DATA LSB	Selected Output	
00000	XXX	Pin 18	Output is selected by address bits
00100	XXX	Pin 14	
00010	XXX	Pin 16	
00110	---	Not used	
00001	XXX	Pin 17	
00101	XXX	Pin 13	
00011	XXX	Pin 15	
00111	---	Not used	
		Selected Input	
00XXX	000	Pin 5	Input is selected by data bits
00XXX	100	Pin 8	
00XXX	010	Pin 3	
00XXX	110	Pin 20	
00XXX	001	Pin 6	
00XXX	101	Pin 10	
00XXX	011	Pin 1	
00XXX	111	Pin 11	

6415C-04.TBL

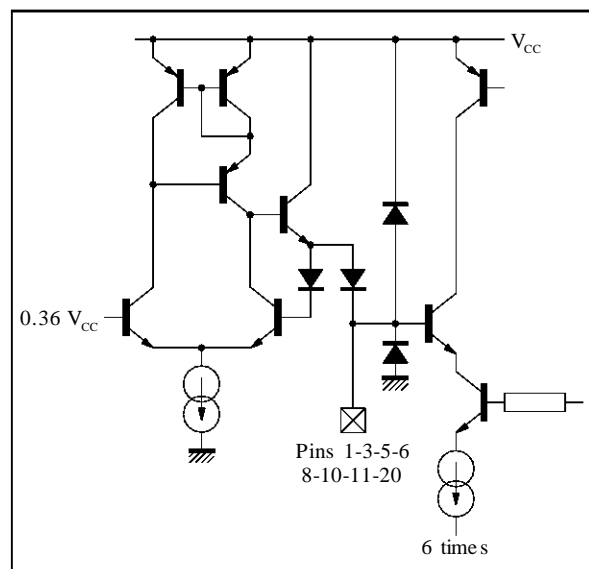
**Example :** 00100 101 connects Pin 10 (input) to Pin 14 (output) (equals 25 in hexadecimal)  
Adress byte (1st byte of transmission)

86	1000	0110
06	0000	0110

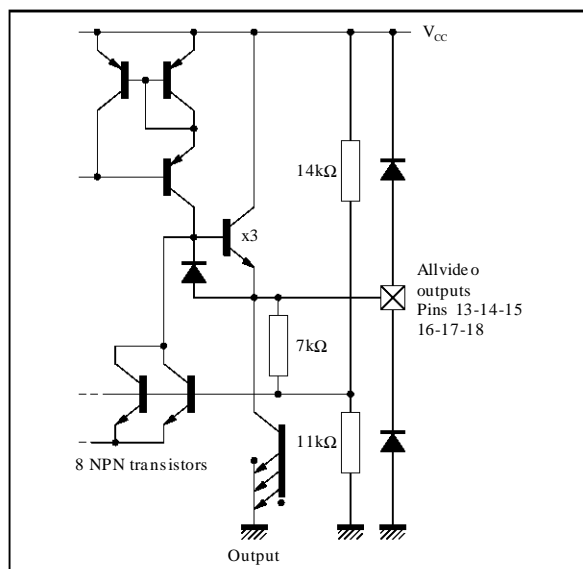
When pin PROG is connected to ground

When pin PROG is connected to V<sub>CC</sub>

6415C-05.TBL

**IN / OUT PIN CONFIGURATION****Figure 2 : Input Configuration**

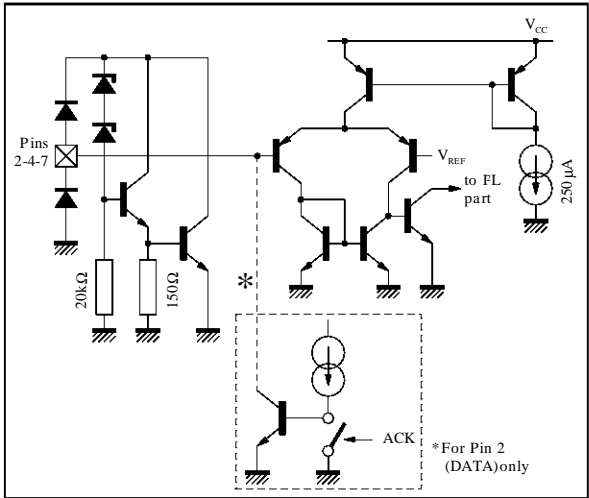
6415C-03.EPS

**Figure 3 : Output Configuration**

6415C-04.EPS

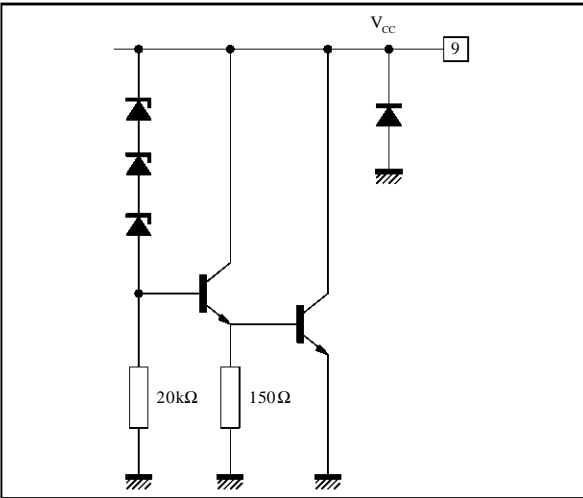
IN / OUT PIN CONFIGURATION (continued)

Figure 4 : Bus I/O Configuration



6415C-05.EPS

Figure 5 :  $V_{CC}$  Pin Configuration



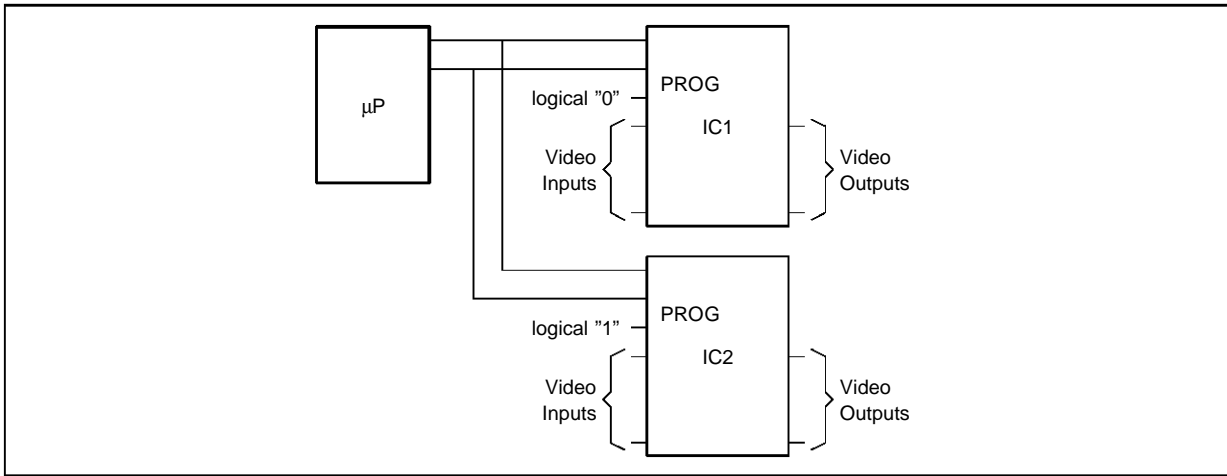
6415C-06.EPS

USE WITH AN OTHER TEA6415C

The programming input (PROG) permits to operate with two TEA6415C in parallel and to select them independantly through the I<sup>2</sup>C-BUS without

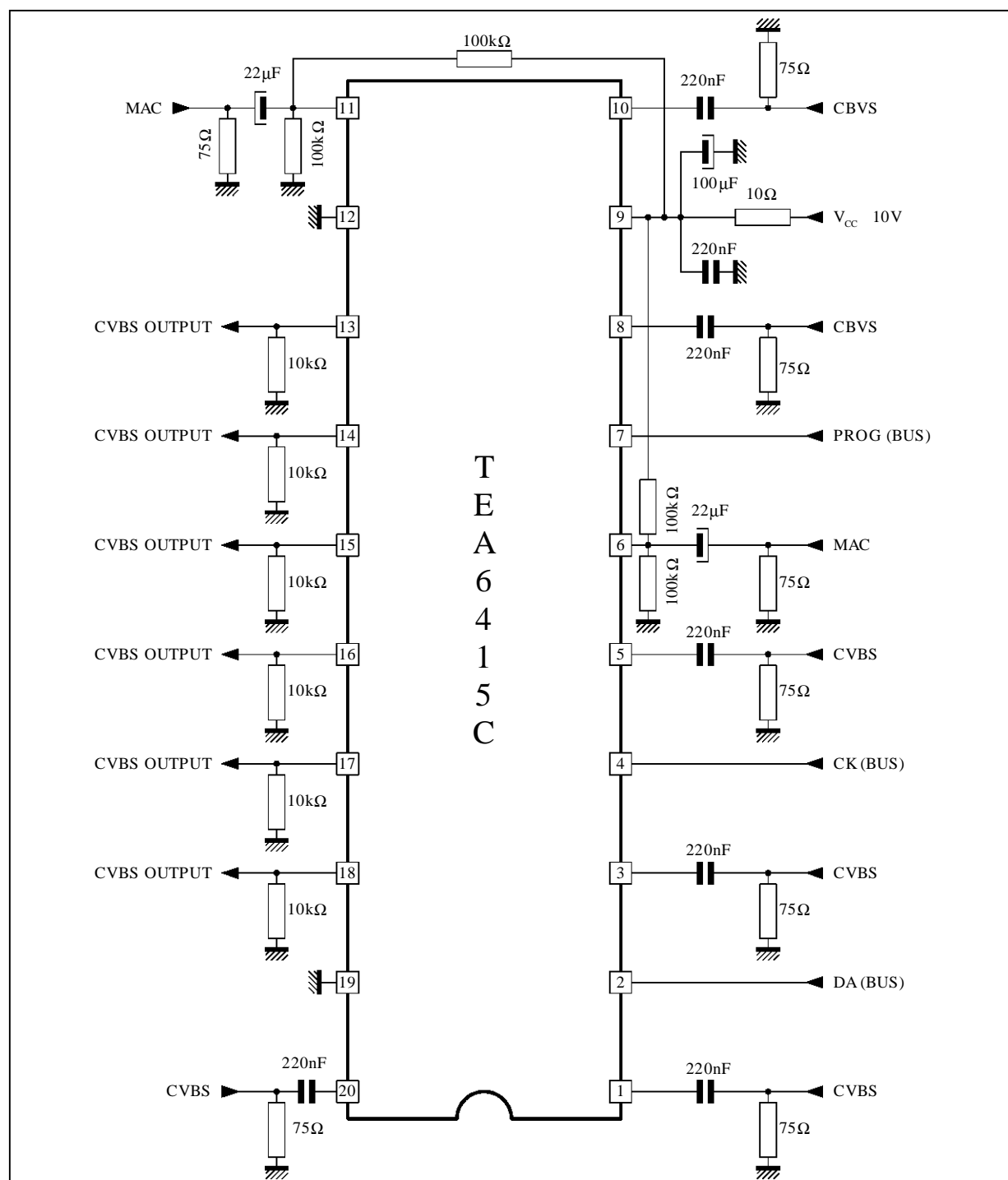
modifying the adress byte. Consequently, the switch capabilities are doubled or IC1 and IC2 can be cascaded.

Figure 6



6415C-07.EPS

## TYPICAL APPLICATION



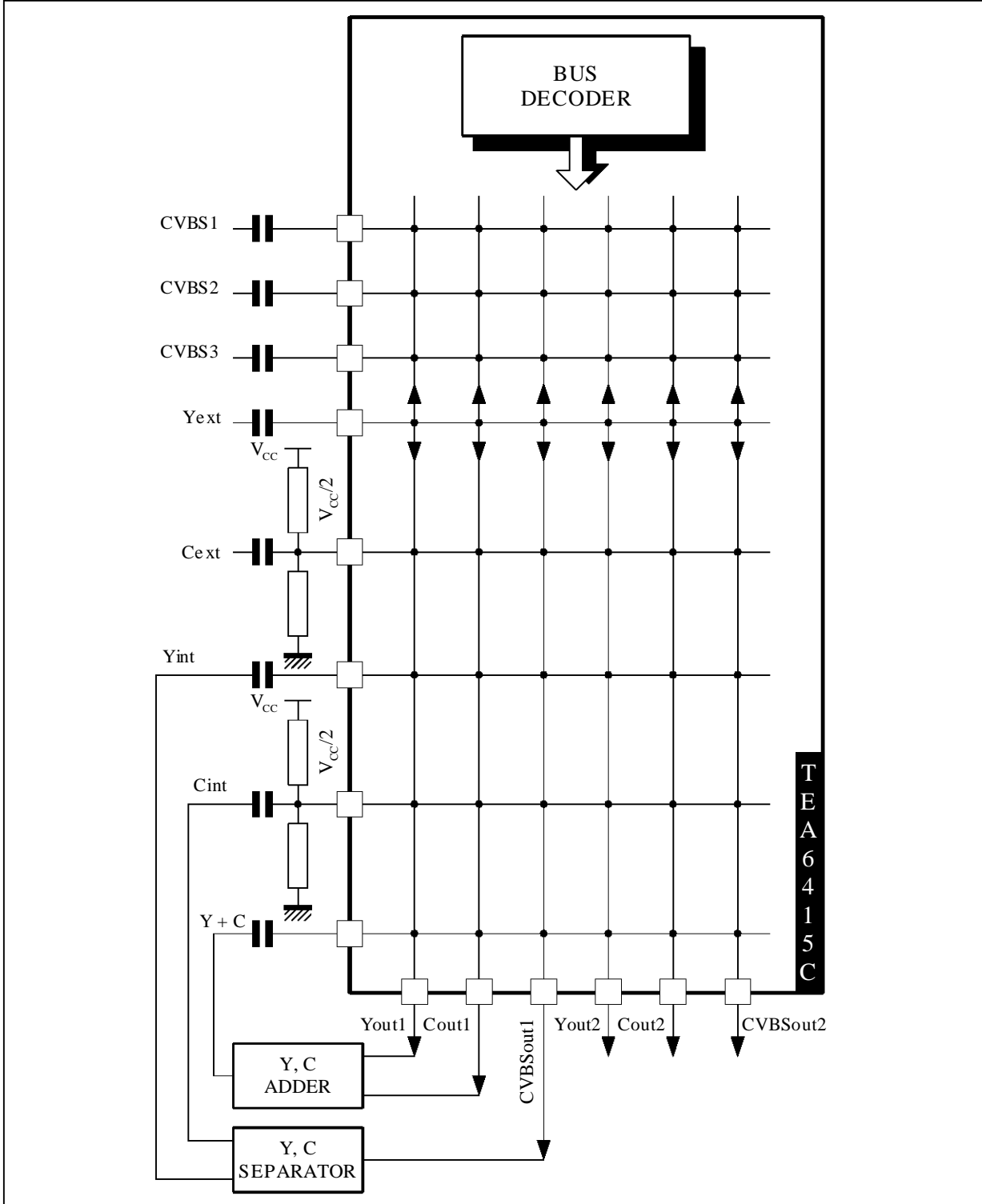
6415C-08.EPS

## CROSSTALK IMPROVEMENT

1 - When any input is not used, it must be bypassed to ground through a 220nF capacitor.

2 - An important improvement can be achieved considering the input crosstalk by means of the application (see technical note).

OTHER APPLICATION DIAGRAM EXAMPLE

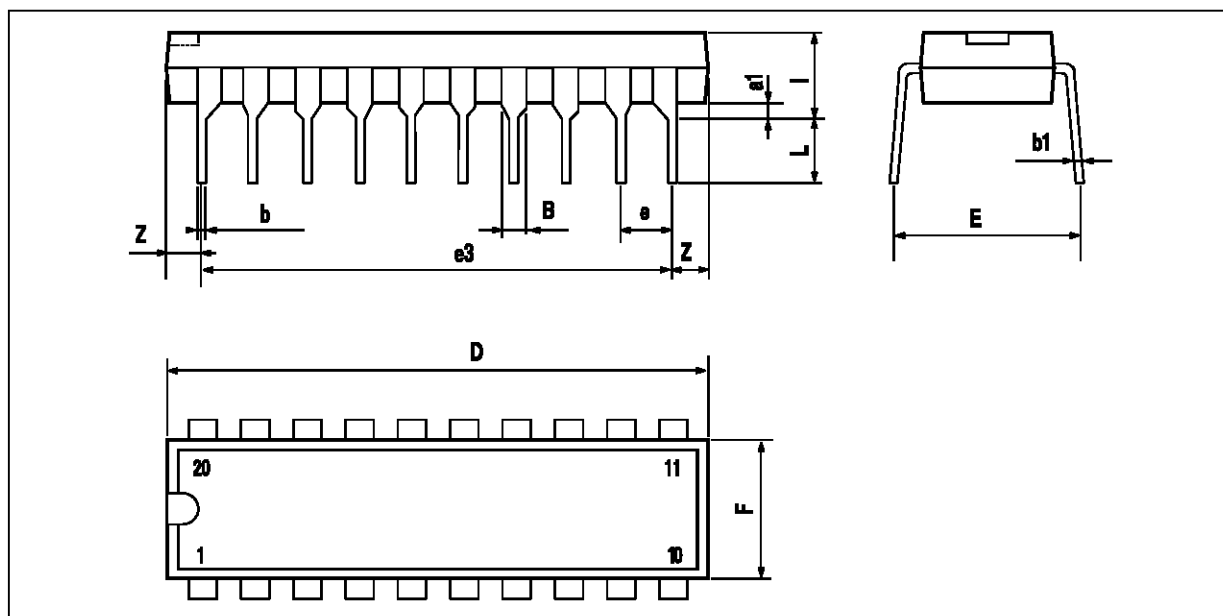


6415C-08.EPS



**PACKAGE MECHANICAL DATA**

20 PINS – PLASTIC DIP

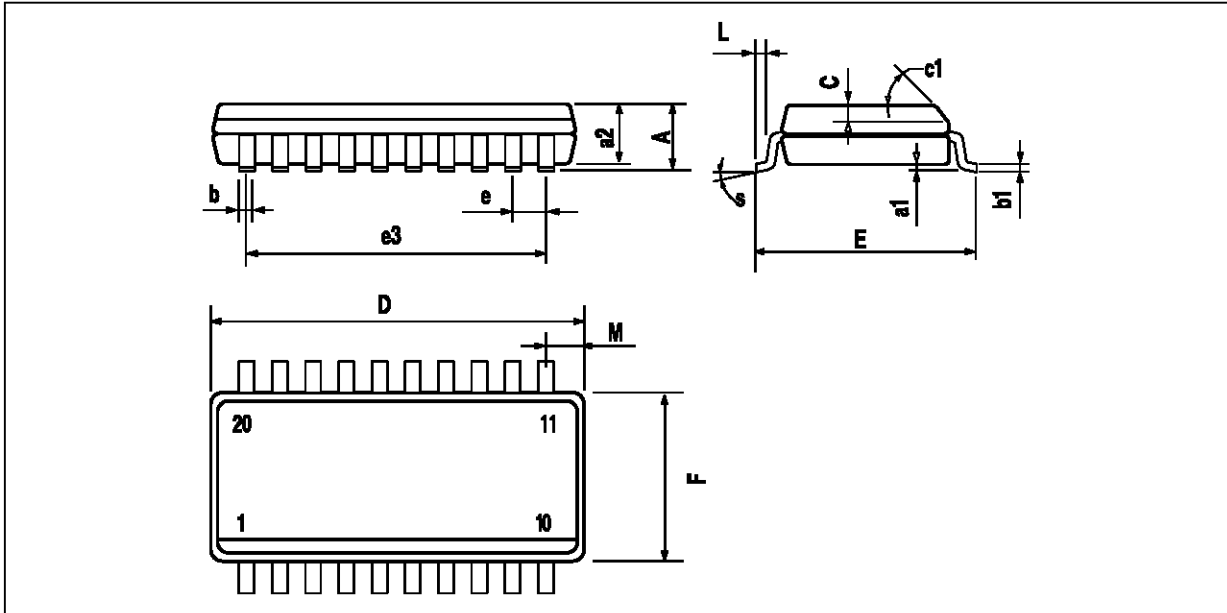


PM-DIP20LEPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
$a_1$	0.254			0.010		
$B$	1.39		1.65	0.055		0.065
$b$		0.45			0.018	
$b_1$		0.25			0.010	
$D$			25.4			1.000
$E$		8.5			0.335	
$e$		2.54			0.100	
$e_3$		22.86			0.900	
$F$			7.1			0.280
$l$			3.93			0.155
$L$		3.3			0.130	
$Z$			1.34			0.053

DIP20.TBL

**PACKAGE MECHANICAL DATA**  
20 PINS – PLASTIC MICROPACKAGE (SO)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (Max.)					

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