International
IOR Rectifier

IR2104(S) & (PbF)

HALF-BRIDGE DRIVER

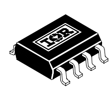
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Internally set deadtime
- High side output in phase with input
- Shut down input turns off both channels
- Matched propagation delay for both channels
- Also available LEAD-FREE

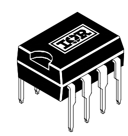
Product Summary

V_{OFFSET}	600V max.
I_O+/-	130 mA / 270 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	680 & 150 ns
Deadtime (typ.)	520 ns

Packages



8 Lead SOIC
IR2104S

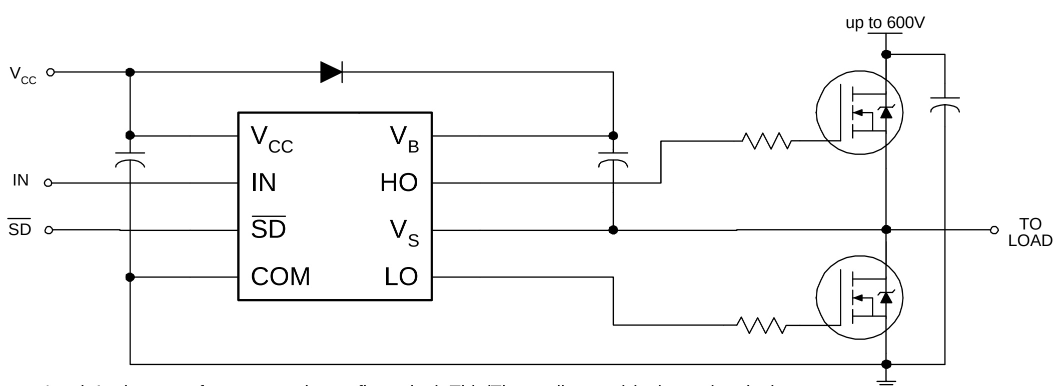


8 Lead PDIP
IR2104

Description

The IR2104(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

Typical Connection



(Refer to Lead Assignment for correct pin configuration) This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \le$ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

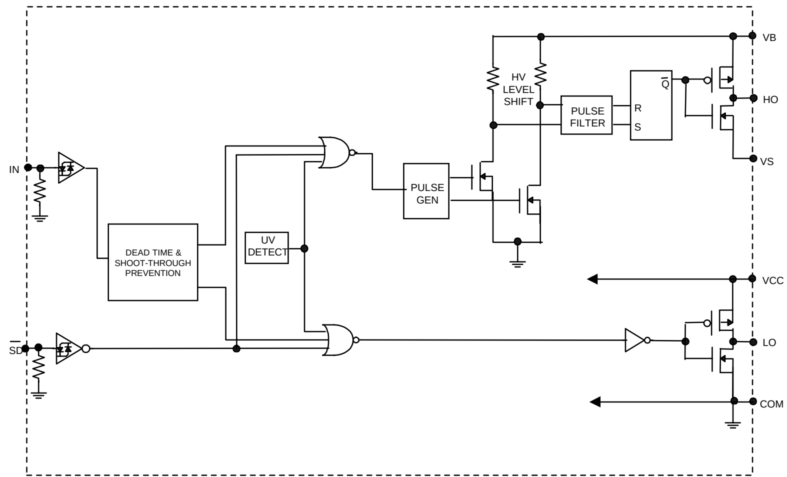
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	820	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 600V
t_{sd}	Shutdown propagation delay	—	160	220		
t_r	Turn-on rise time	—	100	170		
t_f	Turn-off fall time	—	50	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" (HO) & Logic "0" (LO) input voltage	3	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" (HO) & Logic "1" (LO) input voltage	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	SD input positive going threshold	3	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	SD input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	100	mV	I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	100		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		V_{IN} = 0V or 5V
I_{IN+}	Logic "1" input bias current	—	3	10		V_{IN} = 5V
I_{IN-}	Logic "0" input bias current	—	—	1		V_{IN} = 0V
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	V_O = 0V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	360	—		V_O = 15V PW ≤ 10 µs

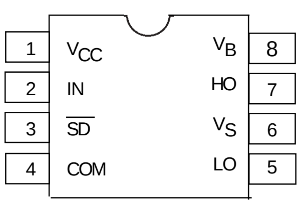
Functional Block Diagram



Lead Definitions

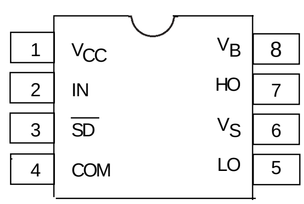
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO
$\overline{SD}$	Logic input for shutdown
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



8 Lead PDIP

IR2104



8 Lead SOIC

IR2104S

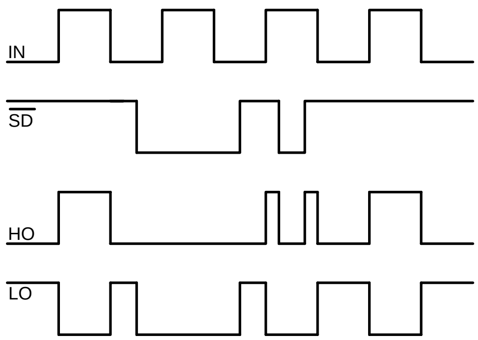


Figure 1. Input/Output Timing Diagram

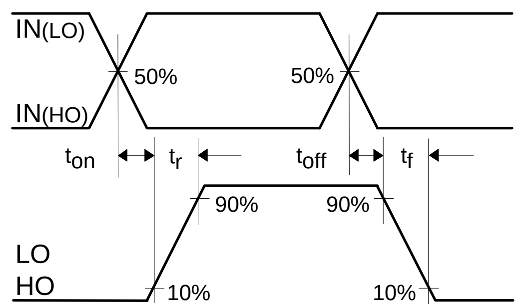


Figure 2. Switching Time Waveform Definitions

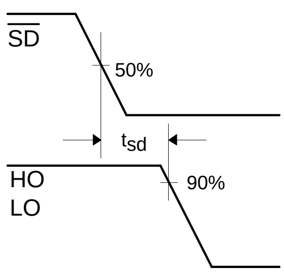


Figure 3. Shutdown Waveform Definitions

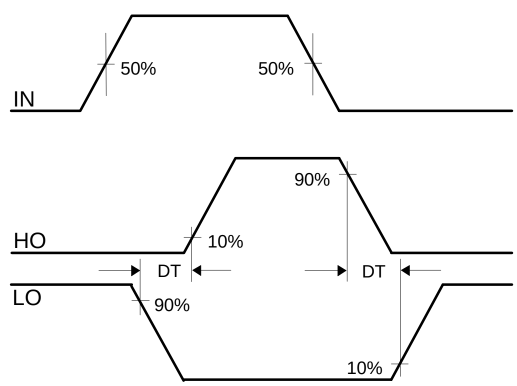


Figure 4. Deadtime Waveform Definitions

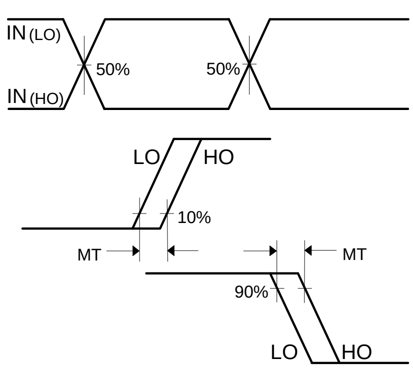


Figure 5. Delay Matching Waveform Definitions

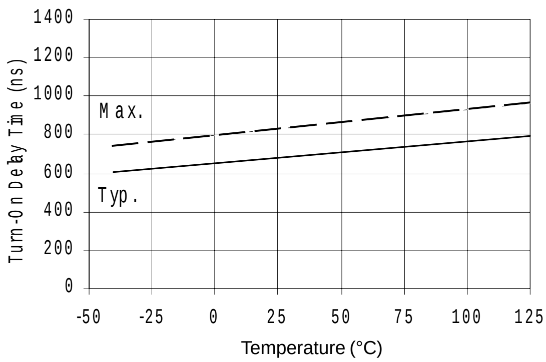


Figure 6A. Turn-On Time vs Temperature

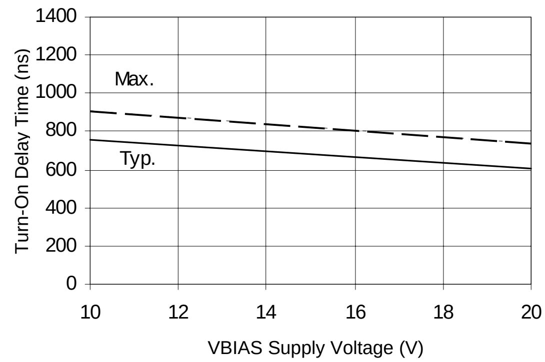


Figure 6B. Turn-On Time vs Supply Voltage

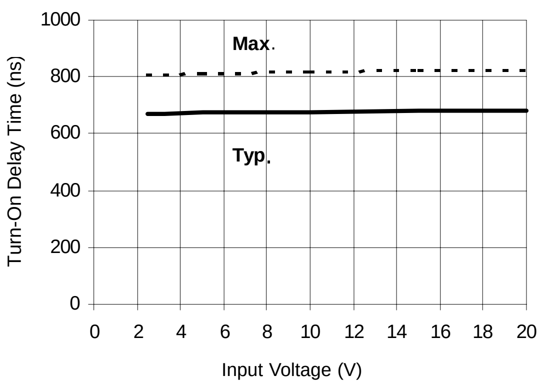


Figure 6C. Turn-On Time vs Input Voltage

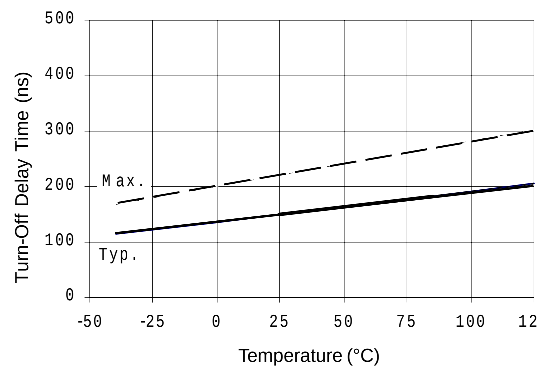


Figure 7A. Turn-Off Time vs Temperature

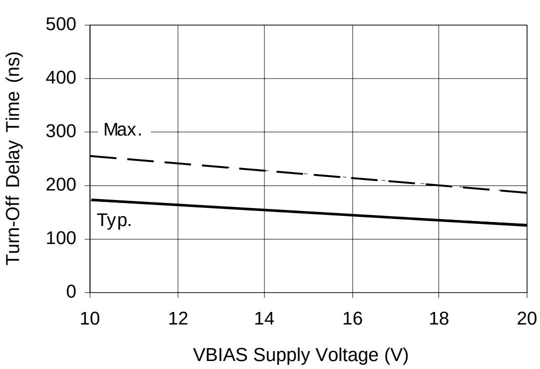


Figure 7B. Turn-Off Time vs Supply Voltage

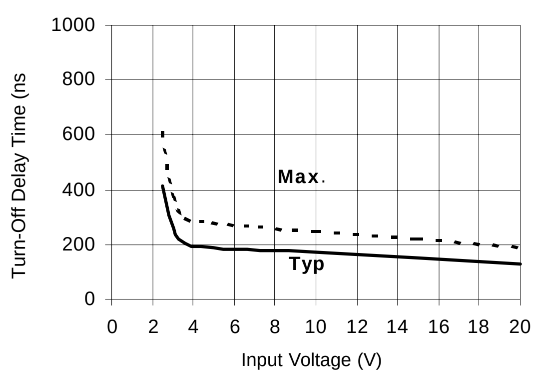


Figure 7C. Turn-Off Time vs Input Voltage

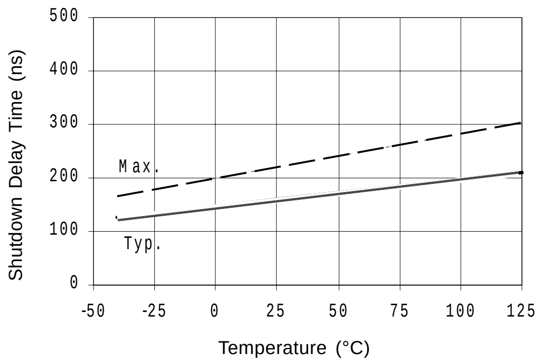


Figure 8A. Shutdown Time vs Temperature

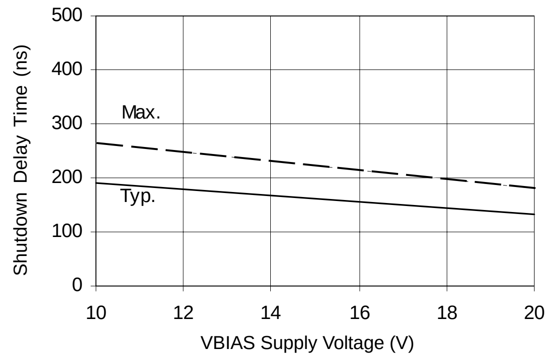


Figure 8B. Shutdown Time vs Voltage

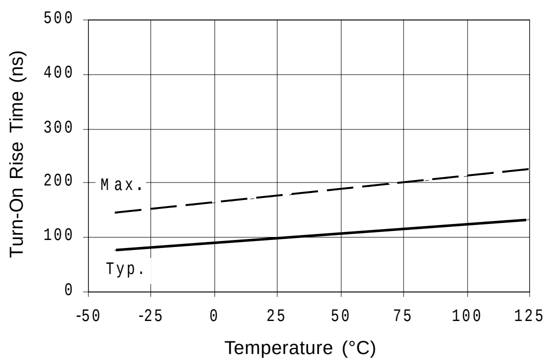


Figure 9A. Turn-On Rise Time vs Temperature

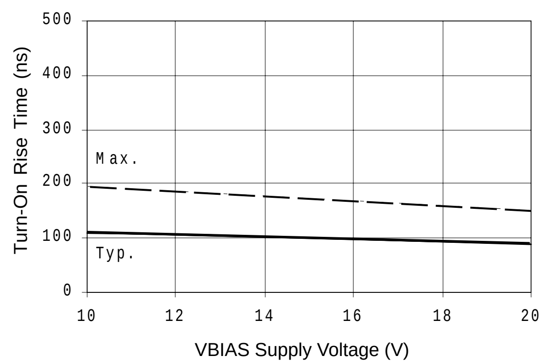


Figure 9B. Turn-On Rise Time vs Voltage

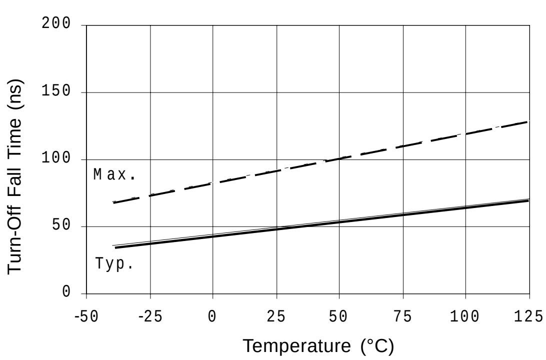


Figure 10A. Turn-Off Fall Time vs Temperature

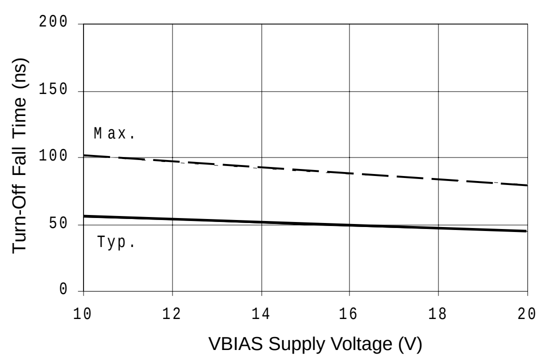


Figure 10B. Turn-Off Fall Time vs Voltage

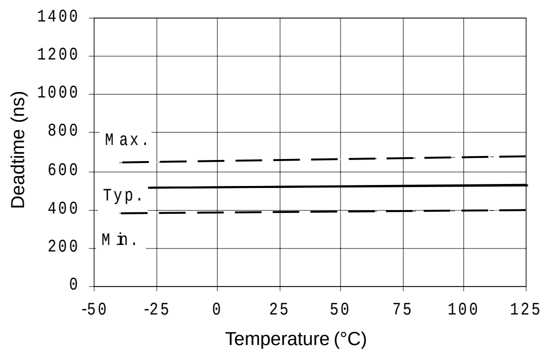


Figure 11A. Deadtime vs Temperature

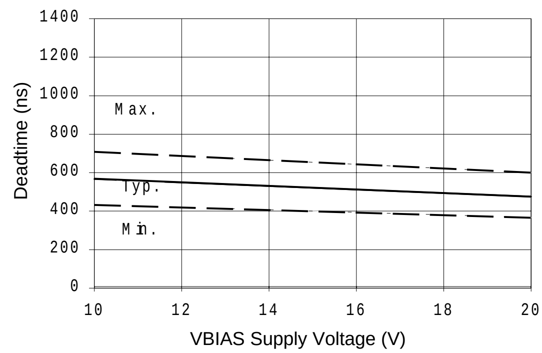


Figure 11B. Deadtime vs Voltage

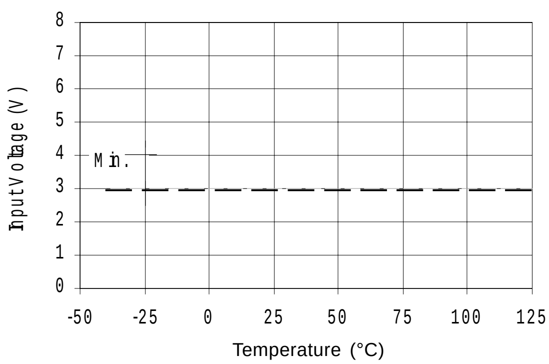


Figure 12A. Logic "1" (HO) & Logic “0” (LO) & Inactive SD Input Voltage vs Temperature

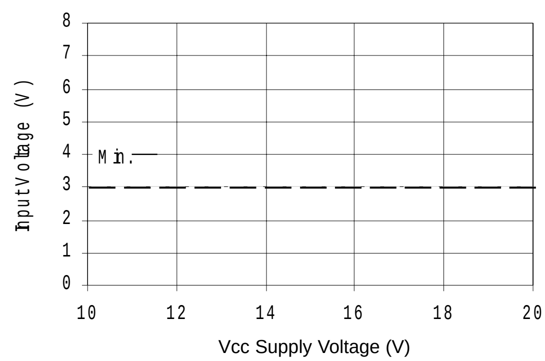


Figure 12B. Logic "1" (HO) & Logic “0” (LO) & Inactive SD Input Voltage vs Voltage

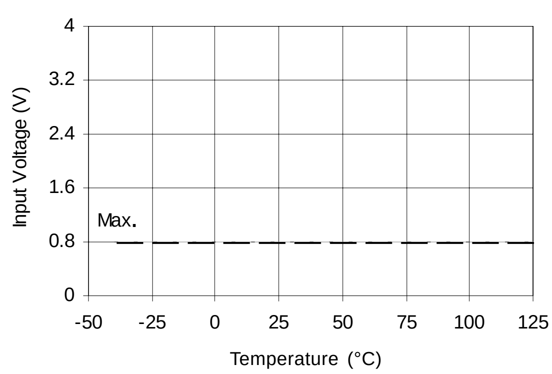


Figure 13A. Logic "0" (HO) & Logic “1” (LO) & Active SD Input Voltage vs Temperature

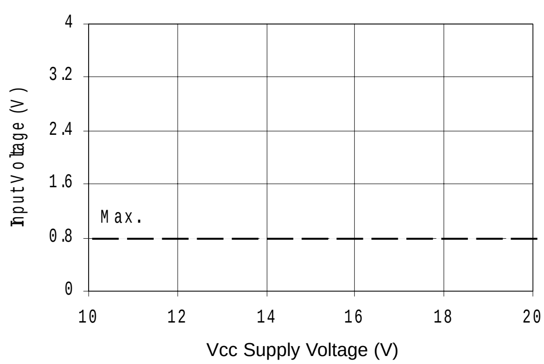


Figure 13B. Logic "0" (HO) & Logic “1” (LO) & Active SD Input Voltage vs Voltage

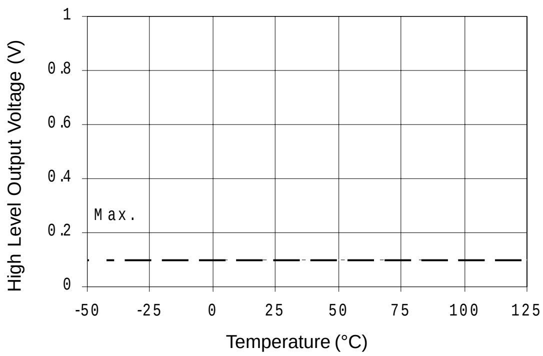


Figure 14A. High Level Output vs Temperature

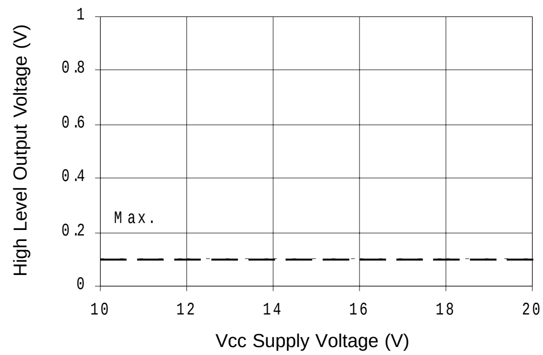


Figure 14B. High Level Output vs Voltage

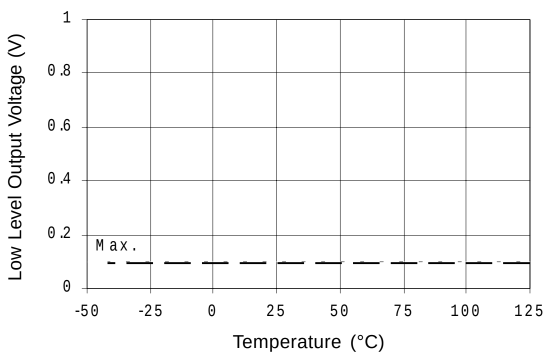


Figure 15A. Low Level Output vs Temperature

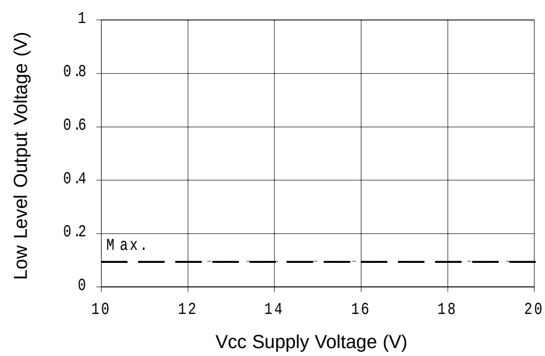


Figure 15B. Low level Output vs Voltage

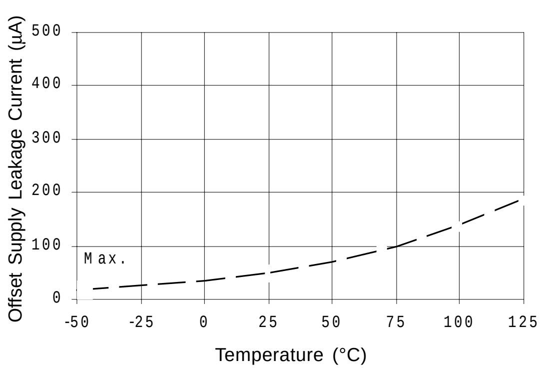


Figure 16A. Offset Supply Current vs Temperature

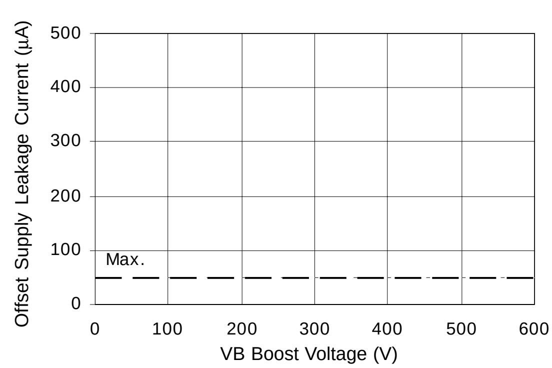


Figure 16B. Offset Supply Current vs Voltage

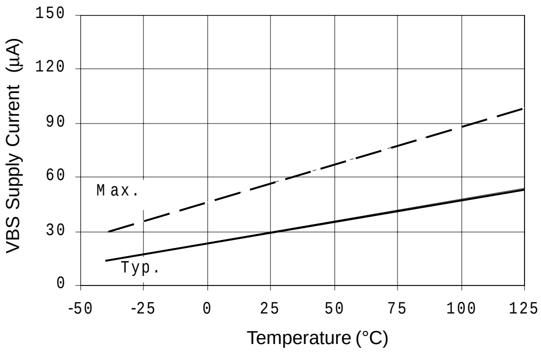


Figure 17A. V_{BS} Supply Current vs Temperature

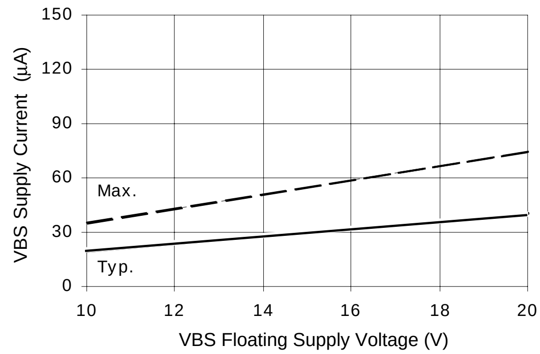


Figure 17B. V_{BS} Supply Current vs Voltage

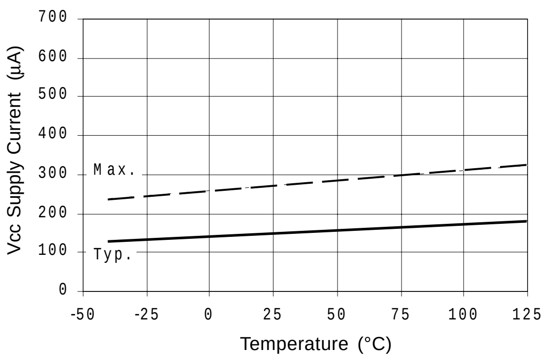


Figure 18A. Vcc Supply Current vs Temperature

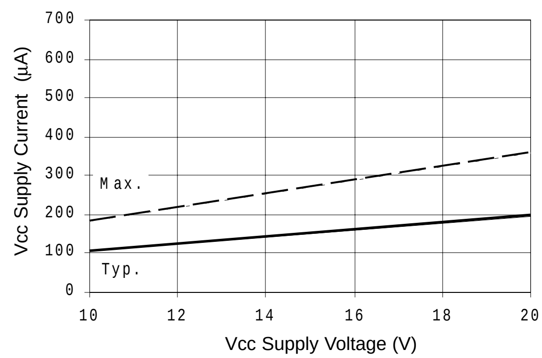


Figure 18B. Vcc Supply Current vs Voltage

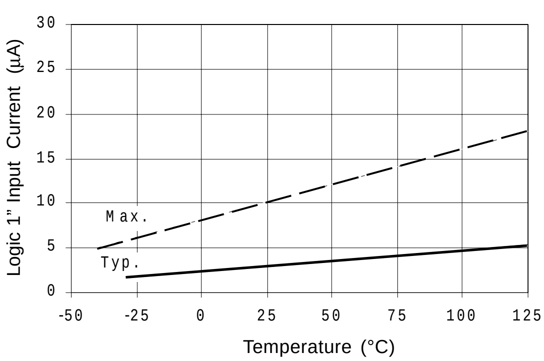


Figure 19A. Logic"1" Input Current vs Temperature

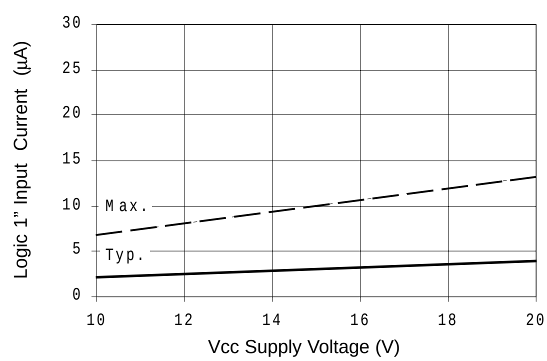


Figure 19B. Logic"1" Input Current vs Voltage

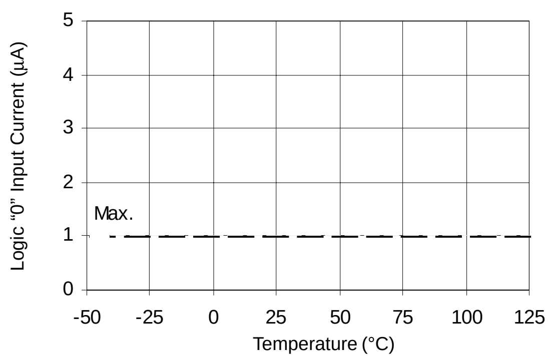


Figure 20A. Logic "0" Input Current vs Temperature

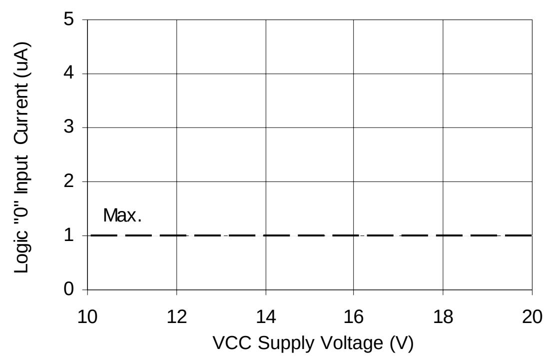


Figure 20B. Logic "0" Input Current vs Voltage

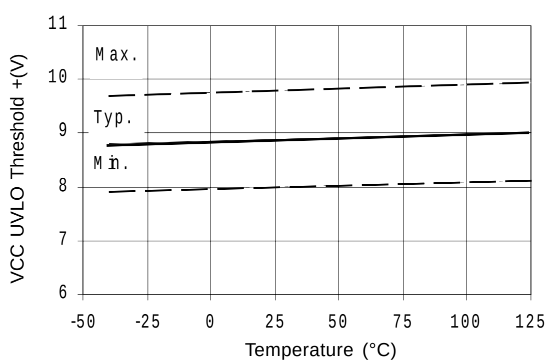


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

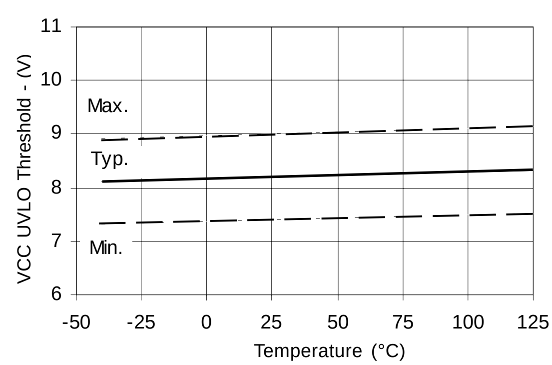


Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature

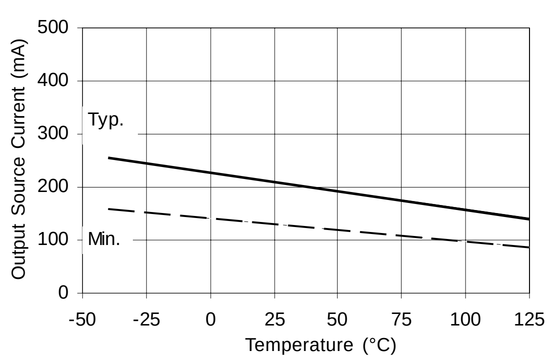


Figure 22A. Output Source Current vs Temperature

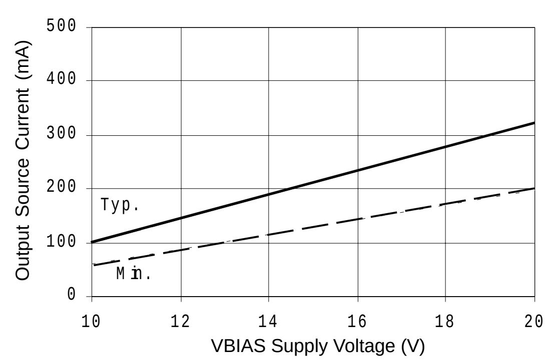


Figure 22B. Output Source Current vs Voltage

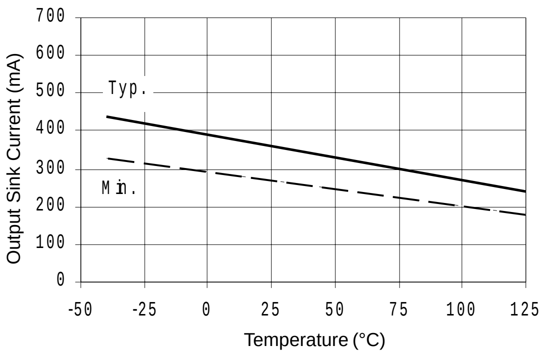


Figure 23A. Output Sink Current vs Temperature

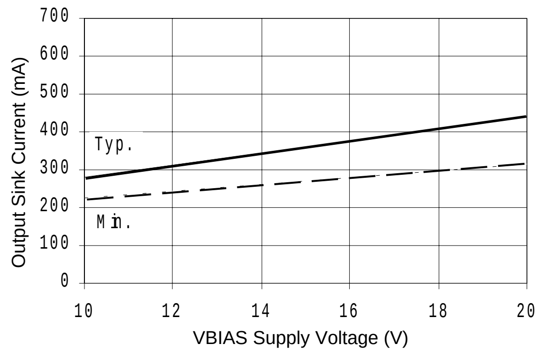
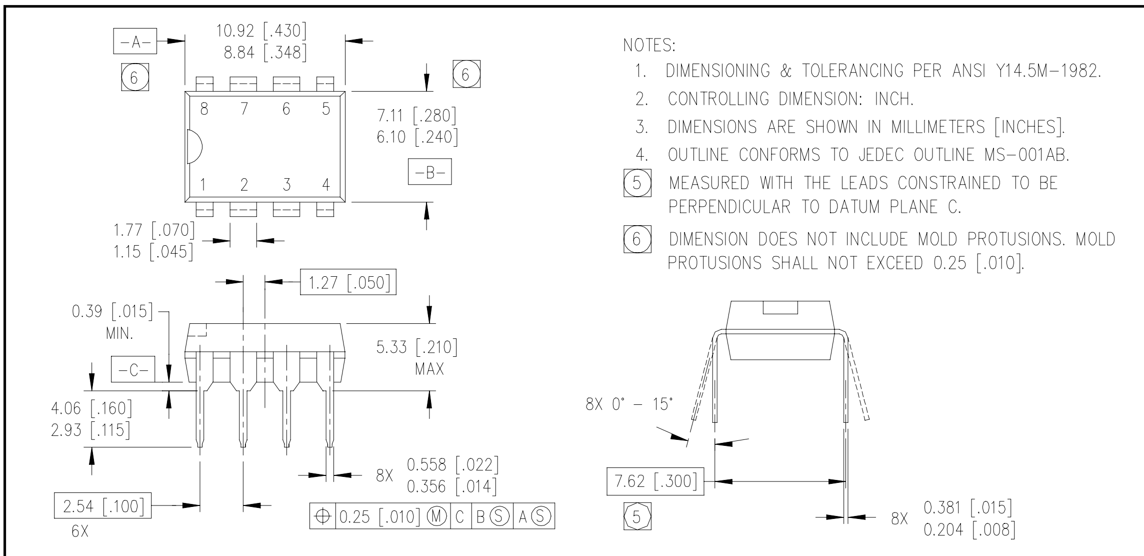


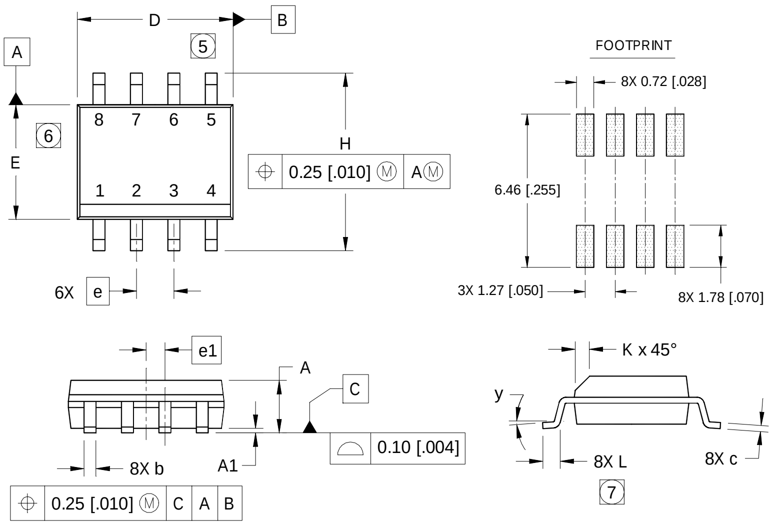
Figure 23B. Output Sink Current vs Voltage

Case Outlines



8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

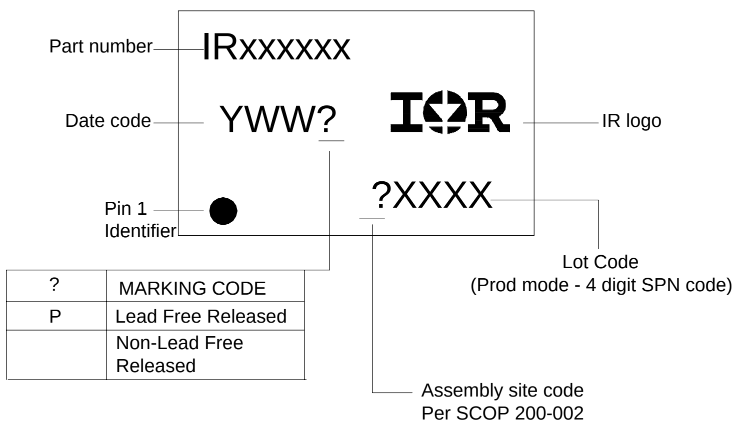
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)
8-Lead PDIP IR2104 order IR2104
8-Lead SOIC IR2104S order IR2104S

Leadfree Part
8-Lead PDIP IR2104 order IR2104PbF
8-Lead SOIC IR2104S order IR2104SPbF

International
IOR Rectifier
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
This product has been qualified per industrial level
Data and specifications subject to change without notice. 4/2/2004