Low Cost 4-Channel 1 MSPS 16-Bit ADC

AD7655*

FEATURES

4-Channel, 16-Bit Resolution ADC
2 Track-and-Hold Amplifiers Throughput:
1 MSPS (Normal Mode)
888 kSPS (Impulse Mode)
Analog Input Voltage Range: 0 V to 5 V
No Pipeline Delay
Parallel and Serial 5 V/3 V Interface
SPI®/QSPI™/MICROWIRE™/DSP Compatible
Single 5 V Supply Operation
Power Dissipation
120 mW Typical,
2.6 mW @ 10 kSPS
Package: 48-Lead Quad Flat Pack (LQFP) or
48-Lead Frame Chip Scale Pack (LFCSP)
Pin-to-Pin Compatible with the AD7654
Low Cost

APPLICATIONS

4-Channel Data Acquisition

GENERAL DESCRIPTION

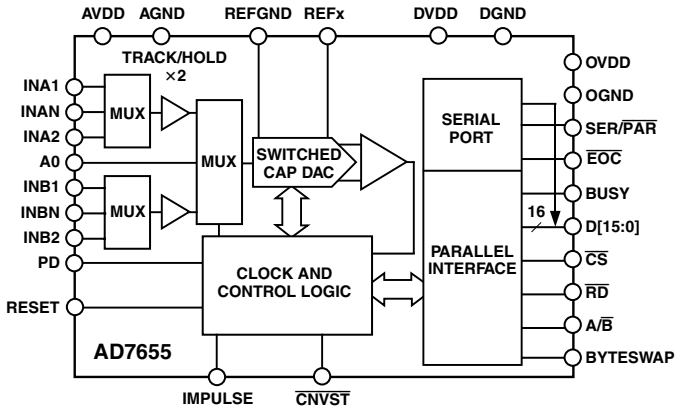
The AD7655 is a low cost, 4-channel, 16-bit, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply. It contains two low noise, wide bandwidth track-and-hold amplifiers that allow simultaneous sampling, a high speed 1 MSPS 16-bit sampling ADC, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports. Each track-and-hold has a multiplexer in front to provide a 4-channel input ADC.

The AD7655 features a very high sampling rate mode (Normal) and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput. It is available in 48-lead LQFP or 48-lead LFCSP packages with operation specified from –40°C to +85°C.

*Patent pending

REV. 0

FUNCTIONAL BLOCK DIAGRAM



PulSAR Selection

Type/kSPS	100–250	500–570	800–1000
Pseudo Differential	AD7651 AD7660/AD7661	AD7650/AD7652 AD7664/AD7666	AD7653 AD7667
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677
18-Bit	AD7678	AD7679	AD7674
Multichannel/ Simultaneous		AD7654 AD7655	

PRODUCT HIGHLIGHTS

1. Multichannel ADC
   The AD7655 features 4-channel inputs with two sample-and-hold circuits that allow simultaneous sampling.
2. Fast Throughput
   The AD7655 is a very high speed (1 MSPS in normal mode and 888 kSPS in impulse mode), charge redistribution, 16-bit SAR ADC that avoids pipeline delay.
3. Single-Supply Operation
   The AD7655 operates from a single 5 V supply and dissipates only 120 mW typical, even lower when a reduced throughput is used with the reduced power mode (Impulse) and a power-down mode.
4. Serial or Parallel Interface
   Versatile parallel or 2-wire serial interface arrangement compatible with both 3 V or 5 V logic.

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AD7655—SPECIFICATIONS (–40°C to +85°C, V_{REF} = 2.5 V, AVDD = AVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{INx} - V_{INxN}$	0		2 V_{REF}	
Common-mode Input Voltage	V_{INxN}	–0.1		+0.5	V
Analog Input CMRR	f_{IN} = 100 kHz		55		dB
Input Current	1 MSPS Throughput		45		µA
Input Impedance		See Analog Input Section			
THROUGHPUT SPEED					
Complete Cycle (2 channels)	In Normal Mode			2	µs
Throughput Rate	In Normal Mode	0		1	MSPS
Complete Cycle (2 channels)	In Impulse Mode			2.25	µs
Throughput Rate	In Impulse Mode	0		888	kSPS
DC ACCURACY					
Integral Linearity Error		–6		+6	LSB[1]
No Missing Codes		15			Bits
Transition Noise			0.8		LSB
Full-Scale Error[2]	T_{MIN} to T_{MAX}		±0.25	±0.5	% of FSR
Full-Scale Error Drift[2]			±2		ppm/°C
Unipolar Zero Error[2]	T_{MIN} to T_{MAX}			±0.25	% of FSR
Unipolar Zero Error Drift[2]			±0.8		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±0.8		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 100 kHz		86		dB[3]
Spurious Free Dynamic Range	f_{IN} = 100 kHz		98		dB
Total Harmonic Distortion	f_{IN} = 100 kHz		–96		dB
Signal-to-(Noise + Distortion)	f_{IN} = 100 kHz		86		dB
	f_{IN} = 100 kHz, –60 dB Input		30		dB
Channel-to-Channel Isolation	f_{IN} = 100 kHz		–92		dB
–3 dB Input Bandwidth			10		MHz
SAMPLING DYNAMICS					
Aperture Delay[4]			2		ns
Aperture Delay Matching[4]			30		ps
Aperture Jitter[4]			5		ps rms
Transient Response	Full-Scale Step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	AVDD/2	V
External Reference Current Drain	1 MSPS Throughput		180		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.0		OVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format		Parallel or Serial 16-Bit Straight Binary Coding			
Pipeline Delay		Conversion Results Available Immediately after Completed Conversion			
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = –500 µA	OVDD – 0.2			V

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.25		5.25[5]	V
Operating Current[6]	1 MSPS Throughput				
AVDD			15.5		mA
DVDD			8.5		mA
OVDD			100		µA
Power Dissipation	1 MSPS Throughput[6]		120	135	mW
	20 kSPS Throughput[7]		2.6		mW
	888 kSPS Throughput[7]		114	125	mW
TEMPERATURE RANGE[8]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[1]LSB means least significant bit. With the 0 V to 5 V input range, one LSB is 76.294 µV.
[2]See Definition of Specifications section. These specifications do not include the error contribution from the external reference.
[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4]Sample tested during initial release.
[5]The maximum should be the minimum of 5.25 V and DVDD + 0.3 V.
[6]In Normal Mode.
[7]In Impulse Mode.
[8]Contact factory for extended temperature range.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (–40°C to +85°C, V_{REF} = 2.5 V, AVDD = AVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figures 8 and 9					
Convert Pulsewidth	t_1	5			ns
Time Between Conversions (Normal Mode/Impulse Mode)	t_2	2/2.25			µs
$\overline{CNVST}$ LOW to BUSY HIGH Delay	t_3			32	ns
BUSY HIGH All Modes Except in Master Serial Read after Convert Mode (Normal Mode/Impulse Mode)	t_4			1.75/2	µs
Aperture Delay	t_5		2		ns
End of Conversions to BUSY LOW Delay	t_6	10			ns
Conversion Time (Normal Mode/Impulse Mode)	t_7			1.75/2	µs
Acquisition Time	t_8	250			ns
$\overline{RESET}$ Pulsewidth	t_9	10			ns
$\overline{CNVST}$ LOW to $\overline{EOC}$ HIGH Delay	t_{10}			30	ns
$\overline{EOC}$ HIGH for Channel A Conversion (Normal Mode/Impulse Mode)	t_{11}			1/1.25	µs
$\overline{EOC}$ LOW after Channel A Conversion	t_{12}	45			ns
$\overline{EOC}$ HIGH for Channel B Conversion	t_{13}			0.75	µs
Channel Selection Setup Time	t_{14}	250			ns
Channel Selection Hold Time	t_{15}			30	ns
Refer to Figures 10, 11, 12, 13, and 14 (Parallel Interface Modes)					
$\overline{CNVST}$ LOW to DATA Valid Delay	t_{16}			1.75/2	µs
DATA Valid to BUSY LOW Delay	t_{17}	14			ns
Bus Access Request to DATA Valid	t_{18}			40	ns
Bus Relinquish Time	t_{19}	5		15	ns
A/$\overline{B}$ LOW to Data Valid Delay	t_{20}			40	ns

TIMING SPECIFICATIONS (CONTINUED)

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figures 15 and 16 (Master Serial Interface Modes)					
$\overline{CS}$ LOW to SYNC Valid Delay	t_{21}			10	ns
$\overline{CS}$ LOW to Internal SCLK Valid Delay	t_{22}			10	ns
$\overline{CS}$ LOW to SDOUT Delay	t_{23}			10	ns
$\overline{CNVST}$ LOW to SYNC Delay (Read during Convert) (Normal Mode/Impulse Mode)	t_{24}		250/500		ns
SYNC Asserted to SCLK First Edge Delay*	t_{25}	3			ns
Internal SCLK Period*	t_{26}	23		40	ns
Internal SCLK HIGH*	t_{27}	12			ns
Internal SCLK LOW*	t_{28}	7			ns
SDOUT Valid Setup Time*	t_{29}	4			ns
SDOUT Valid Hold Time*	t_{30}	2			ns
SCLK Last Edge to SYNC Delay*	t_{31}	1			
$\overline{CS}$ HIGH to SYNC HI-Z	t_{32}			10	ns
$\overline{CS}$ HIGH to Internal SCLK HI-Z	t_{33}			10	ns
$\overline{CS}$ HIGH to SDOUT HI-Z	t_{34}			10	ns
BUSY HIGH in Master Serial Read after Convert (Normal Mode/Impulse Mode)	t_{35}			See Table I	
$\overline{CNVST}$ LOW to SYNC Asserted Delay (Normal Mode/Impulse Mode)	t_{36}		0.75/1		µs
SYNC Deasserted to BUSY LOW Delay	t_{37}		25		ns
Refer to Figures 17 and 18 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{38}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{39}	3		18	ns
SDIN Setup Time	t_{40}	5			ns
SDIN Hold Time	t_{41}	5			ns
External SCLK Period	t_{42}	25			ns
External SCLK HIGH	t_{43}	10			ns
External SCLK LOW	t_{44}	10			ns

*In serial master read during convert mode. See Table I for serial master read after convert mode.

Specifications subject to change without notice.

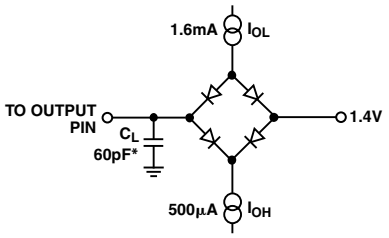
Table I. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{25}	3	17	17	17	ns
Internal SCLK Period Minimum	t_{26}	25	50	100	200	ns
Internal SCLK Period Maximum	t_{26}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{27}	12	22	50	100	ns
Internal SCLK LOW Minimum	t_{28}	7	21	49	99	ns
SDOUT Valid Setup Time Minimum	t_{29}	4	18	18	18	ns
SDOUT Valid Hold Time Minimum	t_{30}	2	4	30	80	ns
SCLK Last Edge to SYNC Delay Minimum	t_{31}	1	3	30	80	ns
Busy High Width Maximum (Normal)	t_{35}	3.25	4.25	6.25	10.75	µs
Busy High Width Maximum (Impulse)	t_{35}	3.5	4.5	6.5	11	µs

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
INAx[2], INBx[2], REFx, INxN, REFGND
AGND . . . . . –0.3 V to AVDD + 0.3 V
Ground Voltage Differences
AGND, DGND, OGND . . . . . ±0.3 V
Supply Voltages
AVDD, DVDD, OVDD . . . . . –0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD . . . . . ±7 V
DVDD to OVDD . . . . . -0.3 V to +7 V
Digital Inputs . . . . . –0.3 V to DVDD + 0.3 V
Internal Power Dissipation[3] . . . . . 700 mW
Internal Power Dissipation[4] . . . . . 2.5 W
Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) . . . . . 300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] See Analog Input section.
[3] Specification is for device in free air: 48-Lead LQFP: θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[4] Specification is for device in free air: 48-Lead LFCSP: θ_{JA} = 26°C/W.



*IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDOUT TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 60pF MAXIMUM.

Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

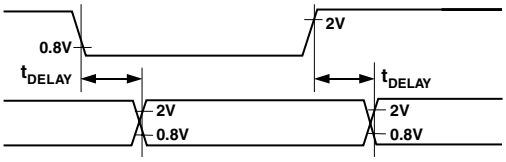


Figure 2. Voltage Reference Levels for Timing

ORDERING GUIDE

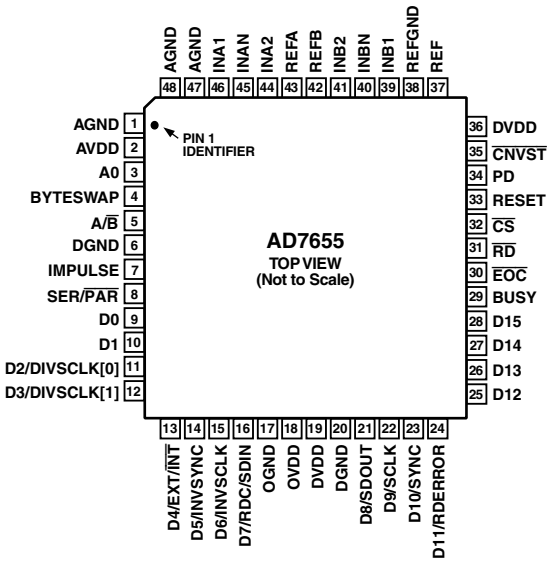
Model	Temperature Range	Package Description	Package Option
AD7655AST	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7655ASTRL	–40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7655ACP	–40°C to +85°C	Chip Scale Pack (LFCSP)	CP-48
AD7655ACPRL	–40°C to +85°C	Chip Scale Pack (LFCSP)	CP-48
EVAL-AD7655CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	

NOTES
[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 for evaluation/demonstration purposes.
[2]This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7655 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Type	Description
1, 47, 48	AGND	P	Analog Power Ground Pin.
2	AVDD	P	Input Analog Power Pin. Nominally 5 V.
3	A0	DI	Multiplexer Select. When LOW, the analog inputs INA1 and INB1 are sampled simultaneously, then converted. When HIGH, the analog inputs INA2 and INB2 are sampled simultaneously, then converted.
4	BYTESWAP	DI	Parallel Mode Selection (8-/16-Bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	A/$\overline{B}$	DI	Data Channel Selection. In parallel mode, when LOW, the data from channel B is read. When HIGH, the data from channel A is read. In serial mode, when HIGH, channel A is output first followed by channel B. When LOW, channel B is output first followed by channel A.
6, 20	DGND		Digital Power Ground Pin.
7	IMPULSE	DI	Mode Selection. When HIGH, this input selects a reduced power mode, IMPULSE. In this mode, the power dissipation is approximately proportional to the sampling rate. When LOW, the mode NORMAL is selected.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the parallel port is selected; when HIGH, the serial interface mode is selected and some bits of the DATA bus are used as a serial port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, EXT/$\overline{INT}$ is LOW and RDC/SDIN is LOW which is the serial master read after convert mode, these inputs, part of the serial port, are used to slow down if desired the internal serial clock which clocks the data output. In the other serial modes, these inputs are not used.
13	D[4] or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock, called respectively, master and slave mode. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D[5] or INVSYNC	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Type	Description
15	D[6] or INVSCLK	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 6 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	D[7] or RDC/SDIN	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/$\overline{\text{INT}}$. When EXT/$\overline{\text{INT}}$ is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 32 SCLK periods after the initiation of the read sequence. When EXT/$\overline{\text{INT}}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the previous data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3 V).
19, 36	DVDD	P	Digital Power. Nominally at 5 V.
21	D[8] or SDOUT	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in a 32-bit on-chip register. The AD7655 provides the two conversion results, MSB first, from its internal shift register. The order of channel outputs is controlled by A/$\overline{\text{B}}$. In serial mode, when EXT/$\overline{\text{INT}}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when EXT/$\overline{\text{INT}}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D[9] or SCLK	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 9 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D[10] or SYNC	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 10 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{\text{INT}}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and frames SDOUT. After the first channel is output, SYNC is pulsed LOW. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid. After the first channel is output, SYNC is pulsed HIGH.
24	D[11] or RDERROR	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 11 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH and EXT/$\overline{\text{INT}}$ is HIGH, this output, part of the serial port, is used as a incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25–28	D[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, these outputs are in high impedance.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the two conversions are complete and the data are latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	$\overline{\text{EOC}}$	DO	End of Convert Output. Going low at each channel conversion.
31	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{\text{CS}}$	DI	Chip Select. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{\text{CS}}$ is also used to gate the external serial clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7655. Current conversion if any is aborted. If not used, this pin could be tied to DGND.

PIN FUNCTION DESCRIPTIONS (continued)

Pin Number	Mnemonic	Type	Description
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample/hold into the hold state and initiates a conversion. In impulse mode (IMPULSE HIGH), if $\overline{\text{CNVST}}$ is held low when the acquisition phase (t_8) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
37	REF	AI	This input pin is used to provide a reference to the converter.
38	REFGND	AI	Reference Input Analog Ground
39, 41	INB1, INB2	AI	Analog Inputs
42, 43	REFB, REFA	AI	These inputs are the references applied to Channel A and Channel B, respectively.
40, 45	INBN, INAN	AI	Analog input ground senses. Allow to sense each channel ground independently.
44, 46	INA2, INA1	AI	Analog Inputs

NOTES
AI = Analog Input
DI = Digital Input
DI/O = Bidirectional Digital
DO = Digital Output
P = Power

DEFINITION OF SPECIFICATIONS

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error
The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Unipolar Zero Error
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. The unipolar zero error is the deviation of the actual transition from that point.

Spurious Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to *S*/(*N*+*D*) by the following formula:

$$ENOB = \left(S / \left[N + D\right]_{dB} - 1.76\right) / 6.02\right)$$

and is expressed in bits.

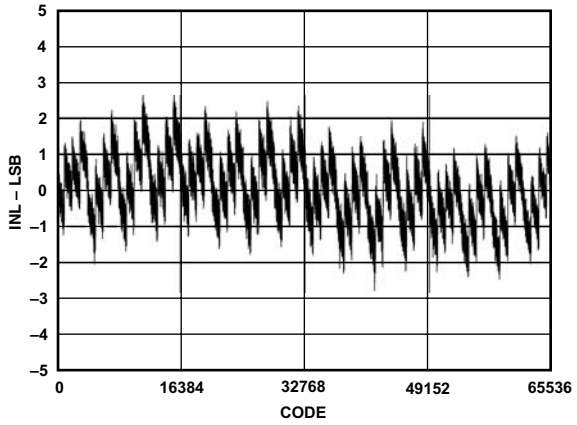
Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

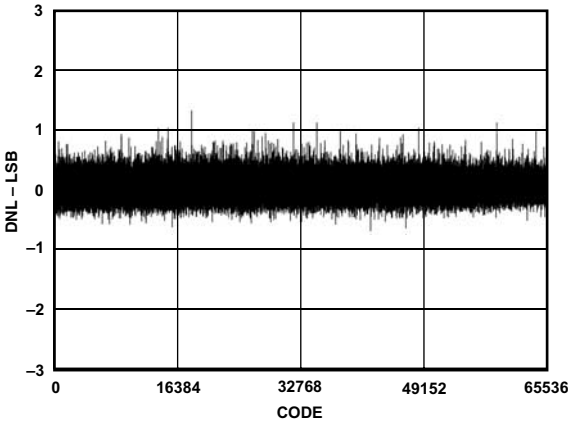
Signal-to-(Noise + Distortion) Ratio (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

Aperture Delay
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signals are held for a conversion.

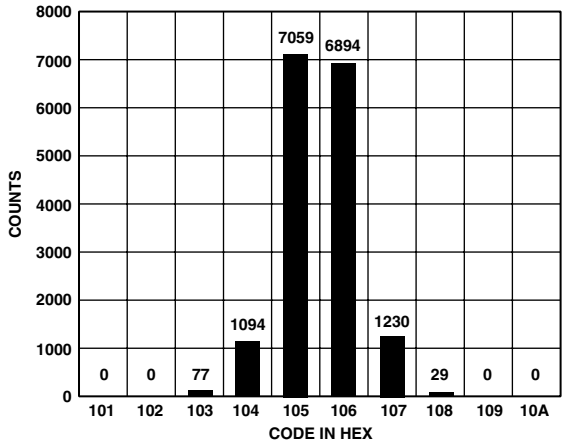
Transient Response
The time required for the AD7655 to achieve its rated accuracy after a full-scale step function is applied to its input.



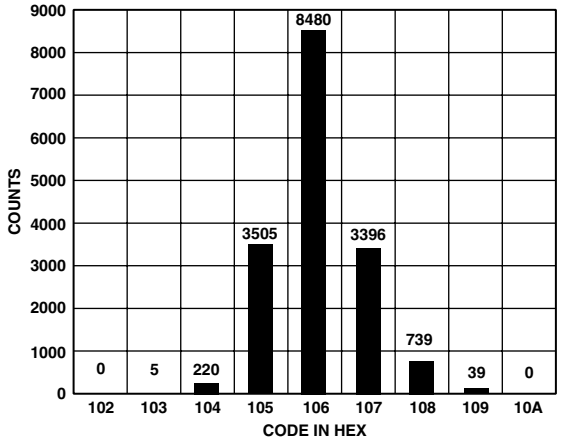
TPC 1. Integral Nonlinearity vs. Code



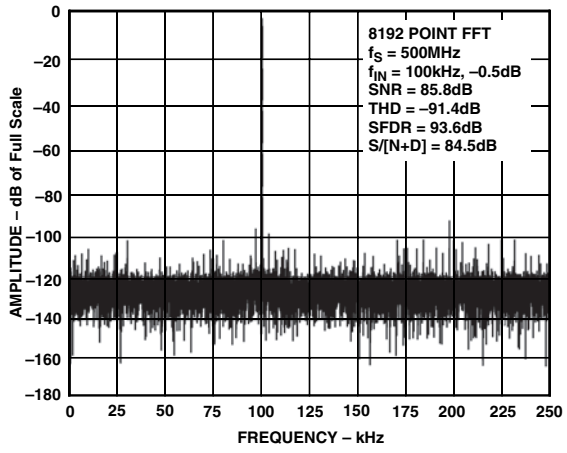
TPC 4. Differential Nonlinearity vs. Code



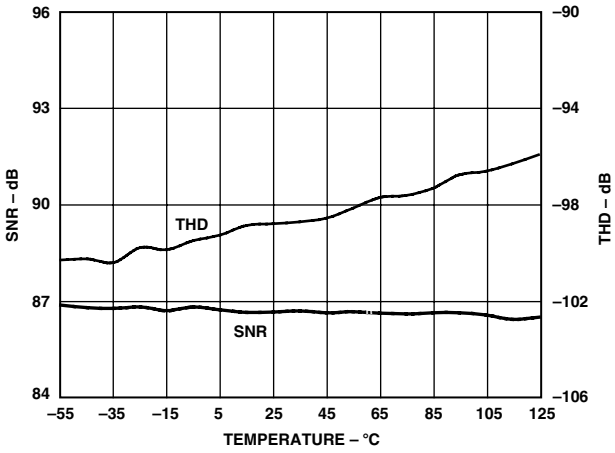
TPC 2. Histogram of 16,384 Conversions of a DC Input at the Code Transition



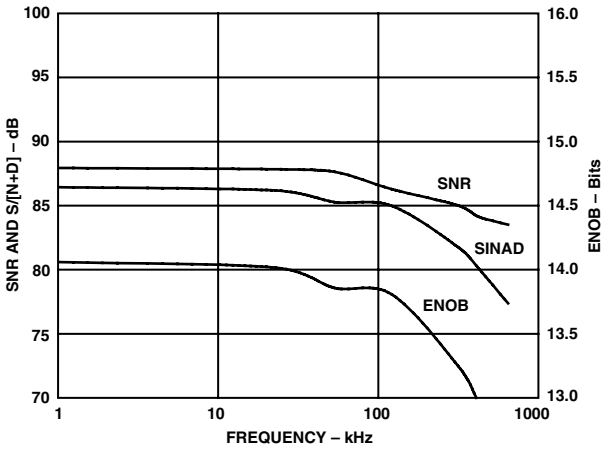
TPC 5. Histogram of 16,384 Conversions of a DC Input at the Code Center



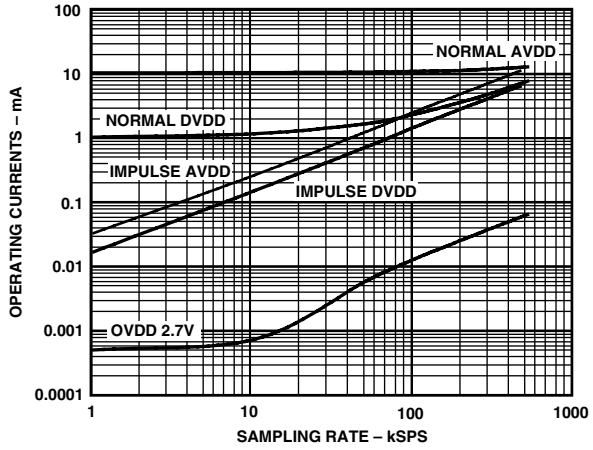
TPC 3. FFT Plot



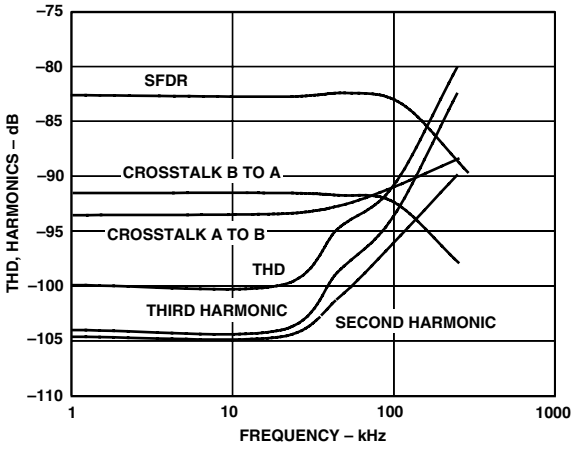
TPC 6. SNR, THD vs. Temperature



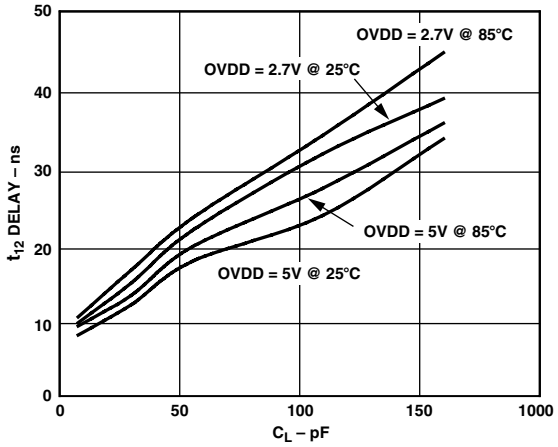
TPC 7. SNR, S/(N+D), and ENOB vs. Frequency



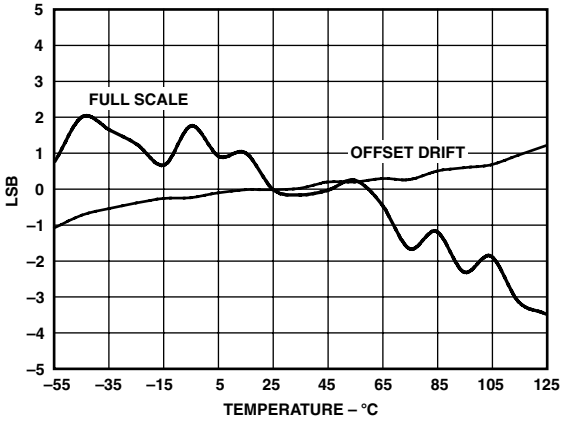
TPC 10. Operating Currents vs. Sample Rate



TPC 8. THD, Harmonics, Crosstalk and SFDR vs. Frequency



TPC 11. Typical Delay vs. Load Capacitance C_L



TPC 9. Full Scale and Zero Error vs. Temperature

CIRCUIT INFORMATION

The AD7655 is a very fast, low power, single-supply, precise 4-channel 16-bit analog-to-digital converter (ADC).

The AD7655 provides the user with two on-chip track-and-hold, successive approximation ADCs that do not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7655 can be operated from a single 5 V supply and can be interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP or in a tiny 48-lead LFCSP package that combines space savings and allows flexible configurations as either serial or parallel interface. The AD7655 is pin-to-pin compatible with PulSAR ADCs.

Modes of Operation

The AD7655 features two modes of operation, normal and impulse. Each of these modes is more suitable for specific applications.

The normal mode is the fastest mode (1 MSPS). Except when it is powered down (PD HIGH), the power dissipation is almost independent of the sampling rate.

The impulse mode, the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 888 kSPS. When operating at 20 kSPS, for example, it typically consumes only 2.6 mW. This feature makes the AD7655 ideal for battery-powered applications.

Transfer Functions

The AD7655 data format is straight binary. The ideal transfer characteristic for the AD7655 is shown in Figure 3 and Table II.

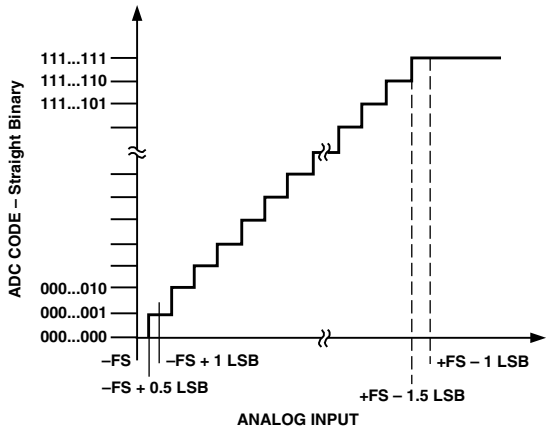


Figure 3. ADC Ideal Transfer Function

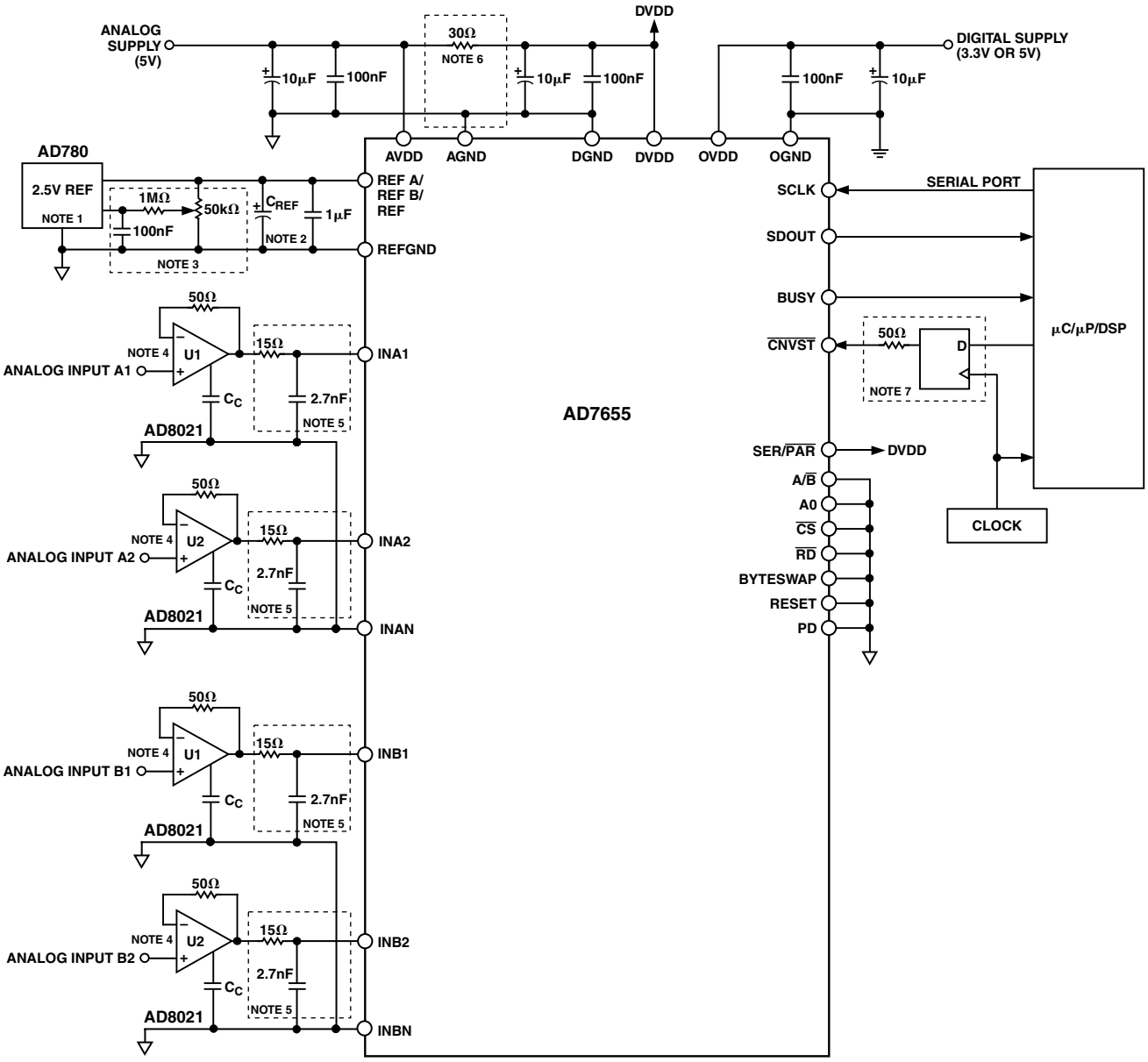
Table II. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 2.5 V	Digital Output Code (Hex)
FSR –1 LSB	4.999924 V	FFFF[1]
FSR – 2 LSB	4.999847 V	FFFE
Midscale + 1 LSB	2.500076 V	8001
Midscale	2.5 V	8000
Midscale – 1 LSB	2.499924 V	7FFF
–FSR + 1 LSB	–76.29 μV	0001
–FSR	0 V	0000[2]

NOTES

[1]This is also the code for overrange analog input ($V_{INx} - V_{INxN}$ above $2 \times (V_{REF} - V_{REFGND})$).

[2]This is also the code for underrange analog input (V_{INx} below V_{INxN}).



NOTES
1. SEE VOLTAGE REFERENCE INPUT SECTION.
2. WITH THE RECOMMENDED VOLTAGE REFERENCES, C_{REF} IS 47μF. SEE VOLTAGE REFERENCE INPUT SECTION.
3. OPTIONAL CIRCUITRY FOR HARDWARE GAIN CALIBRATION.
4. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
5. SEE ANALOG INPUTS SECTION.
6. OPTION, SEE POWER SUPPLY SECTION.
7. OPTIONAL LOW JITTER $\overline{CNVST}$. SEE CONVERSION CONTROL SECTION.

Figure 4. Typical Connection Diagram (Serial Interface)

TYPICAL CONNECTION DIAGRAM

Figure 4 shows a typical connection diagram for the AD7655. Different circuitry shown on this diagram is optional and is discussed below.

Analog Inputs

Figure 5 shows a simplified analog input section of the AD7655.

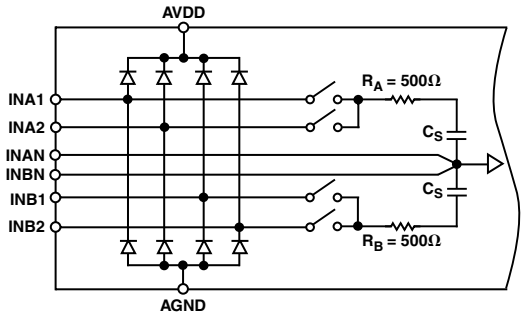


Figure 5. Simplified Analog Input

The diodes shown in Figure 5 provide ESD protection for the inputs. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. This condition could eventually occur when the input buffer's (U1) or (U2) supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

This analog input structure allows the sampling of the differential signal between INx and INxN. Unlike other converters, the INxN is sampled at the same time as the INx input. By using these differential inputs, small signals common to both inputs are rejected.

During the acquisition phase, for ac signals, the AD7655 behaves like a one-pole RC filter consisting of the equivalent resistance R_A, R_B, and C_S. The resistors R_A and R_B are typically 500 Ω and are a lumped component made up of some serial resistance and the on resistance of the switches. The capacitor C_S is typically 32 pF and is mainly the ADC sampling capacitor. This one-pole filter with a typical –3 dB cutoff frequency of 10 MHz reduces undesirable aliasing effects and limits the noise coming from the inputs.

Because the input impedance of the AD7655 is very high, the AD7655 can be driven directly by a low impedance source without gain error. As shown in Figure 4, that allows an external one-pole RC filter between the output of the amplifier output and the ADC analog inputs to even further improve the noise filtering done by the AD7655 analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD degrades with the increase of the source impedance.

Driver Amplifier Choice

Although the AD7655 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7655 analog input circuit have to be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, the settling at 0.1% or 0.01% is more commonly specified. It could significantly differ from the settling time at a 16-bit level and, therefore, it should be verified prior to the driver selection. The tiny op amp AD8021, which combines ultra-low noise and a high gain bandwidth, meets this settling time requirement even when used with a high gain of up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7655. The noise coming from the driver is filtered by the AD7655 analog input circuit one-pole low-pass filter made by R_A, R_B, and C_S.
- The driver needs to have a THD performance suitable to that of the AD7655.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where a dual version is needed and a gain of 1 is used.

The AD829 is another alternative where high frequency (above 100 kHz) performance is not required. In a gain of 1, it requires an 82 pF compensation capacitor.

The AD8610 is also an option where low bias current is needed in low frequency applications.

Voltage Reference Input

The AD7655 requires an external 2.5 V reference. The reference input should be applied to REF, REFA for Channel A, and to REFB for Channel B. The voltage reference input REF of the AD7655 has a dynamic input impedance; it should therefore be driven by a low impedance source with an efficient decoupling. This decoupling depends on the choice of the voltage reference but usually consists of a 1 μF ceramic capacitor and a low ESR tantalum capacitor connected to the REFA, REFB, and REFGND inputs with minimum parasitic inductance. 47 μF is an appropriate value for the tantalum capacitor when using one of the recommended reference voltages:

- The low noise, low temperature drift AD780 voltage reference
- The low cost AD1582 voltage reference

For applications using multiple AD7655s, it is more effective to buffer the reference voltage using the internal buffer. Each ADC should be decoupled individually.

Care should also be taken with the reference temperature coefficient of the voltage reference, which directly affects the full-scale accuracy if this parameter is applicable. For instance, a ±15 ppm/°C tempco of the reference changes the full scale by ±1 LSB/°C.

Power Supply

The AD7655 uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.7 V and DVDD + 0.3 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply, as shown in Figure 5. The AD7655 is independent of power supply sequencing, once OVDD does not exceed DVDD by more than 0.3 V, and thus is free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 6.

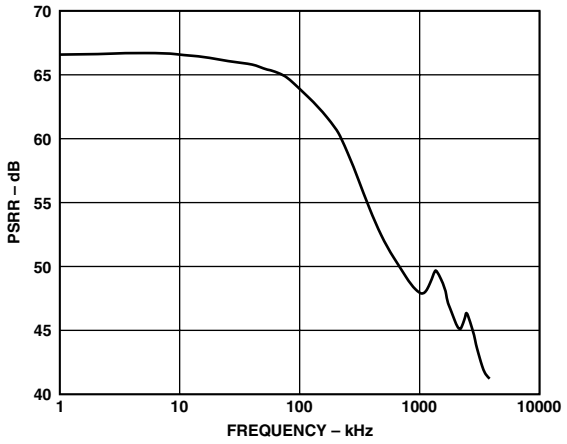


Figure 6. PSRR vs. Frequency

POWER DISSIPATION

In impulse mode, the AD7655 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows significant power savings when the conversion rate is reduced, as shown in Figure 7. This feature makes the AD7655 ideal for very low power battery applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (i.e., DVDD and DGND) and OVDD should not exceed DVDD by more than 0.3 V.

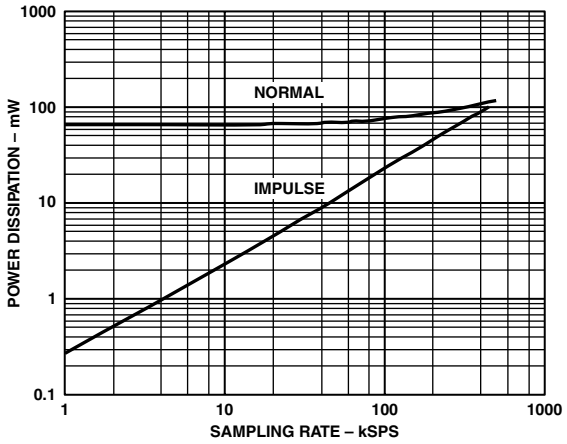


Figure 7. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 8 shows the detailed timing diagrams of the conversion process. The AD7655 is controlled by the signal $\overline{\text{CNVST}}$, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. The A0 signal is the MUX select signal that chooses which input signal is to be sampled. When high, INx1 is chosen and when low, INx2 is chosen, where x is either A or B. It should be noted that this signal should not be changed during the acquisition phase of the converter.

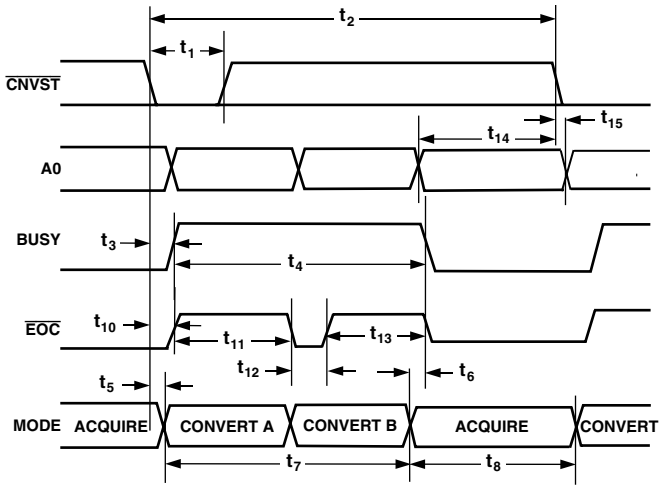


Figure 8. Conversion Control

In impulse mode, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held low when BUSY is low, the AD7655 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ low, the AD7655 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, $\overline{\text{CNVST}}$ should be brought low once to initiate the conversion process. In this mode, the AD7655 could sometimes run slightly faster than the guaranteed limits in the impulse mode of 888 kSPS. This feature does not exist in normal mode.

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges and levels, and with minimum overshoot and undershoot or ringing.

For applications where the SNR is critical, the $\overline{\text{CNVST}}$ signal should have a very low jitter. Some solutions to achieve this are to use a dedicated oscillator for $\overline{\text{CNVST}}$ generation or, at least, to clock it with a high frequency low jitter clock, as shown in Figure 4.

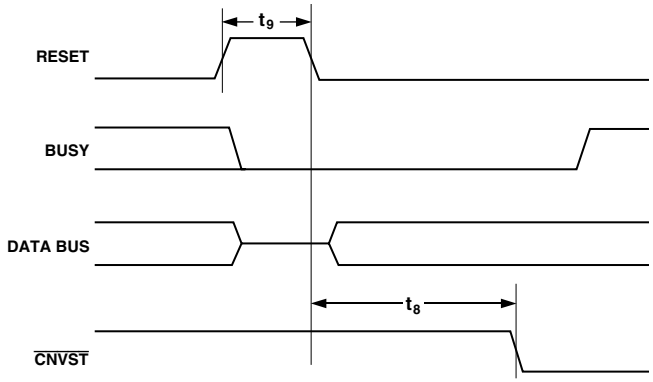


Figure 9. Reset Timing

DIGITAL INTERFACE

The AD7655 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7655 digital interface also accommodates either 3 V or 5 V logic by simply connecting the OVDD supply pin of the AD7655 to the host system interface digital supply.

Signals $\overline{CS}$ and $\overline{RD}$ control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7655 in multicircuit applications and is held low in a single AD7655 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus. In parallel mode, signal A/$\overline{B}$ allows the choice of reading either the output of Channel A or Channel B, whereas in serial mode, signal A/$\overline{B}$ controls which channel is output first.

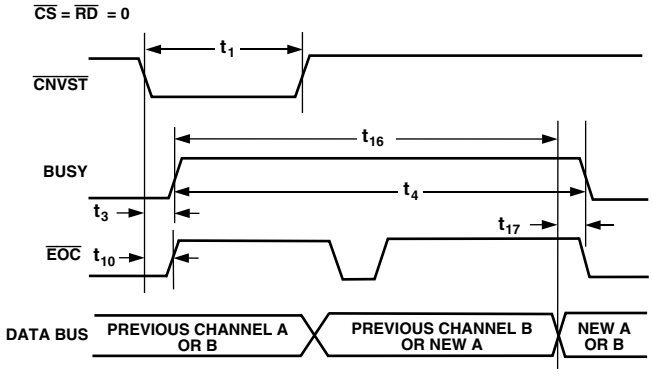


Figure 10. Master Parallel Data Timing for Reading (Continuous Read)

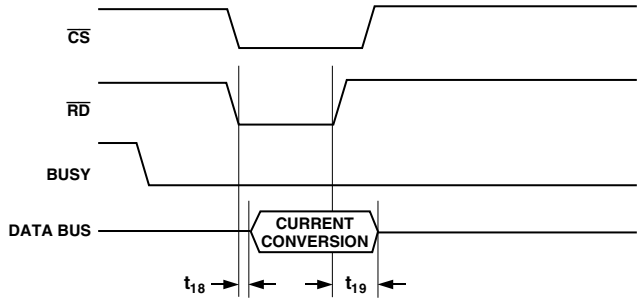


Figure 11. Slave Parallel Data Timing for Reading (Read after Convert)

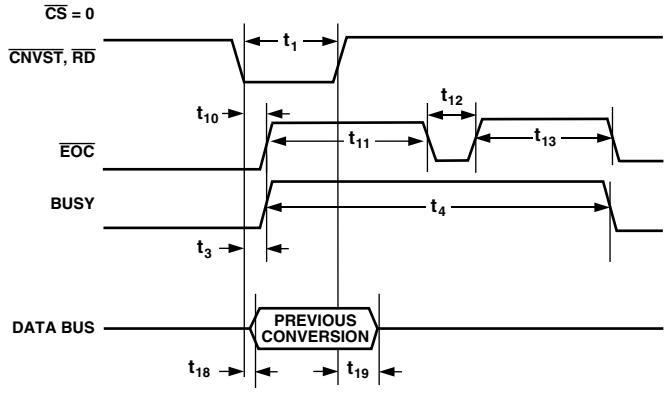


Figure 12. Slave Parallel Data Timing for Reading (Read during Convert)

PARALLEL INTERFACE

The AD7655 is configured to use the parallel interface (Figure 10) when SER/$\overline{PAR}$ is held low. The data can be read either after each conversion, which is during the next acquisition phase or during the other channel's conversion, or during the following conversion as shown, respectively, in Figures 11 and 12. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. That avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 13, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is low. When BYTESWAP is high, the LSB and MSB bytes are swapped, the LSB is output on D[15:8], and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16-bit data can be read in two bytes on either D[15:8] or D[7:0].

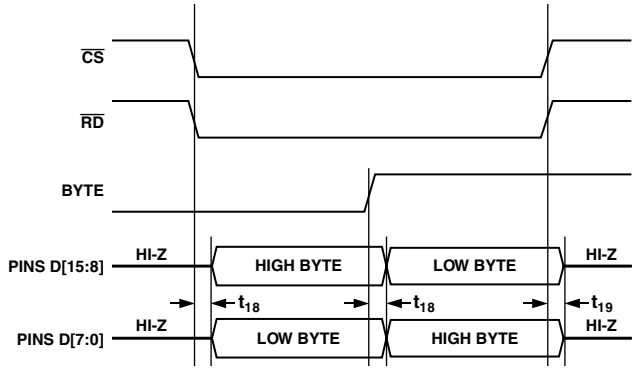


Figure 13. 8-Bit Parallel Interface

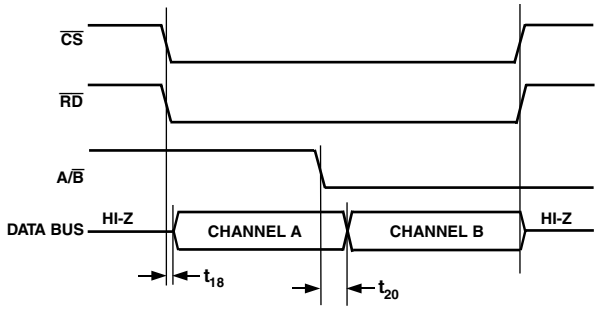


Figure 14. A/$\overline{B}$ Channel Reading

The detailed functionality of A/$\overline{B}$ is explained in Figure 14. When high, the data from Channel A is available on the data bus. When low, the data bus now carries output from Channel B. Note that Channel A can be read immediately after conversion is done ($\overline{EOC}$), while Channel B is still in its converting phase.

SERIAL INTERFACE

The AD7655 is configured to use the serial interface when SER/$\overline{PAR}$ is held high. The AD7655 outputs 32 bits of data, MSB first, on the SDOUT pin. The order of the channels being output is controlled by A/$\overline{B}$. When HIGH, Channel A is output first; when LOW, Channel B is output first. Unlike in parallel mode, Channel A data is updated only after Channel B conversion. This data is synchronized with the 32 clock pulses provided on the SCLK pin.

MASTER SERIAL INTERFACE

Internal Clock

The AD7655 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7655 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired.

The output data is valid on both the rising and falling edge of the data clock. Depending on RDC/SDIN input, the data can be read after each conversion or during the following conversion.

Figures 15 and 16 show the detailed timing diagrams of these two modes.

Usually, because the AD7655 is used with a fast throughput, the mode master, read during conversion is the most recommended serial mode when it can be used.

In read after conversion mode, it should be noted that unlike in other modes, the signal BUSY returns low after the 32 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width. One advantage of this mode is

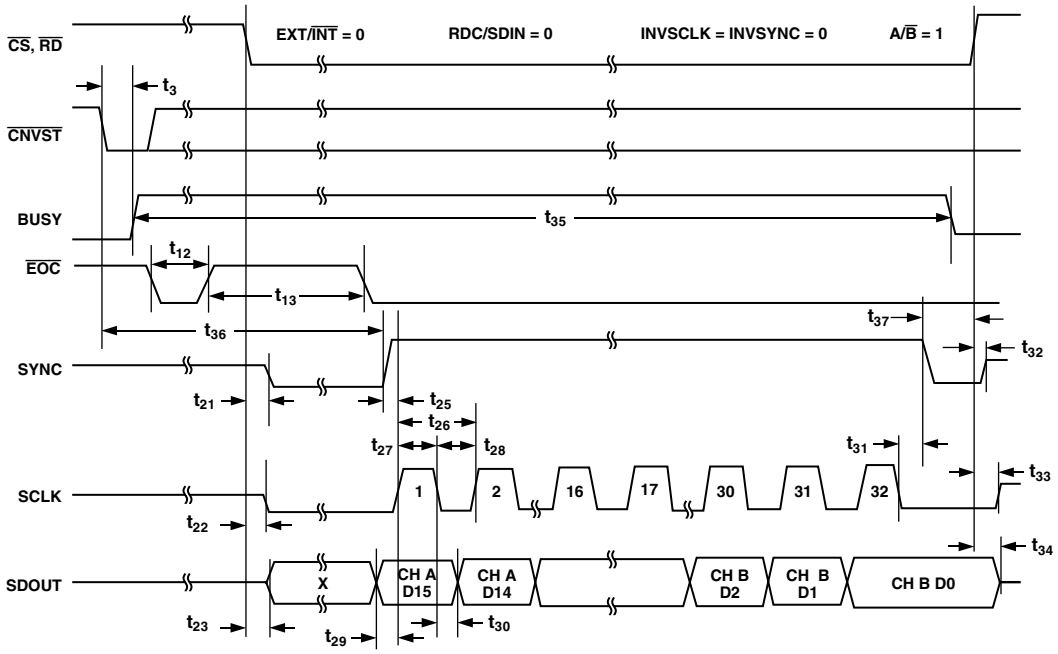


Figure 15. Master Serial Data Timing for Reading (Read after Convert)

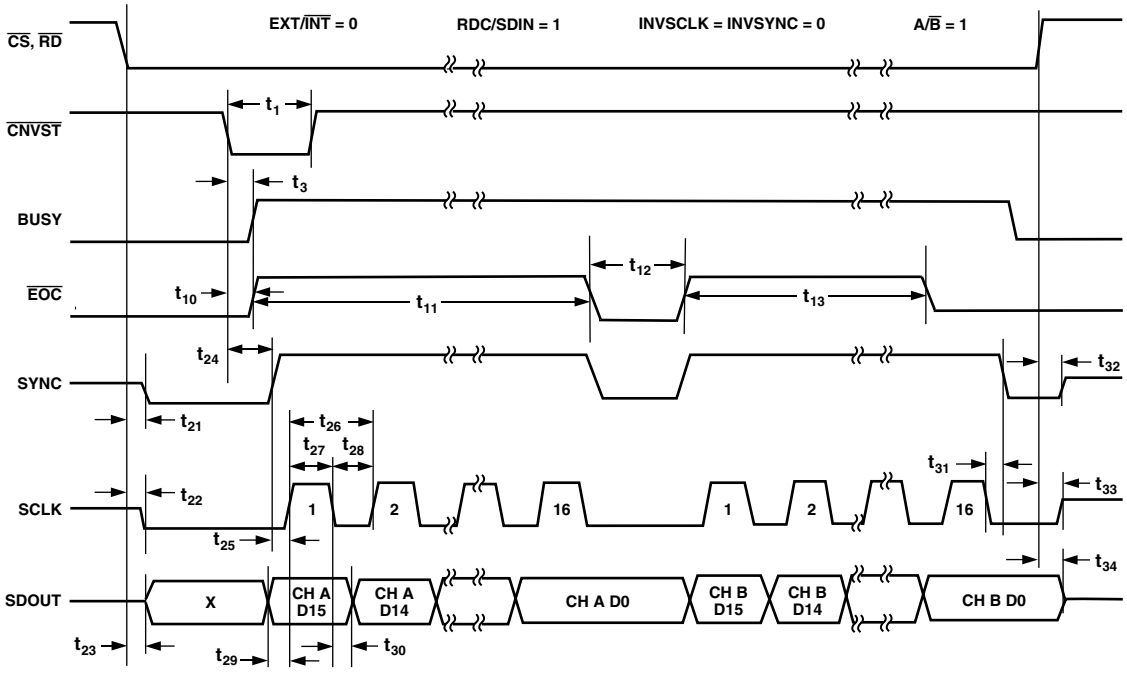


Figure 16. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

that it can accommodate slow digital hosts because the serial clock can be slowed down by using DIVSCLK.

In read during conversion mode, the serial clock and data toggle at appropriate instants, which minimizes potential feedthrough between digital activity and the critical conversion decisions. The SYNC signal goes low after the LSB of each channel has been output.

SLAVE SERIAL INTERFACE

External Clock

The AD7655 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{INT}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS}$ and the data are output when both $\overline{CS}$ and $\overline{RD}$ are low. Thus, depending on $\overline{CS}$, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figures 17 and 18 show the detailed timing diagrams of these methods.

While the AD7655 is performing a bit decision, it is important that voltage transients do not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase of each channel because the AD7655 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of $\overline{EOC}$ high.

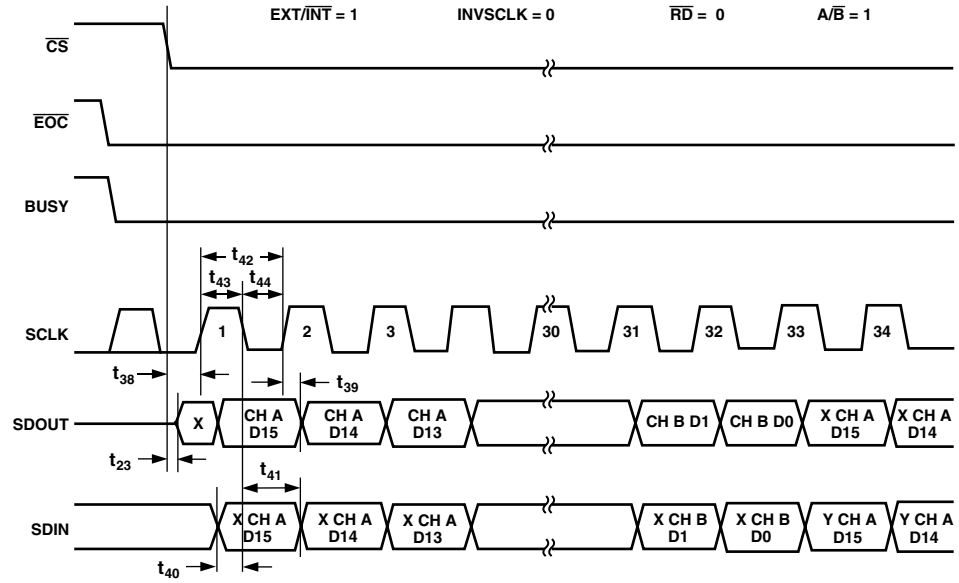


Figure 17. Slave Serial Data Timing for Reading (Read after Convert)

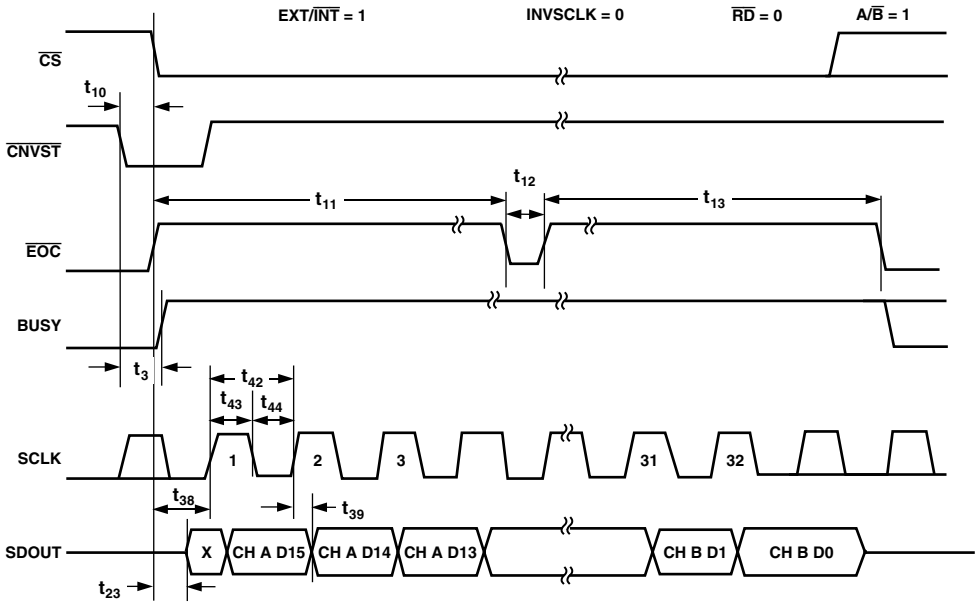


Figure 18. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

External Discontinuous Clock Data Read after Conversion
This mode is the most recommended of the serial slave modes. Figure 18 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the results of this conversion can be read while both $\overline{CS}$ and $\overline{RD}$ are low. The data from both channels are shifted out, MSB first, with 32 clock pulses and are valid on both the rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

Another advantage is to be able to read the data at any speed up to 40 MHz, which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7655 provides a daisy-chain feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when it is desired, as it is for instance in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 19. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the opposite edge of SCLK of the one used to shift out the data on SDOUT. Therefore, the MSB of the upstream converter follows the LSB of the downstream converter on the next SCLK cycle.

External Clock Data Read during Conversion
Figure 18 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 32 clock pulses, and is valid on both rising and falling edges of the clock. The 32 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode, and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated.

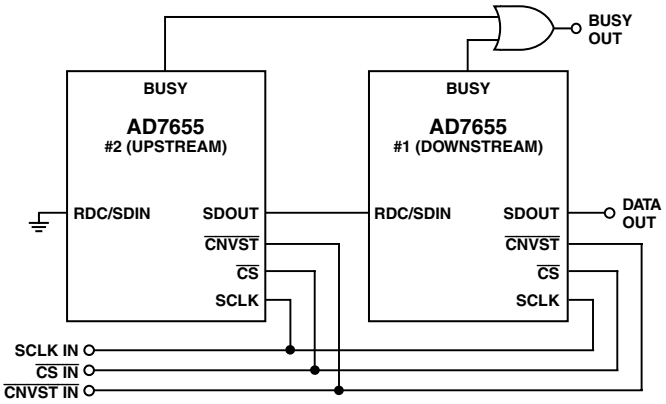


Figure 19. Two AD7655s in a Daisy-Chain Configuration

MICROPROCESSOR INTERFACING
The AD7655 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7655 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7655 to prevent digital noise from coupling into the ADC. The following section illustrates the use of the AD7655 with an SPI equipped DSP, the ADSP-219x.

SPI Interface (ADSP-219x)

Figure 20 shows an interface diagram between the AD7655 and an SPI equipped DSP, ADSP-219x. To accommodate the slower speed of the DSP, the AD7655 acts as a slave device and data must be read after conversion. This mode also allows the daisy chain feature. The convert command could be initiated in response to an internal timer interrupt. The 32-bit output data are read with two SPI 16-bit wide access. The reading process could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The serial peripheral interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, clock phase bit (CPHA) = 1 by writing to the SPI control register (SPICLTx).

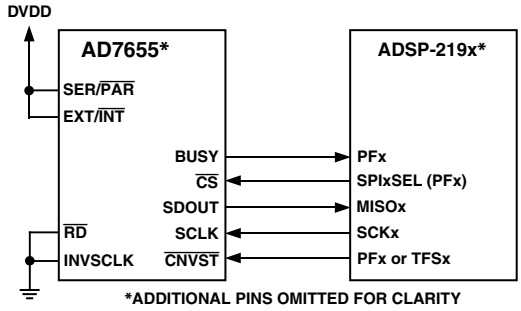


Figure 20. Interfacing the AD7655 to SPI Interface

APPLICATION HINTS

Layout

The AD7655 has very good immunity to noise on the power supplies, as seen in Figure 5. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7655 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7655, or at least as close as possible to the AD7655. If the AD7655 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7655.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7655 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board. The power supply lines to the AD7655 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supply's impedance presented to the AD7655 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supply's pins, AVDD, DVDD, and OVDD close to and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7655 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if there is no separate supply available to connect the DVDD digital supply to the analog supply AVDD through an RC filter, as shown in Figure 5, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7655 has four different ground pins: REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

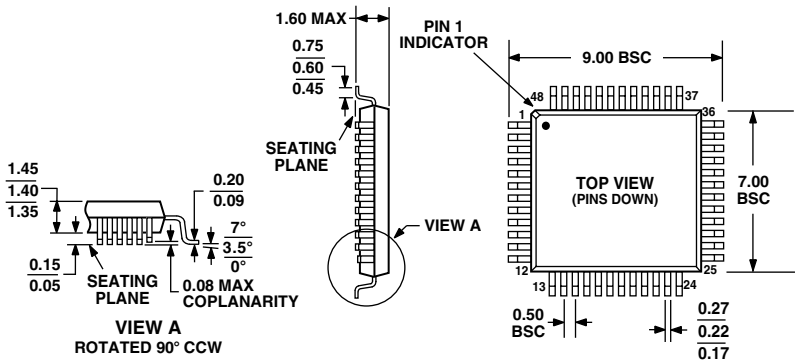
Evaluating the AD7655 Performance

A recommended layout for the AD7655 is outlined in the documentation of the evaluation board for the AD7655. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control BRD2.

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
1.4 mm Thick
(ST-48)

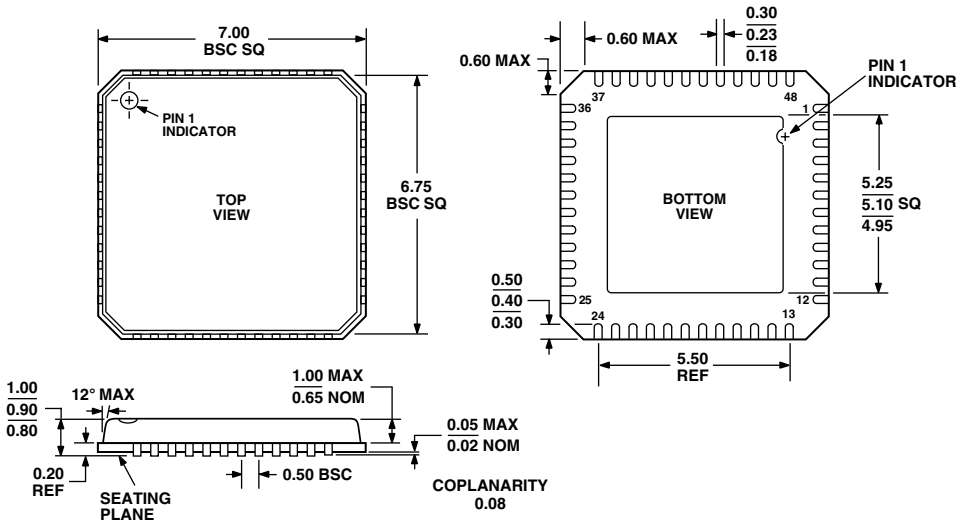
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

48-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2