Low-Voltage Sub-Ohm SPST/SPDT MICRO FOOT® Analog Switch

FEATURES

- MICRO FOOT Chip Scale Package (1.0 x 1.5 mm)
- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 0.4 Ω
- Fast Switching - t_{ON} : 47 ns, t_{OFF}: 40 ns
- Low Power Consumption
- TTL/CMOS Compatible

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- PCM Cards
- PDA

DESCRIPTION

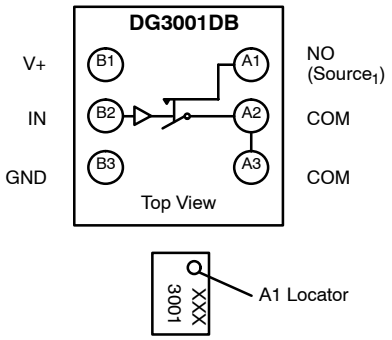
The DG3001/DG3002/DG3003 are monolithic CMOS analog switches designed for high performance switching of analog signals. The DG3001 and DG3002 are configured as SPST switches, and the DG3003 is an SPDT switch. Combining low power, high speed (t_{ON}: 47 ns, t_{OFF}: 40 ns), low on-resistance ($r_{DS(on)}$: 0.4 Ω) and small physical size (MICRO FOOT, 6-bump), the DG3001/DG3002/DG3003 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG3001/DG3002/DG3003 are built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

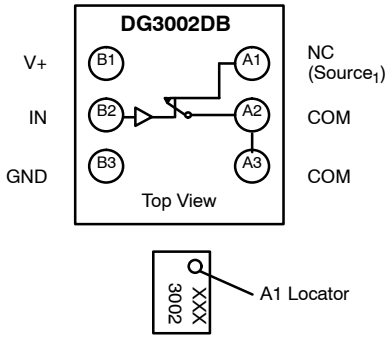
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

MICRO FOOT (6-Bump)



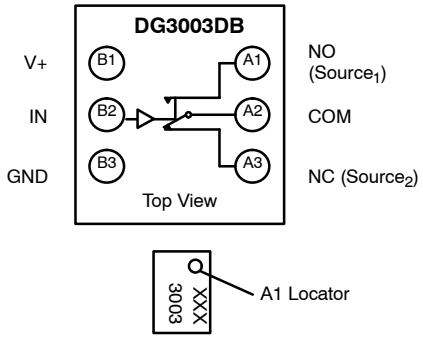
Device Marking: 3001
xxx = Date/Lot Traceability Code

MICRO FOOT (6-Bump)



Device Marking: 3002
xxx = Date/Lot Traceability Code

MICRO FOOT (6-Bump)



Device Marking: 3003
xxx = Date/Lot Traceability Code

TRUTH TABLE		
Logic	**NC**	**NO**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	MICRO FOOT: 6-Bump (3 × 2, 0.5-mm pitch, 165-µm nom. bump height)	DG3001DB
		DG3002DB
		DG3003DB

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ ..... -0.3 to +6 V
IN, COM, NC, NO[a] ..... -0.3 to (V+ + 0.3 V)
Continuous Current (NO, NC, COM) ..... ±250 mA
Peak Current ..... ±400 mA
(Pulsed at 1 ms, 10% duty cycle)
Storage Temperature (D Suffix) ..... -65 to 150°C

Package Reflow Conditions[b]
VPR ..... 215°C
IR/Convection ..... 220°C

Power Dissipation (Packages)[c]
6-Bump, 2 x 3 MICRO FOOT[d] ..... 250 mW

Notes:
a Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b Refer to IPC/JEDEC (J-STD-020A)
c All bumps soldered to PC Board.
d Derate 3.1 mW/°C above 70°C

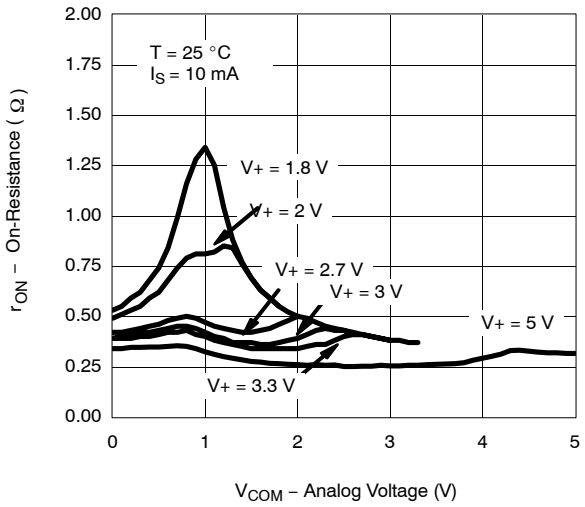
SPECIFICATIONS (V+ = 3.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance[d]	r_{ON}	V+ = 2.7 V, V_{COM} = 1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		0.4	0.7 0.8	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 2.7 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room		0.1	0.2	
r_{ON} Match[d]	Δr_{ON}		Room		0.01	0.05	
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V	Room Full	1 −10		1 10	nA
	$I_{COM(off)}$		Room Full	1 −10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	1 −10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}		Full		5		pF
Input Current[d]	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	−1		1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF Figure 1 and 2	Room Full		47	71	ns
Turn-Off Time[d]	t_{OFF}		Room Full		40	59	
Break-Before-Make Time[d]	t_d		Room	1	6		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		64		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room		−70		dB
Crosstalk[d]	X_{TALK}		Room		−70		
NO, NC Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		100		pF
Channel-On Capacitance[d]	C_{ON}		Room		340		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current[d]	I+	V_{IN} = 0 or V+			0.1	1.0	µA

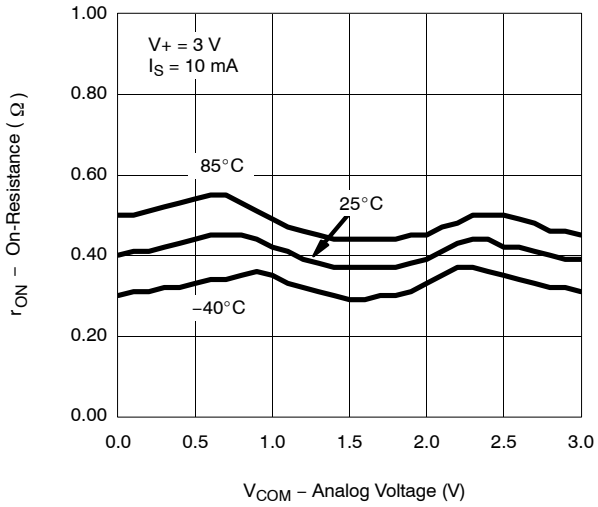
Notes:
a. Room = 25°C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

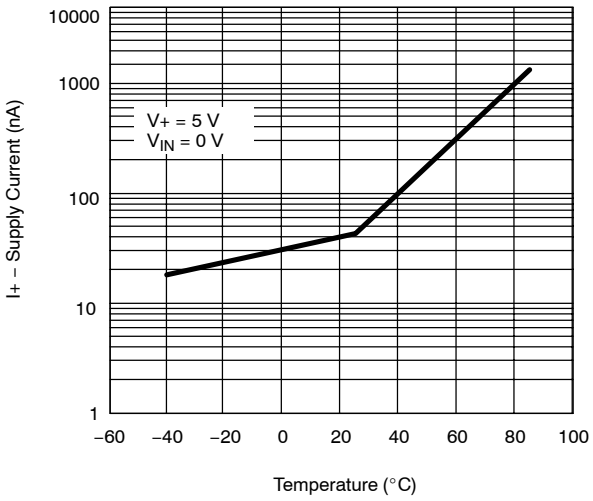
r_{ON} vs. V_{COM} and Single Supply Voltage



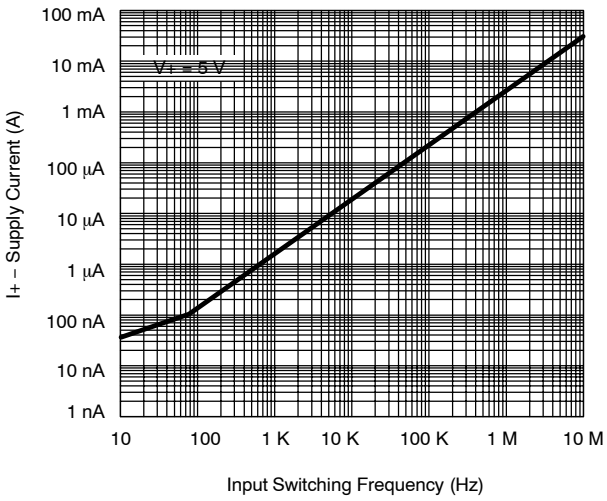
r_{ON} vs. Analog Voltage and Temperature



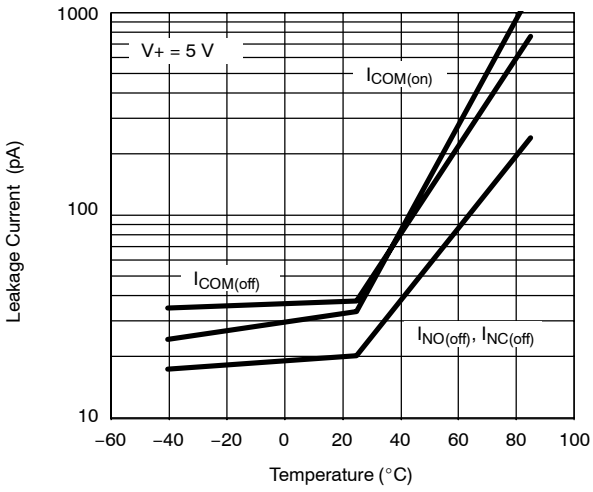
Supply Current vs. Temperature



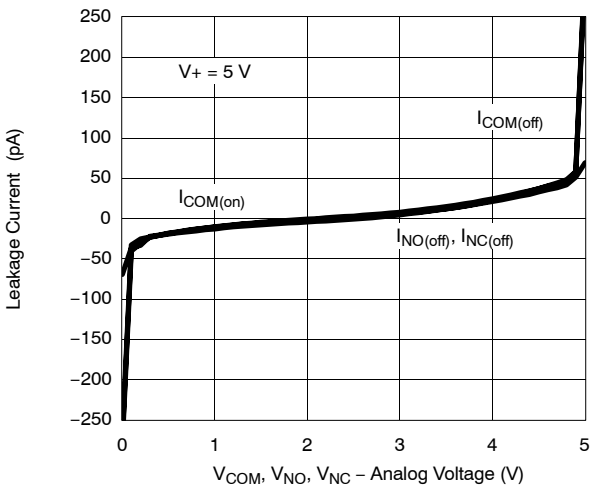
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

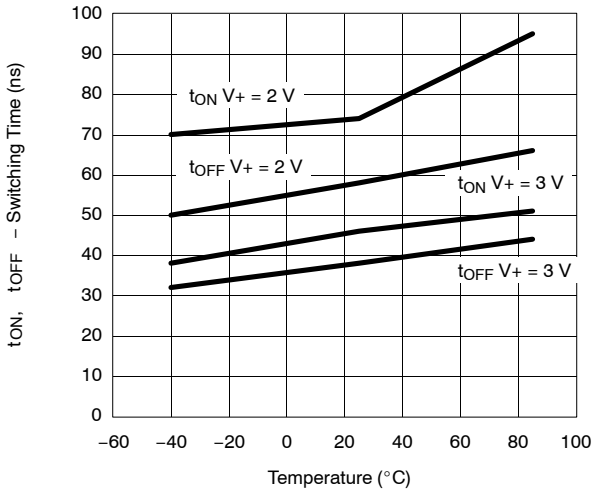


Leakage vs. Analog Voltage

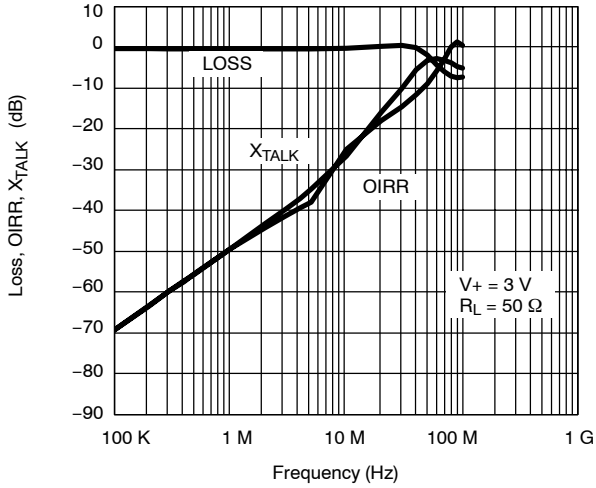


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

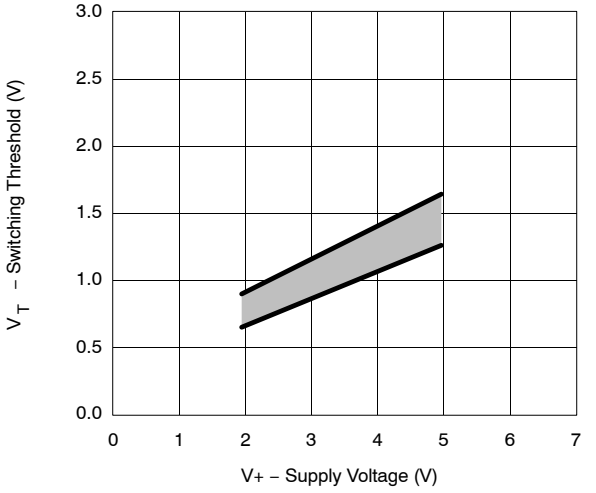
Switching Time vs. Temperature and Supply Voltage



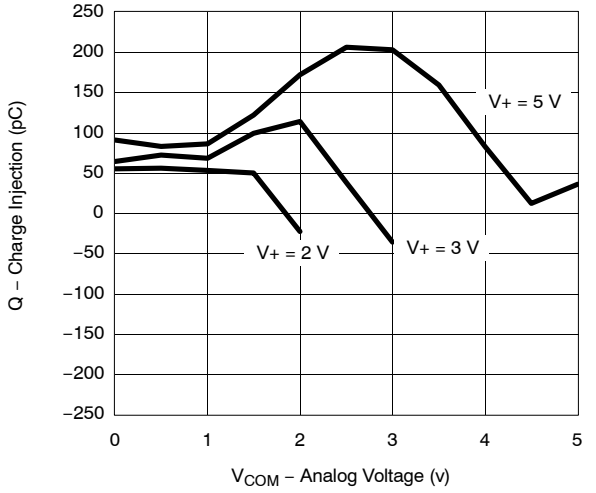
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



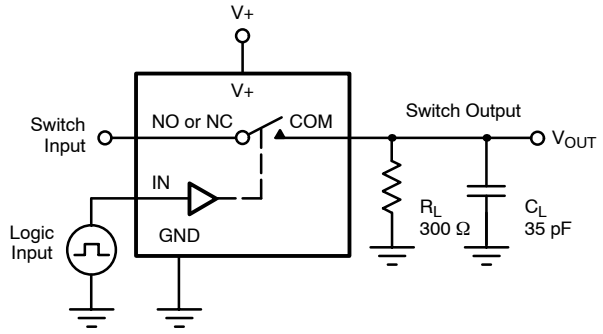
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

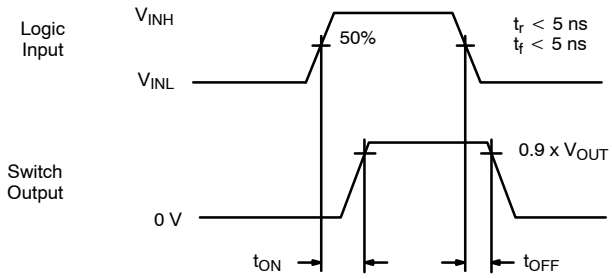


TEST CIRCUITS



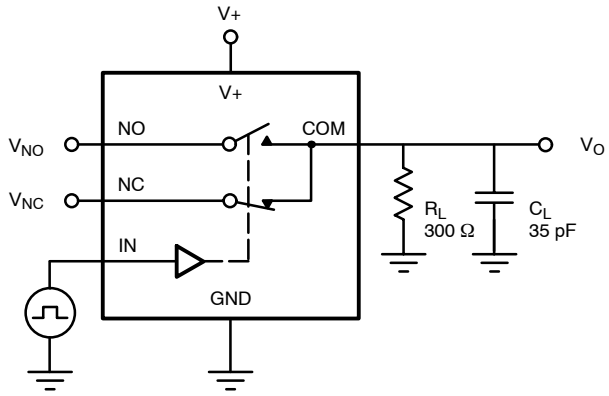
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

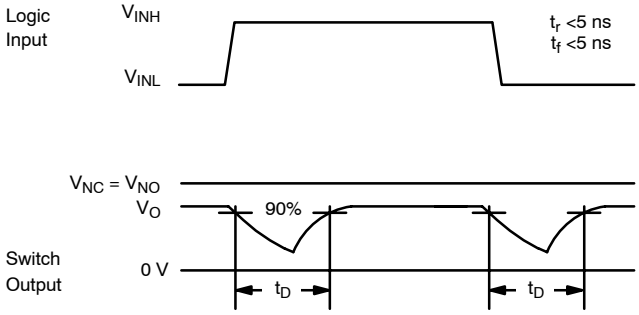
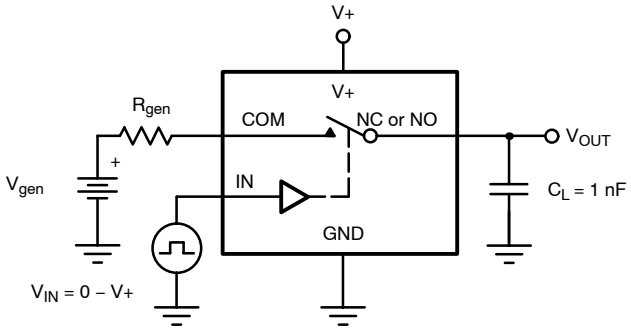
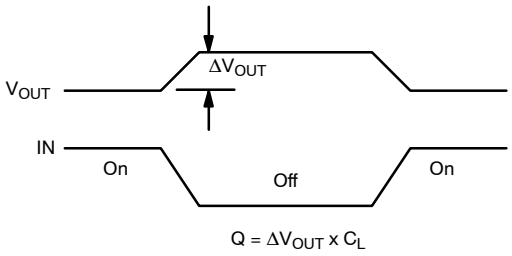


FIGURE 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

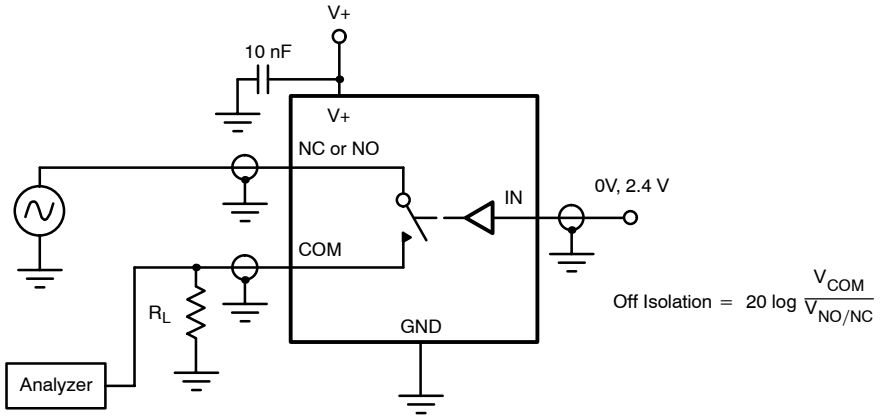


FIGURE 4. Off-Isolation

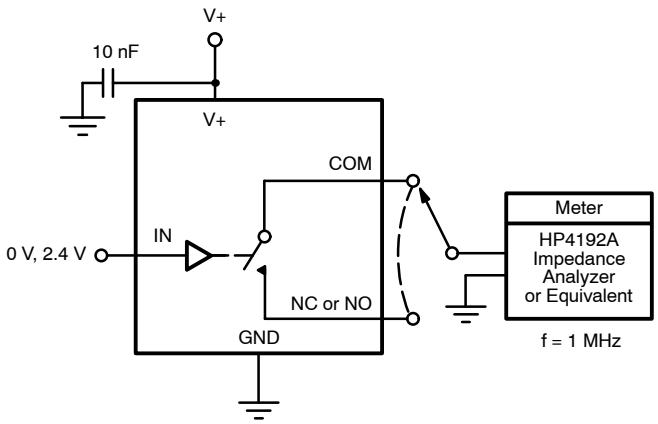
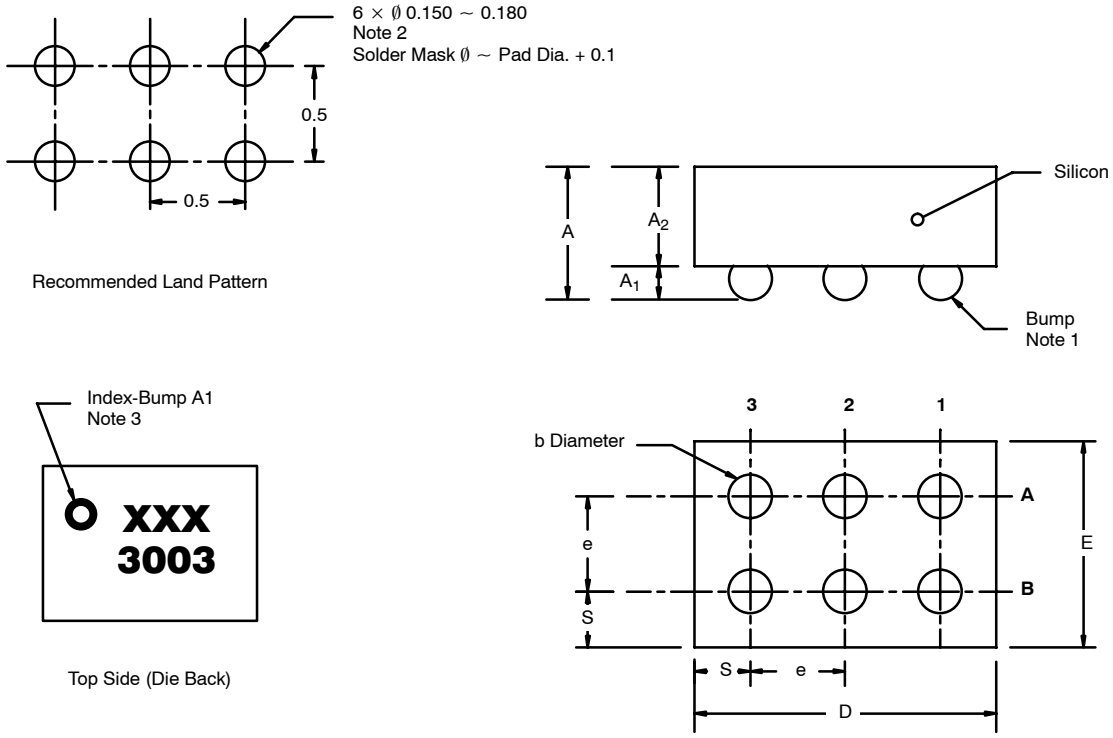


FIGURE 5. Channel Off/On Capacitance

PACKAGE OUTLINE

MICRO FOOT: 6-BUMP (3 X 2, 0.5-mm PITCH, 165-μm BUMP HEIGHT)



NOTES (Unless Otherwise Specified):

1. Bump is Eutectic 63/57 Sn/Pb.
2. Non-solder mask defined copper landing pad.
3. Laser Mark on silicon die back; no coating. Shown is not actual marking; sample only.

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.610	0.685	0.0240	0.0270
A_1	0.140	0.190	0.0055	0.0075
A_2	0.470	0.495	0.0185	0.0195
b	0.180	0.250	0.0071	0.0098
D	1.490	1.515	0.0587	0.0596
E	0.990	1.015	0.0390	0.0400
e	0.5 BASIC		0.0197 BASIC	
S	0.245	0.258	0.0096	0.0101

* Use millimeters as the primary measurement.