

FEATURES

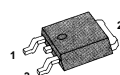
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = -200V$
- Lower $R_{DS(ON)}$: 1.111 Ω (Typ.)

$$BV_{DSS} = -200 V$$

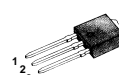
$$R_{DS(on)} = 1.5 \Omega$$

$$I_D = -3.1 A$$

D-PAK



I-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	-200	V
I_D	Continuous Drain Current ($T_C=25^\circ C$)	-3.1	A
	Continuous Drain Current ($T_C=100^\circ C$)	-1.96	
I_{DM}	Drain Current-Pulsed ①	-12	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	256	mJ
I_{AR}	Avalanche Current ①	-3.1	A
E_{AR}	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
P_D	Total Power Dissipation ($T_A=25^\circ C$) *	2.5	W
	Total Power Dissipation ($T_C=25^\circ C$)	30	W
	Linear Derating Factor	0.24	W/ $^\circ C$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	4.17	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient *	--	50	
$R_{\theta JA}$	Junction-to-Ambient	--	110	

* When mounted on the minimum pad size recommended (PCB Mount).

Rev. B

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	-200	--	--	V	$V_{GS}=0V, I_D=-250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	-0.18	--	V/ $^\circ\text{C}$	$I_D=-250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	--	-4.0	V	$V_{DS}=-5V, I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage , Forward	--	--	-100	nA	$V_{GS}=-30V$
	Gate-Source Leakage , Reverse	--	--	100		$V_{GS}=30V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	-10	μA	$V_{DS}=-200V$
		--	--	-100		$V_{DS}=-160V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	1.5	Ω	$V_{GS}=-10V, I_D=-1.6A$ ④
g_{fs}	Forward Transconductance	--	2.2	--	Ω	$V_{DS}=-40V, I_D=-1.6A$ ④
C_{iss}	Input Capacitance	--	415	540	pF	$V_{GS}=0V, V_{DS}=-25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	70	105		
C_{rss}	Reverse Transfer Capacitance	--	26	40		
$t_{d(on)}$	Turn-On Delay Time	--	12	35	ns	$V_{DD}=-100V, I_D=-3.5A,$ $R_G=18\Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	--	22	55		
$t_{d(off)}$	Turn-Off Delay Time	--	33	75		
t_f	Fall Time	--	15	40		
Q_g	Total Gate Charge	--	15	19	nC	$V_{DS}=-160V, V_{GS}=-10V,$ $I_D=-3.5A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	--	3.3	--		
Q_{gd}	Gate-Drain(" Miller ") Charge	--	7.5	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	-3.1	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	-12		
V_{SD}	Diode Forward Voltage ④	--	--	-5.0	V	$T_J=25^\circ\text{C}, I_S=-3.1A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	125	--	ns	$T_J=25^\circ\text{C}, I_F=-3.5A$
Q_{rr}	Reverse Recovery Charge	--	0.59	--	μC	$di_F/dt=100A/\mu s$ ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
 ② $L=40\text{mH}, I_{AS}=-3.1A, V_{DD}=-50V, R_G=27\Omega^*,$ Starting $T_J=25^\circ\text{C}$
 ③ $I_{SD}\leq -3.5A, di/dt \leq 300A/\mu s, V_{DD}\leq BV_{DSS},$ Starting $T_J=25^\circ\text{C}$
 ④ Pulse Test : Pulse Width = 250 μs , Duty Cycle $\leq 2\%$
 ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

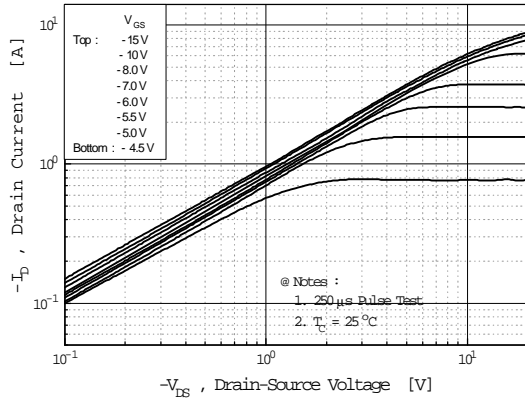


Fig 2. Transfer Characteristics

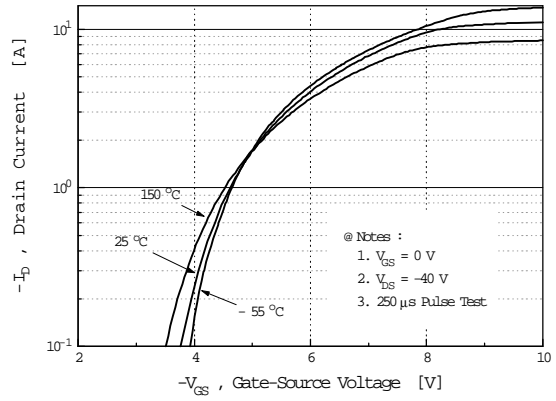


Fig 3. On-Resistance vs. Drain Current

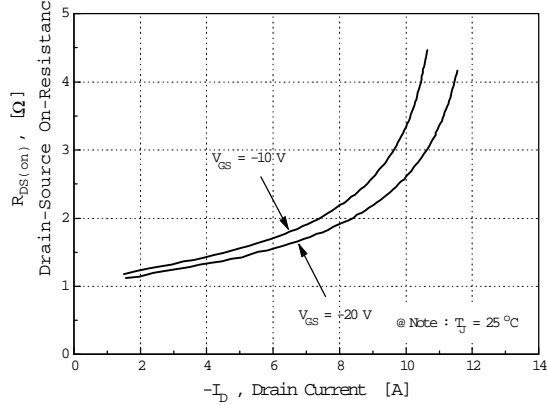


Fig 4. Source-Drain Diode Forward Voltage

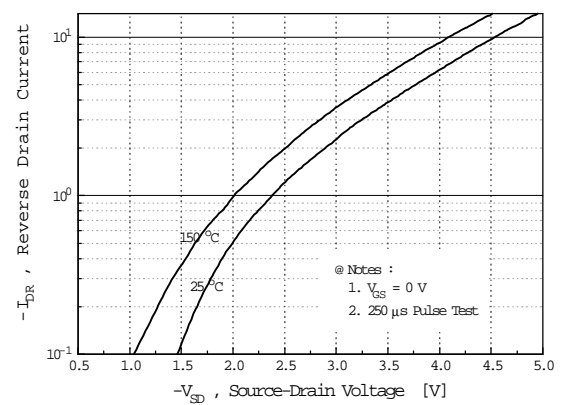


Fig 5. Capacitance vs. Drain-Source Voltage

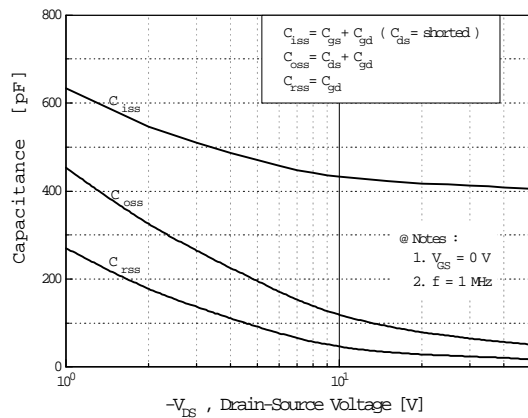
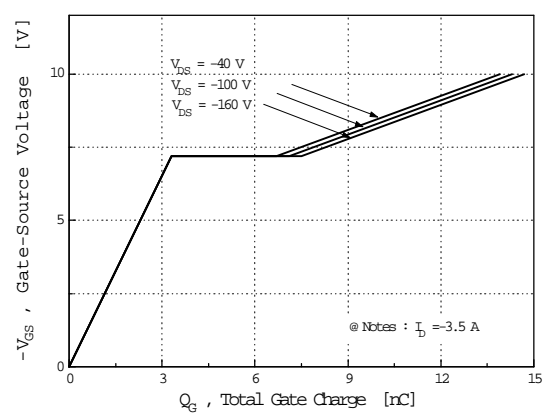


Fig 6. Gate Charge vs. Gate-Source Voltage



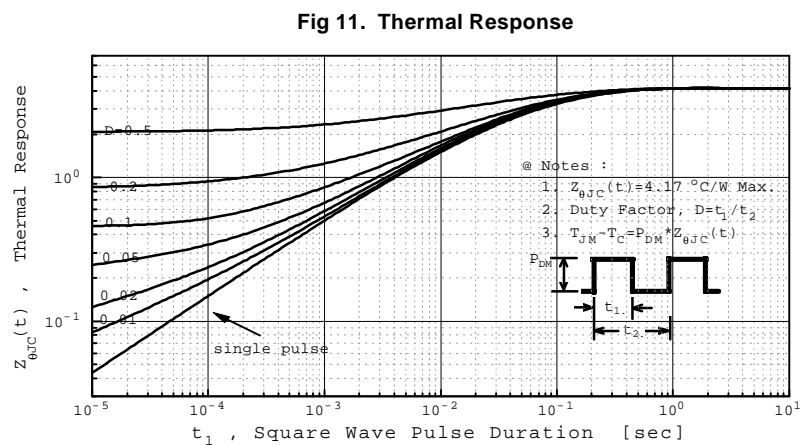
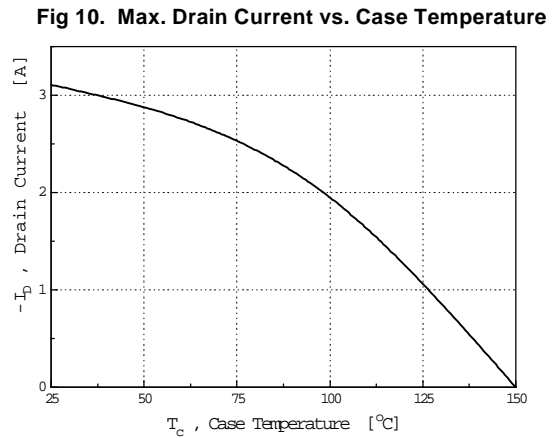
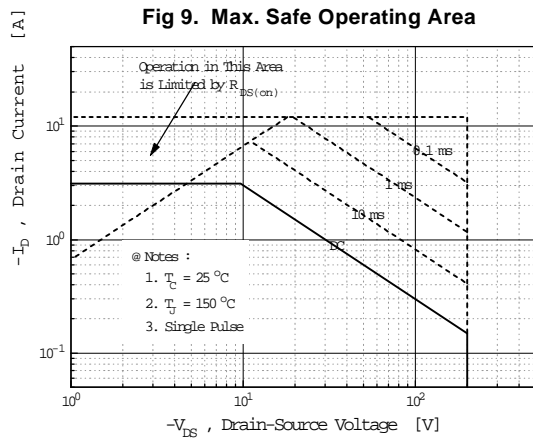
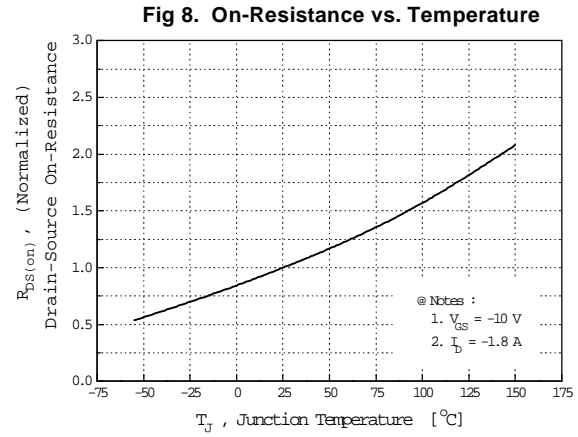
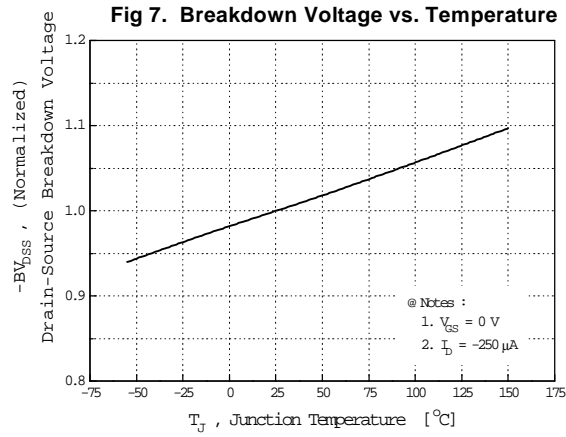


Fig 12. Gate Charge Test Circuit & Waveform

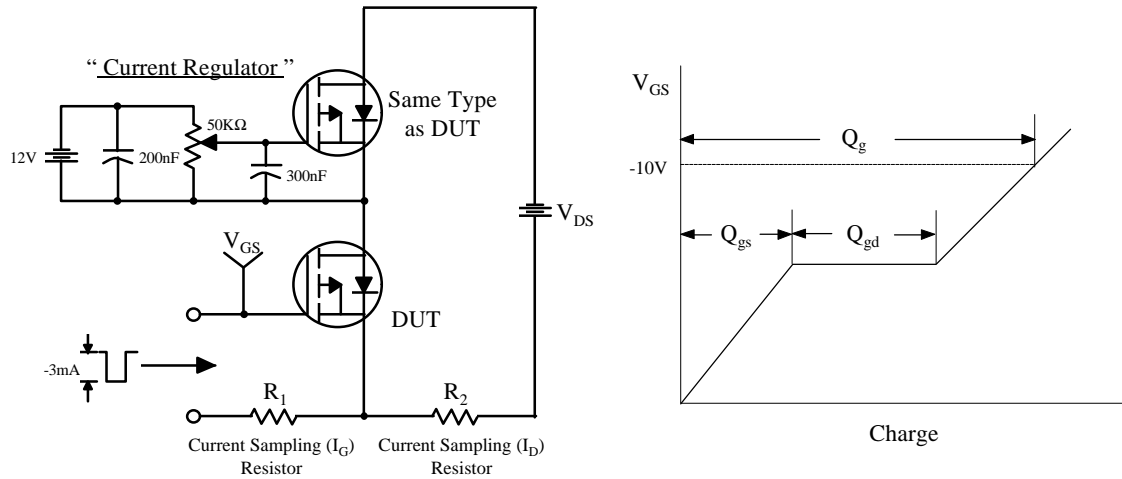


Fig 13. Resistive Switching Test Circuit & Waveforms

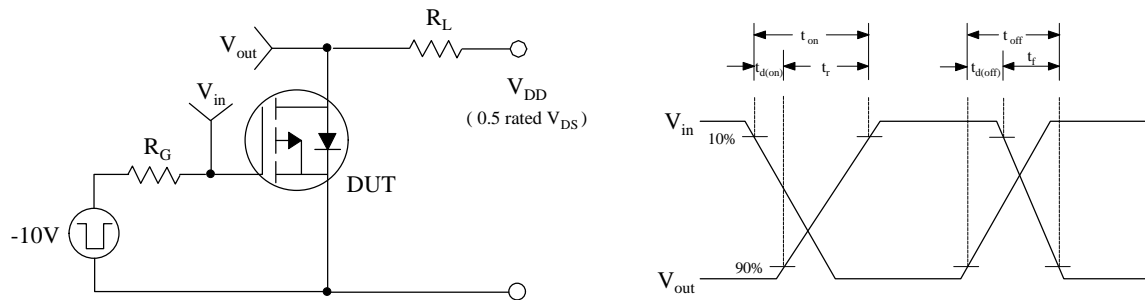
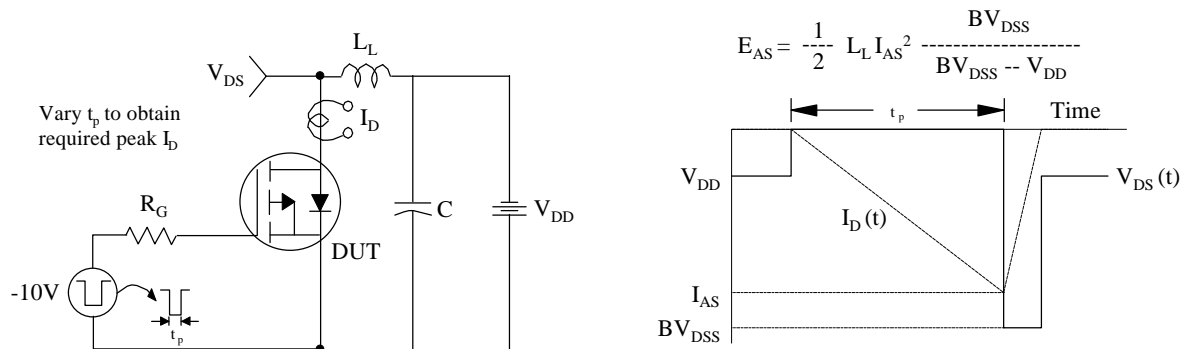
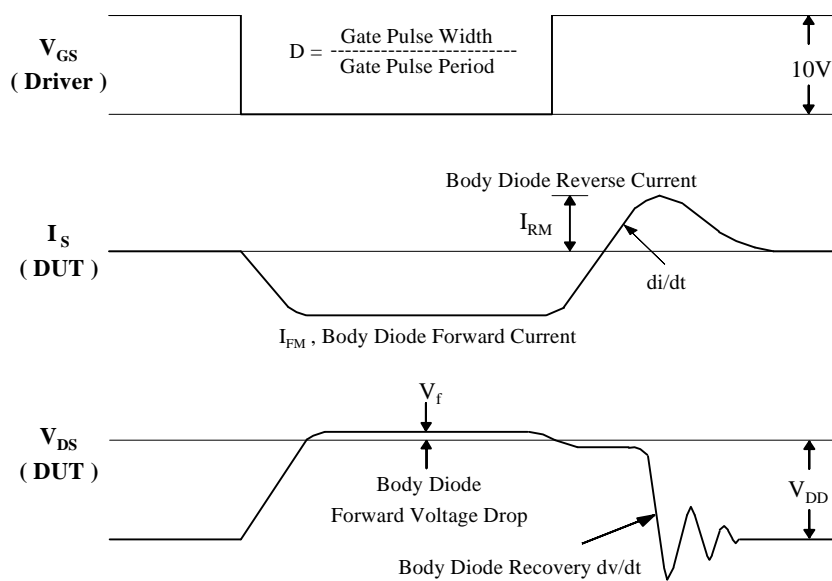


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



• dv/dt controlled by “ R_G ”

• I_S controlled by Duty Factor “D”



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