



# STM809, STM810 STM811, STM812

## Reset Circuit

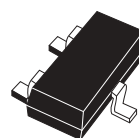
### FEATURES SUMMARY

- PRECISION MONITORING OF 3V, 3.3V, and 5V SUPPLY VOLTAGES
- TWO OUTPUT CONFIGURATIONS
  - Push-pull  $\overline{\text{RST}}$  Output (STM809/811)
  - Push-pull RST Output (STM810/812)
- 140ms RESET PULSE WIDTH (MIN)
- LOW SUPPLY CURRENT - 6 $\mu$ A (TYP)
- GUARANTEED  $\overline{\text{RST}}$ /RST ASSERTION DOWN TO  $V_{\text{CC}} = 1.0\text{V}$
- OPERATING TEMPERATURE:  
–40°C to 85°C (Industrial Grade)
- LEAD-FREE, SMALL SOT23 and SOT143 PACKAGE

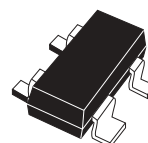
Table 1. Device Options

	Active-Low RESET	Active-High RESET	Manual RESET Input	Package
STM809	✓			SOT23-3
STM810		✓		SOT23-3
STM811	✓		✓	SOT143-4
STM812		✓	✓	SOT143-4

Figure 1. Packages



SOT23-3 (WX)



SOT143-4 (W1)

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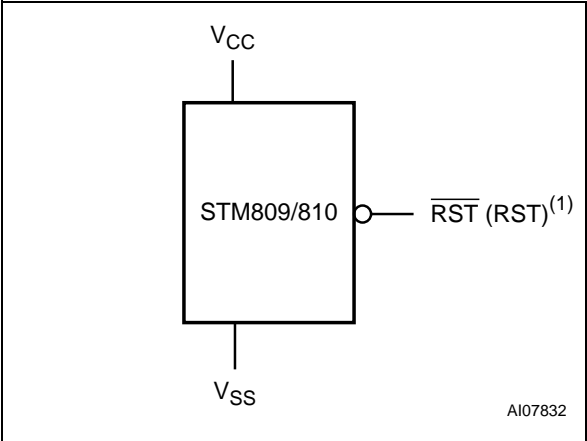
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SUMMARY DESCRIPTION

The STM809/810/811/812 MICROPROCESSOR RESET Circuits are low-power supervisory devices used to monitor power supplies. They perform a single function: asserting a reset signal whenever the  $V_{CC}$  supply voltage drops below a preset

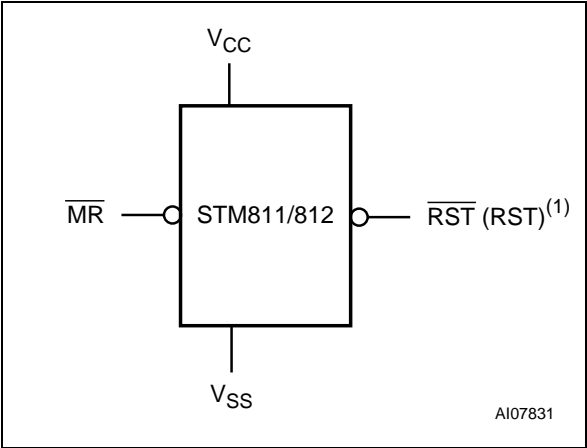
value and keeping it asserted until  $V_{CC}$  has risen above the preset threshold for a minimum period of time ( $t_{rec}$ ). The STM811/812 also provide a push-button reset input (MR).

Figure 2. Logic Diagram (STM809/810)



Note: 1. For STM810

Figure 3. Logic Diagram (STM811/812)



Note: 1. For STM812

Table 2. Signal Names

$V_{SS}$	Ground
$\overline{RST}$	Active-Low RESET Output
$RST^{(1)}$	Active-High RESET Output
$V_{CC}$	Supply Voltage
$\overline{MR}^{(2)}$	Manual Reset Input

Note: 1. STM810/812 only  
2. STM811/812 only

Figure 4. SOT23-3 Connections

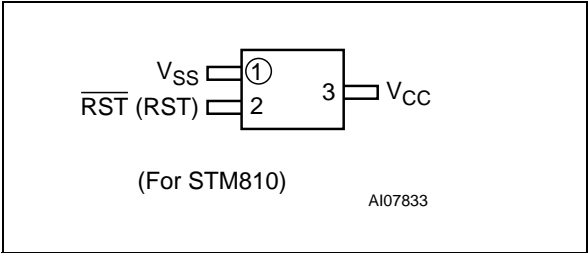


Figure 5. SOT143-4 Connections

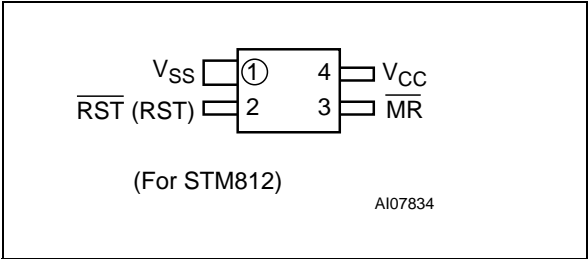
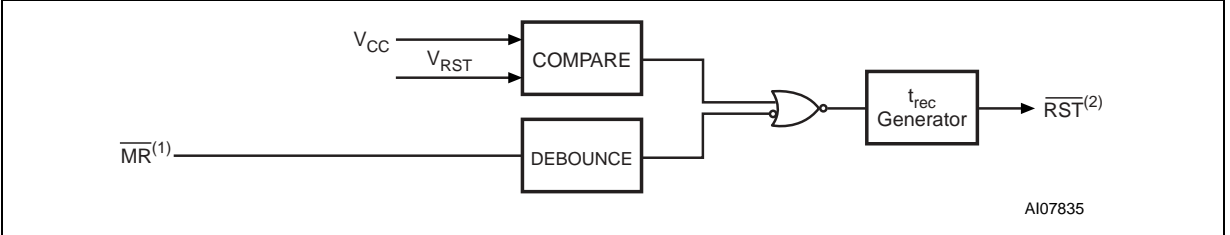
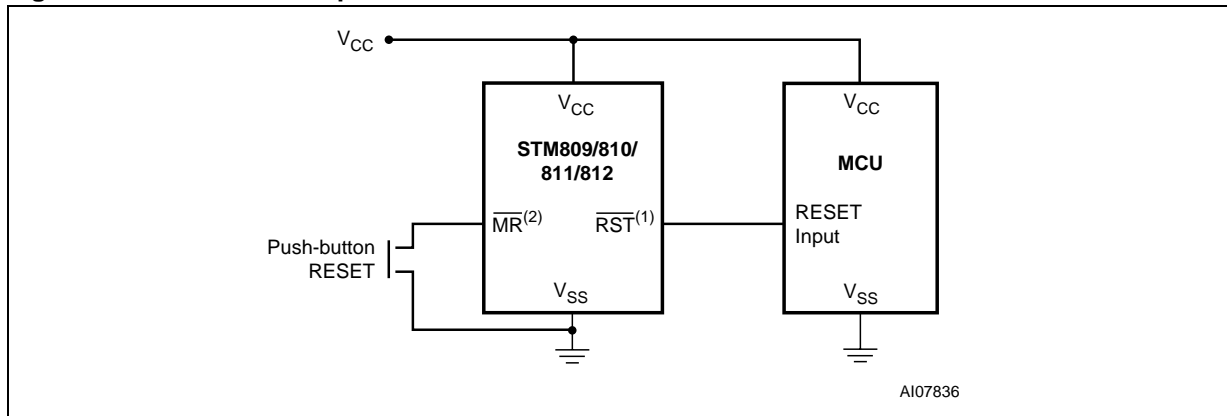


Figure 6. Block Diagram



Note: 1. STM811/812 only  
2. RST for STM810/812

Figure 7. Hardware Hookup



Note: 1. STM809/811 only (RST for STM810/812)  
2. STM811/812 only

## OPERATION

### Reset Output

The STM809/810/811/812 MICROPROCESSOR RESET CIRCUIT asserts a reset signal to the MCU whenever  $V_{CC}$  goes below the reset threshold ( $V_{RST}$ ), or when the push-button reset input ( $\overline{MR}$ ) is taken low (see [Figure 15., page 11](#)).  $\overline{RST}$  (active high for STM810/812) is guaranteed valid down to  $V_{CC} = 1V$  ( $0^\circ$  to  $70^\circ C$ ).

During power-up, once  $V_{CC}$  exceeds the reset threshold an internal timer keeps  $\overline{RST}$  low for the reset time-out period,  $t_{rec}$ . After this interval,  $\overline{RST}$  returns high.

If  $V_{CC}$  drops below the reset threshold,  $\overline{RST}$  goes low. Each time  $\overline{RST}$  is asserted, it stays low for at least the reset time-out period. Any time  $V_{CC}$  goes below the reset threshold, the internal timer clears. The reset timer starts when  $V_{CC}$  returns above the reset threshold. The active-low reset ( $\overline{RST}$ ) and active-high reset ( $RST$ ) both source and sink current.

### Push-Button Reset Input (STM811/812)

A logic low on  $\overline{MR}$  asserts  $\overline{RST}$ .  $\overline{RST}$  remains asserted while  $\overline{MR}$  is low, and for  $t_{rec}$  after it returns high. The  $\overline{MR}$  input has an internal  $20k\Omega$  pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open push-button switch from  $\overline{MR}$  to GND to create a manual reset function; external debounce circuitry is not required. If the device is used in a noisy environment, connect a  $0.1\mu F$  capacitor from  $\overline{MR}$  to GND to provide additional noise immunity.

### Negative-Going $V_{CC}$ Transients

The STM809/810/811/812 are relatively immune to negative-going  $V_{CC}$  transients (glitches). [Figure 13., page 9](#) shows typical transient duration versus reset comparator overdrive (for which the STM809/810/811/812 will NOT generate a reset pulse). The graph was generated using a negative pulse applied to  $V_{CC}$ , starting at  $0.5V$  above the actual reset threshold and ending below it by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative  $V_{CC}$  transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a  $V_{CC}$  transient that goes  $100mV$  below the reset threshold and lasts  $20\mu s$  or less will not cause a reset pulse. A  $0.1\mu F$  bypass capacitor mounted as close as possible to the  $V_{CC}$  pin provides additional transient immunity.

### Valid $\overline{RST}$ Output Down to $V_{CC} = 0V$

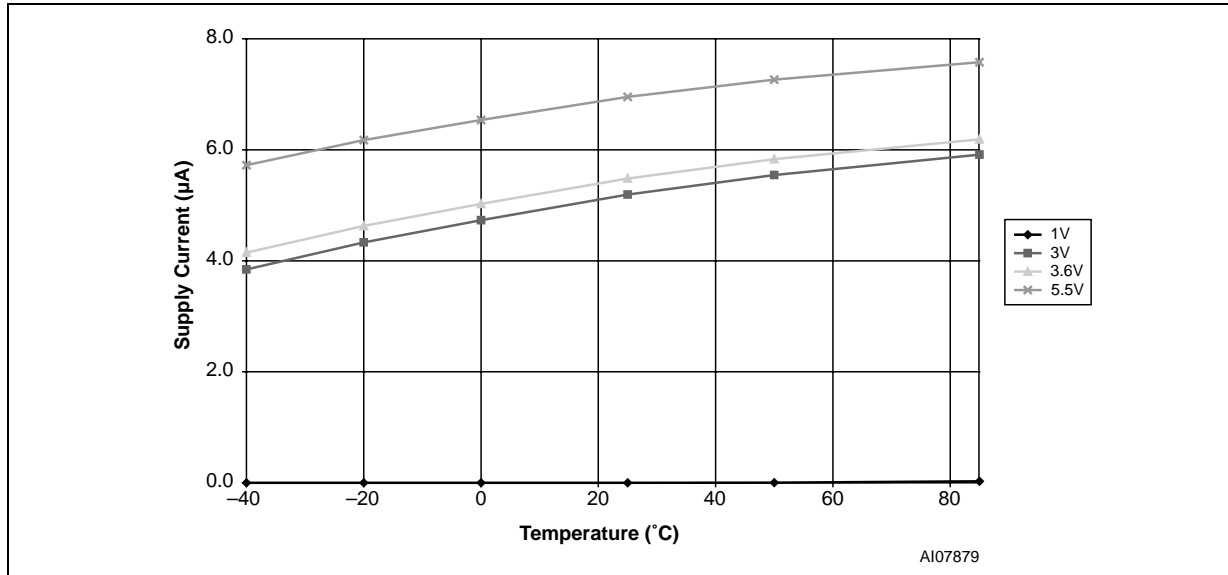
When  $V_{CC}$  falls below  $1V$ , the  $\overline{RST}$  (STM809/811) output no longer sinks current, but becomes an open circuit. In most systems this is not a problem, as most MCUs do not operate below  $1V$ . However, in applications where  $\overline{RST}$  output must be valid down to  $0V$ , a pull-down resistor may be added to hold the  $\overline{RST}$  output low. This resistor must be large enough to not load the  $\overline{RST}$  output, and still be small enough to pull the output to ground. A  $100k\Omega$  resistor is recommended.

**Note:** The same situation applies for the active-high  $RST$  of the STM810/812. A  $100k\Omega$  pull-up resistor to  $V_{CC}$  should be used if  $RST$  must remain valid for  $V_{CC} < 1.0V$ .

## TYPICAL OPERATING CHARACTERISTICS

**Note:** Typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  for L/M versions,  $V_{CC} = 3.3\text{V}$  for T/S versions, and  $V_{CC} = 3.0\text{V}$  for R versions.

**Figure 8. Supply Current vs. Temperature, L/M/R/S/T (no load)**



**Figure 9. Power-down Reset Delay vs. Temperature -  $V_{OD} = V_{TH} - V_{CC}$  (L/M)**

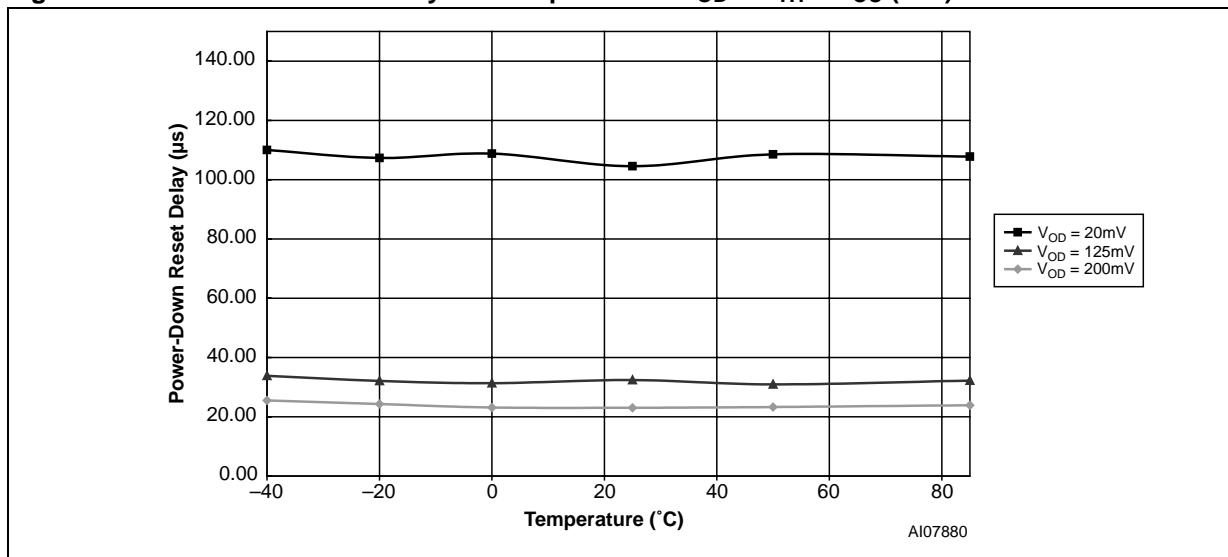


Figure 10. Power-down Reset Delay vs. Temperature -  $V_{OD} = V_{TH} - V_{CC}$  (R/S/T)

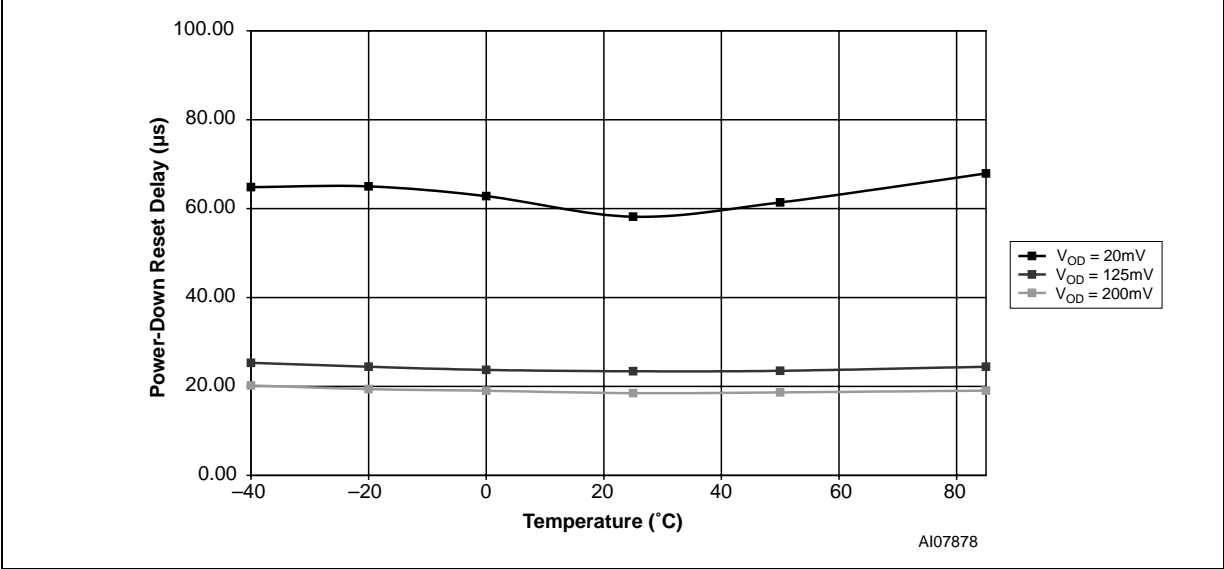


Figure 11. Power-up  $t_{rec}$  vs. Temperature

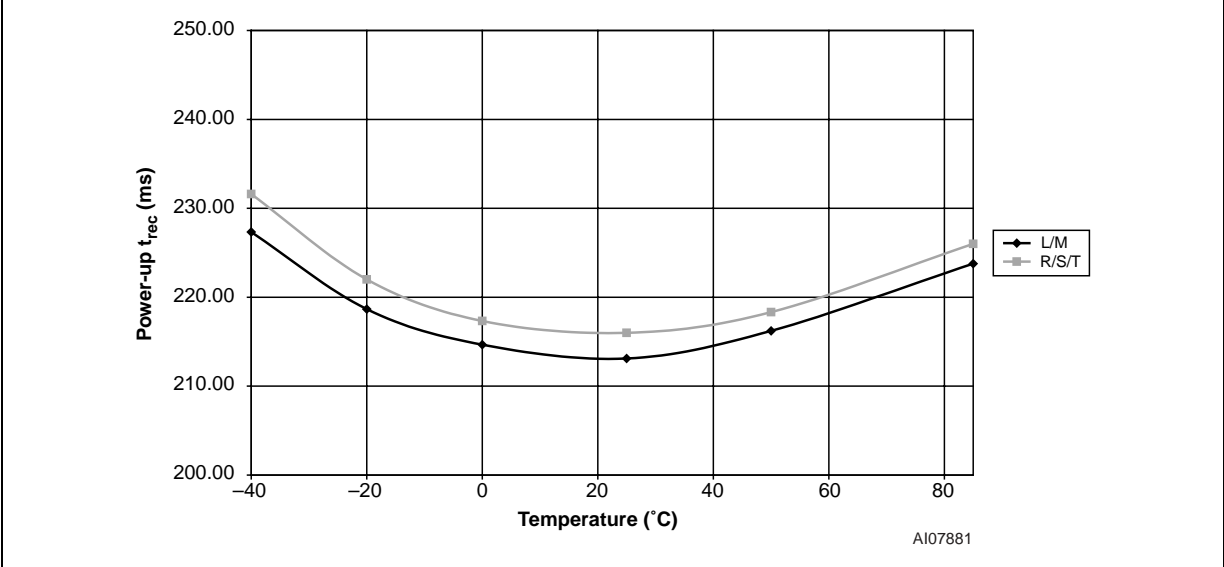




Figure 12. Normalized Reset Threshold vs. Temperature

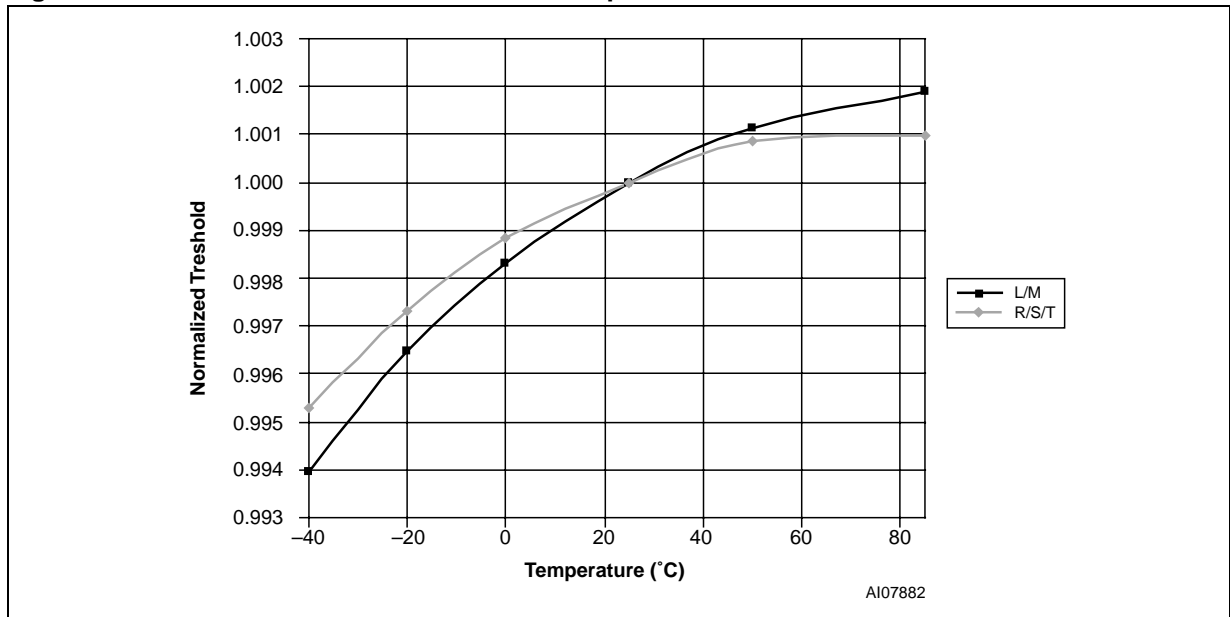
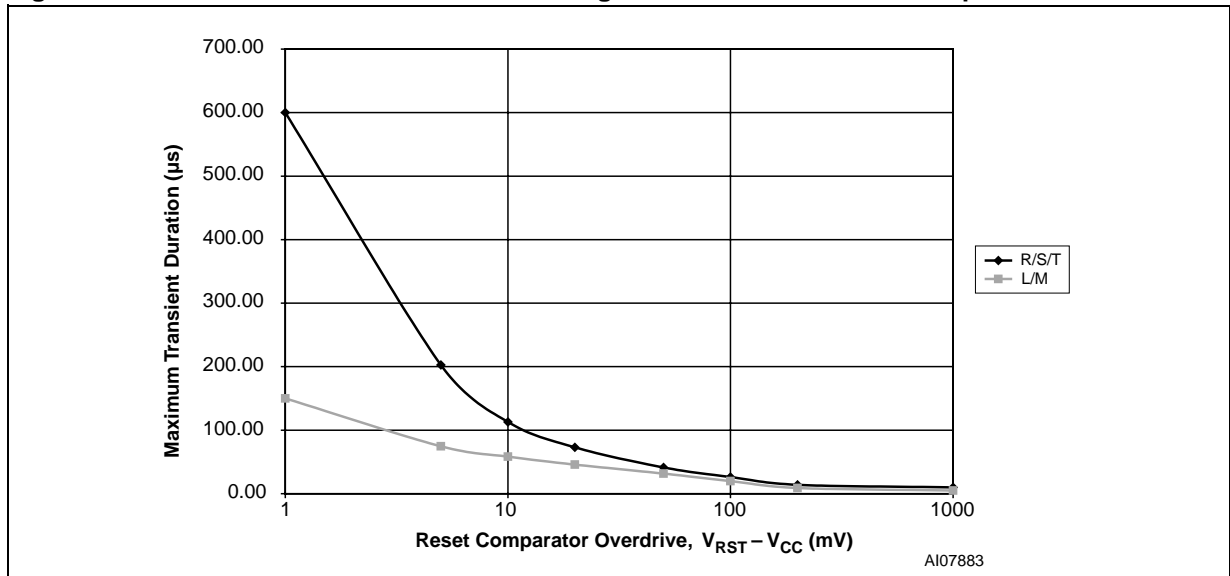


Figure 13. Max Transient Duration NOT Causing Reset Pulse vs. Reset Comparator Overdrive



## MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off)	–55 to 150	°C
T <sub>SLD</sub> <sup>(1)</sup>	Lead Solder Temperature for 10 seconds	260	°C
V <sub>IO</sub>	Input or Output Voltage	–0.3 to V <sub>CC</sub> +0.3	V
V <sub>CC</sub>	Supply Voltage	–0.3 to 7.0	V
I <sub>O</sub>	Output Current	20	mA
P <sub>D</sub>	Power Dissipation	320	mW

Note: 1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

## DC AND AC PARAMETERS

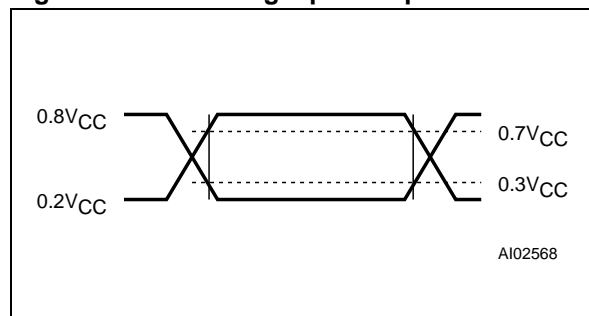
This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement

Conditions summarized in [Table 4.](#), Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

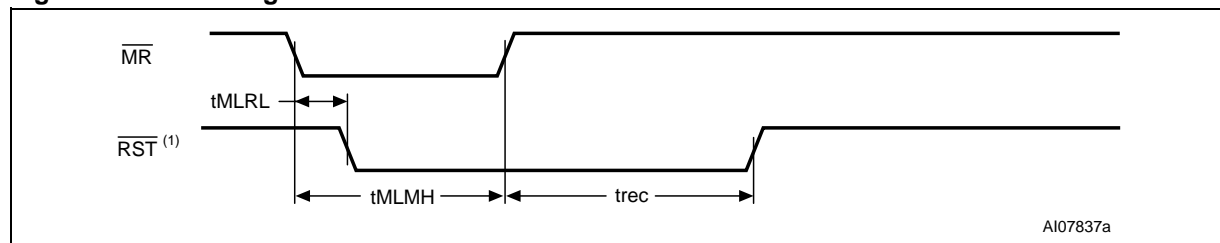
**Table 4. Operating and AC Measurement Conditions**

Parameter	STM809/810/811/812	Unit
V <sub>CC</sub> Supply Voltage	1.0 to 5.5	V
Ambient Operating Temperature (T <sub>A</sub> )	−40 to 85	°C
Input Rise and Fall Times	≤ 5	ns
Input Pulse Voltages	0.2 to 0.8V <sub>CC</sub>	V
Input and Output Timing Ref. Voltages	0.3 to 0.7V <sub>CC</sub>	V

**Figure 14. AC Testing Input/Output Waveforms**



**Figure 15.  $\overline{\text{MR}}$  Timing Waveform**



Note: 1. RST for STM810/812

Table 5. DC and AC Characteristics

Sym	Alter- native	Description	Test Condition <sup>(1)</sup>	Min	Typ	Max	Unit	
V <sub>CC</sub>		Operating Voltage	T <sub>A</sub> = −40 to +85°C	1.2		5.5	V	
			T <sub>A</sub> = 0 to +70°C	1.0		5.5	V	
I <sub>CC</sub>		V <sub>CC</sub> Supply Current	V <sub>CC</sub> < 3.6V		5.5	10	μA	
			V <sub>CC</sub> < 5.5V		7	15	μA	
V <sub>IH</sub>		$\overline{\text{MR}}$ Input High Voltage	V <sub>CC</sub> > V <sub>RST</sub> (max), STM8XXL/M	2.2			V	
			V <sub>CC</sub> > V <sub>RST</sub> (max), STM8XXR/S/T	0.7V <sub>CC</sub>			V	
V <sub>IL</sub>		$\overline{\text{MR}}$ Input Low Voltage	V <sub>CC</sub> > V <sub>RST</sub> (max), STM8XXL/M			0.8	V	
			V <sub>CC</sub> > V <sub>RST</sub> (max), STM8XXR/S/T			0.25V <sub>CC</sub>	V	
V <sub>OL</sub>		$\overline{\text{RST}}$ Output Low Voltage (Active High <sup>(2)</sup> or Low)	STM8XXR/S/T only, I <sub>OL</sub> = 1.2mA V <sub>CC</sub> = V <sub>RST</sub> (min)			0.3	V	
			STM8XXL/M only, I <sub>OL</sub> = 3.2mA V <sub>CC</sub> = V <sub>RST</sub> (min)			0.4	V	
V <sub>OL</sub>		$\overline{\text{RST}}$ Output Low Voltage	I <sub>OL</sub> = 50μA; V <sub>CC</sub> > 1.0V			0.3	V	
V <sub>OH</sub>		$\overline{\text{RST}}$ Output High Voltage	STM8XXR/S/T only, I <sub>OH</sub> = 500μA	0.8V <sub>CC</sub>			V	
			STM8XXL/M only, I <sub>OH</sub> = 800μA	0.8V <sub>CC</sub>			V	
		RST Output High Voltage	I <sub>OH</sub> = 150μA, 1.8V < V <sub>CC</sub> < V <sub>RST</sub> (min)	0.8V <sub>CC</sub>			V	
RESET Thresholds								
V <sub>RST</sub>		Reset Threshold	STM8XXL	25°C	4.56	4.63	4.70	V
				−40 to 85°C	4.50		4.75	V
			STM8XXM	25°C	4.31	4.38	4.45	V
				−40 to 85°C	4.25		4.50	V
			STM8XXT	25°C	3.04	3.08	3.11	V
				−40 to 85°C	3.00		3.15	V
			STM8XXS	25°C	2.89	2.93	2.96	V
				−40 to 85°C	2.85		3.00	V
			STM8XXR	25°C	2.59	2.63	2.66	V
				−40 to 85°C	2.55		2.70	V
		V <sub>RST</sub> Temperature Coefficient	V <sub>CC</sub> = 3.3V			45		ppm/ °C
		V <sub>CC</sub> to $\overline{\text{RST}}$ Delay	V <sub>CC</sub> = V <sub>RST</sub> to (V <sub>RST</sub> − 100mV)	STM8XXL/M		40		μs
				STM8XXR/S/T		20		μs
Push-Button RESET Input								
t <sub>MLMH</sub>	t <sub>MR</sub>	$\overline{\text{MR}}$ Pulse Width		10				μs
t <sub>MLRL</sub>	t <sub>MRD</sub>	$\overline{\text{MR}}$ to $\overline{\text{RST}}$ Output Delay <sup>(3)</sup>			0.5			μs
		$\overline{\text{MR}}$ Glitch Immunity <sup>(4)</sup>			100			ns
		$\overline{\text{MR}}$ Pull-up Resistance		10	20	30		kΩ
	t <sub>rec</sub>	$\overline{\text{RST}}$ Pulse Width		140	210	280		ms

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = -40 to 85°C; V<sub>CC</sub> = 1.2V to 5.5V (except where noted).

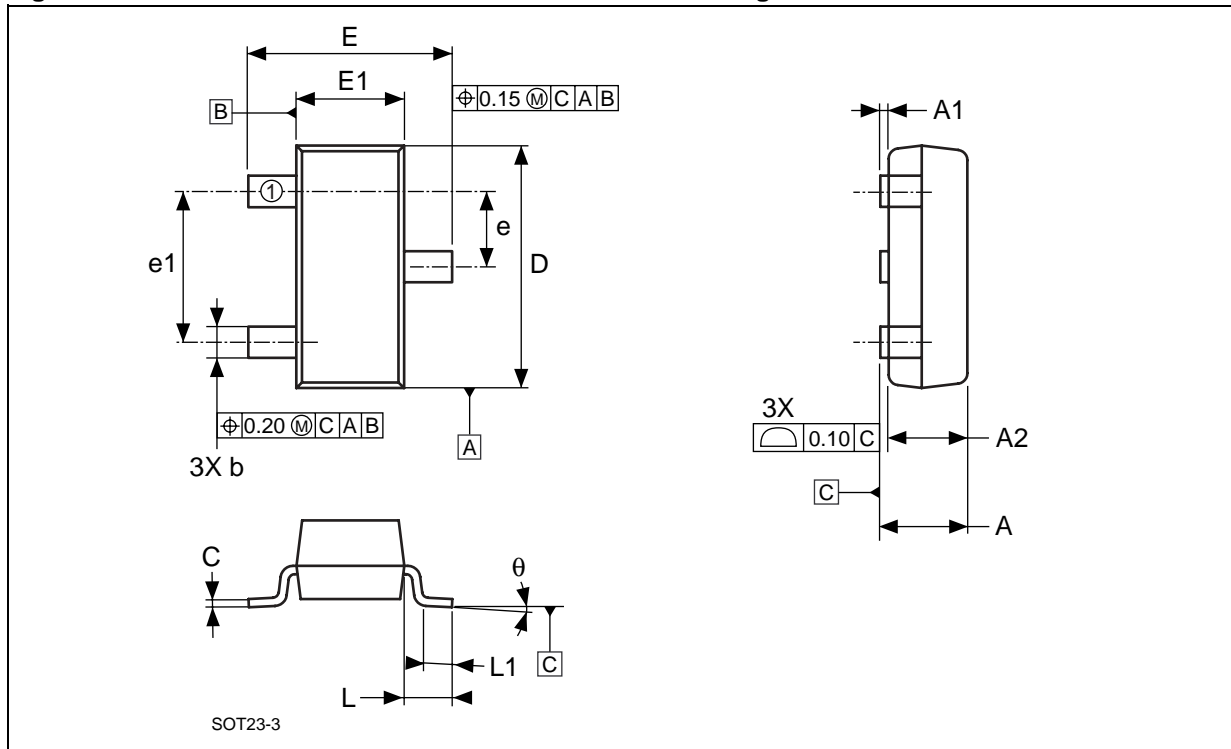
2. For Active High (RST); V<sub>CC</sub> = V<sub>RST</sub> (max)

3. RST output for STM810/812

4. "Glitches" of 100ns or less typically will not generate a RESET pulse.

## PACKAGE MECHANICAL

Figure 16. SOT23-3 – 3-lead Small Outline Transistor Package Outline

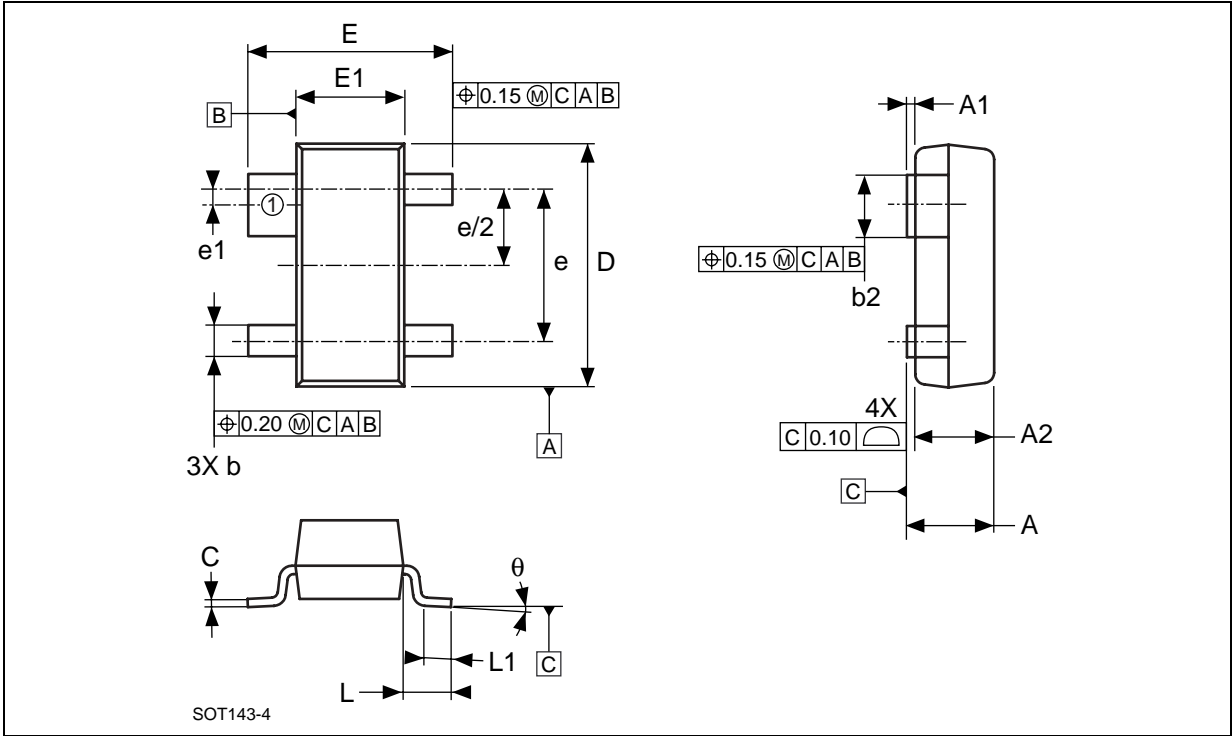


Note: Drawing is not to scale.

Table 6. SOT23-3 – 3-lead Small Outline Transistor Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.89	1.12		0.035	0.044
A1		0.01	0.10		0.001	0.004
A2		0.88	1.02		0.035	0.042
b		0.30	0.50		0.012	0.020
C		0.08	0.20		0.003	0.008
D		2.80	3.04		0.110	0.120
E		2.10	2.64		0.083	0.104
E1		1.20	1.40		0.047	0.055
e		0.89	1.03		0.035	0.041
e1		1.78	2.05		0.070	0.081
L	0.54			0.021		
L1		0.40	0.60		0.016	0.024
$\theta$		0°	8°		0°	8°
N	3			3		

Figure 17. SOT143-4 – 4-lead Small Outline Transistor Package Outline



Note: Drawing is not to scale.

Table 7. SOT143-4 – 4-lead Small Outline Transistor Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.89	1.12		0.035	0.044
A1		0.01	0.10		0.001	0.004
A2		0.88	1.02		0.035	0.042
b		0.37	0.51		0.015	0.020
b2		0.76	0.94		0.030	0.037
C		0.09	0.18		0.004	0.007
D		2.80	3.04		0.110	0.120
E		2.10	2.64		0.083	0.104
E1		1.20	1.40		0.047	0.055
e	1.92			0.076		
e1	0.20			0.008		
L	0.55			0.022		
L1		0.40	0.60		0.016	0.024
θ		0°	10°		0°	10°
N		4			4	

## PART NUMBERING

**Table 8. Ordering Information Scheme**

Example:

STM8XX

L

WX

6

F

### Device Type

STM8XX

### Reset Threshold Voltage

L =  $V_{RST} = 4.50V$  to  $4.75V$

M =  $V_{RST} = 4.25V$  to  $4.50V$

T =  $V_{RST} = 3.00V$  to  $3.15V$

S =  $V_{RST} = 2.85V$  to  $3.00V$

R =  $V_{RST} = 2.55V$  to  $2.70V$

### Package

WX = SOT23-3 (STM809, STM810)

W1 = SOT143-4 (STM811, STM812)

### Temperature Range

6 =  $-40$  to  $85^{\circ}C$

### Shipping Method

F = Pb-Free Package (ECO<sup>2</sup>PACK<sup>®</sup>), Tape & Reel

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 9. Marking Description

Part Number	Reset Threshold	Output	Topside Marking
STM809L	4.63V	Push-Pull $\overline{\text{RST}}$	8AAx
STM809M	4.38V	Push-Pull $\overline{\text{RST}}$	8ABx
STM809T	3.08V	Push-Pull $\overline{\text{RST}}$	8ACx
STM809S	2.93V	Push-Pull $\overline{\text{RST}}$	8ADx
STM809R	2.63V	Push-Pull $\overline{\text{RST}}$	8AEx
STM810L	4.63V	Push-Pull RST	8AFx
STM810M	4.38V	Push-Pull RST	8AGx
STM810T	3.08V	Push-Pull RST	8AHx
STM810S	2.93V	Push-Pull RST	8AJx
STM810R	2.63V	Push-Pull RST	8AKx
STM811L	4.63V	Push-Pull $\overline{\text{RST}}$	8ALx
STM811M	4.38V	Push-Pull $\overline{\text{RST}}$	8AMx
STM811T	3.08V	Push-Pull $\overline{\text{RST}}$	8ANx
STM811S	2.93V	Push-Pull $\overline{\text{RST}}$	8APx
STM811R	2.63V	Push-Pull $\overline{\text{RST}}$	8AQx
STM812L	4.63V	Push-Pull RST	8ARx
STM812M	4.38V	Push-Pull RST	8ASx
STM812T	3.08V	Push-Pull RST	8ATx
STM812S	2.93V	Push-Pull RST	8AUx
STM812R	2.63V	Push-Pull RST	8AVx



## REVISION HISTORY

**Table 10. Document Revision History**

Date	Version	Revision Details
02-Sep-03	1.0	First Issue
03-Oct-03	1.1	Update Operating Characteristics (Figure 8, 9, 10, 11, 12, 13)
16-Oct-03	1.2	Update characteristics (Table 5); modify illustration (Figure 13)
17-Nov-03	1.3	Modified with JEDEC timing symbols (Figure 15; Table 5)
04-Dec-03	2.0	Reformatted; promoted; updated (Figure 15; Table 5, 6)
09-Dec-03	2.1	Correct timing label, combine characteristics (Figure 11; Table 5)
10-Feb-04	3.0	Clarify package; update DC Characteristics (Table 5, 8)
19-Nov-04	4.0	Update dimensions (Table 6)

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