



STS12NH3LL

N-CHANNEL 30 V - 0.008 Ω - 12 A SO-8 ULTRA LOW GATE CHARGE STripFET™ MOSFET

PRODUCT PREVIEW

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS12NH3LL	30 V	< 0.0105 Ω	12 A

- TYPICAL R_{DS(on)} = 0.008 Ω @ 10V
- OPTIMAL R_{DS(on)} x Q_g TRADE-OFF @ 4.5 V
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- LOW INPUT CAPACITANCE

DESCRIPTION

The STS12NH3LL is based on the latest generation of ST's proprietary "STripFET™" technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements as high-side switch in high-frequency DC-DC converters. It's therefore ideal for high-density converters in Telecom and Computer applications.

APPLICATIONS

- HIGH FREQUENCY DC-DC CONVERTERS FOR COMPUTER AND TELECOM

Figure 1: Package

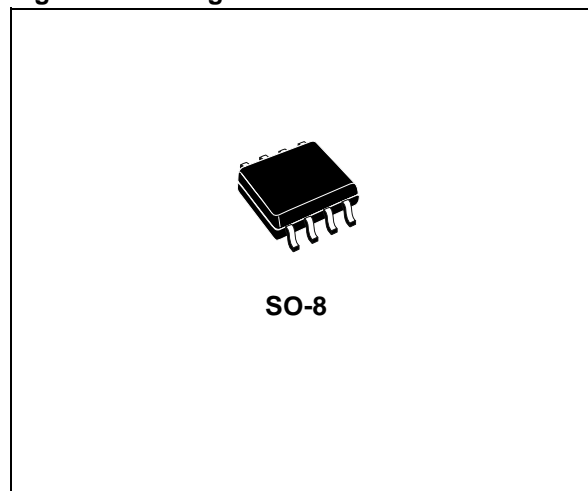


Figure 2: Internal Schematic Diagram

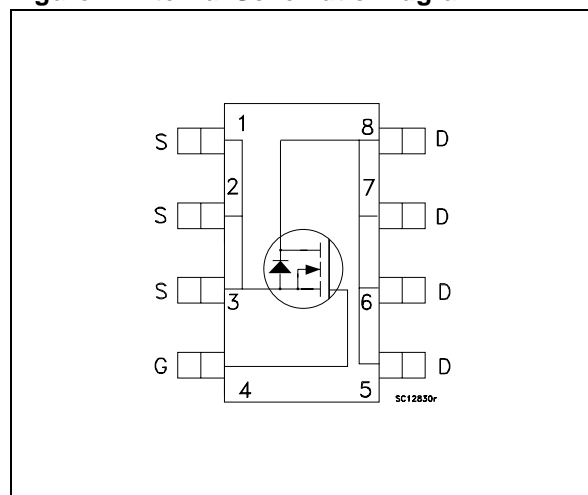


Table 2: Order Codes

Part Number	Marking	Package	Packaging
STS12NH3LL	S12NH3LL	SO-8	TAPE & REEL

Rev. 3

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	30	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	30	V
V_{GS}	Gate-source Voltage	± 16	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	12	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	7.5	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	48	A
P_{tot}	Total Dissipation at $T_C = 25^\circ\text{C}$	2.5	W
T_{stg}	Storage Temperature	– 55 to 150	$^\circ\text{C}$
T_J	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area

Table 4: Thermal Data

Rthj-amb (#)	Thermal Resistance Junction-ambient	50	$^\circ\text{C}/\text{W}$
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(#) When Mounted on 1 inch² FR-4 board, 2 oz Cu ($t \leq 10\text{ sec.}$)

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)**Table 5: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 6\text{ A}$		0.008 0.010	0.0105 0.013	Ω Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 6\text{ A}$		TBD		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		965		pF
C_{oss}	Output Capacitance			285		pF
C_{rss}	Reverse Transfer Capacitance			38		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 6\text{ A}$		15		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 3)		32		ns
Q_g	Total Gate Charge	$V_{DD} = 15\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see Figure 5)		9	12	nC
Q_{gs}	Gate-Source Charge			3.7		nC
Q_{gd}	Gate-Drain Charge			3		nC

Table 8: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 6\text{ A}$,		18		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 3)		8.5		ns

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				12	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				48	A
V_{SD}	Forward On Voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		24		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 20\text{ V}$, $T_j = 150^\circ\text{C}$ (see Figure 4)		17.4		nC
I_{RRM}	Reverse Recovery Current			1.45		A

Figure 3: Switching Times Test Circuit For Resistive Load

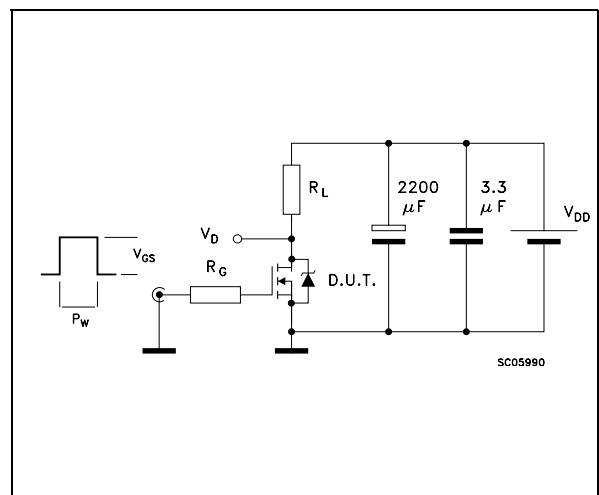


Figure 4: Test Circuit For Diode Recovery Times

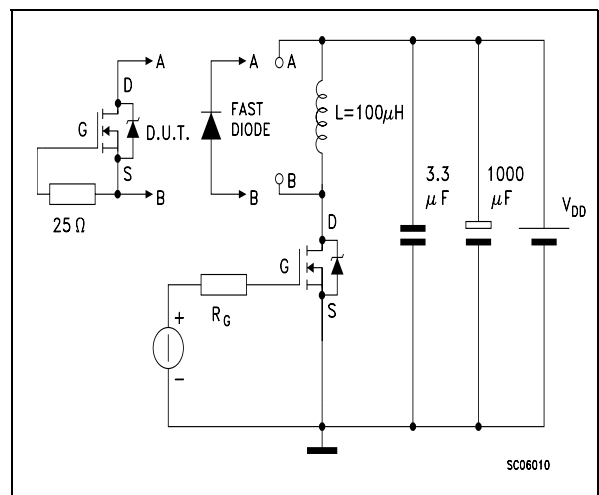
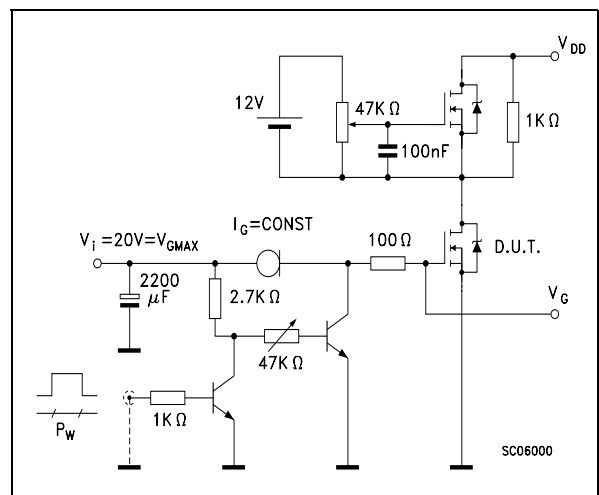
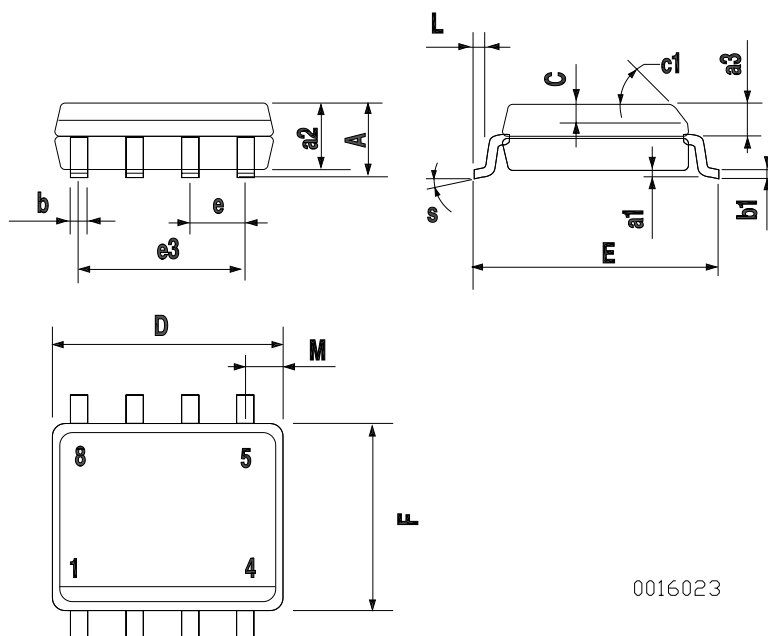


Figure 5: Gate Charge Test Circuit



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

Table 10: Revision History

Date	Revision	Description of Changes
21-July-2004	3	The Rds(on) value changed (see table5). New stylesheet

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