

Digitally Controlled Potentiometer (XDCP™)

The Intersil X9313 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the \overline{CS} , U/\overline{D} , and \overline{INC} inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

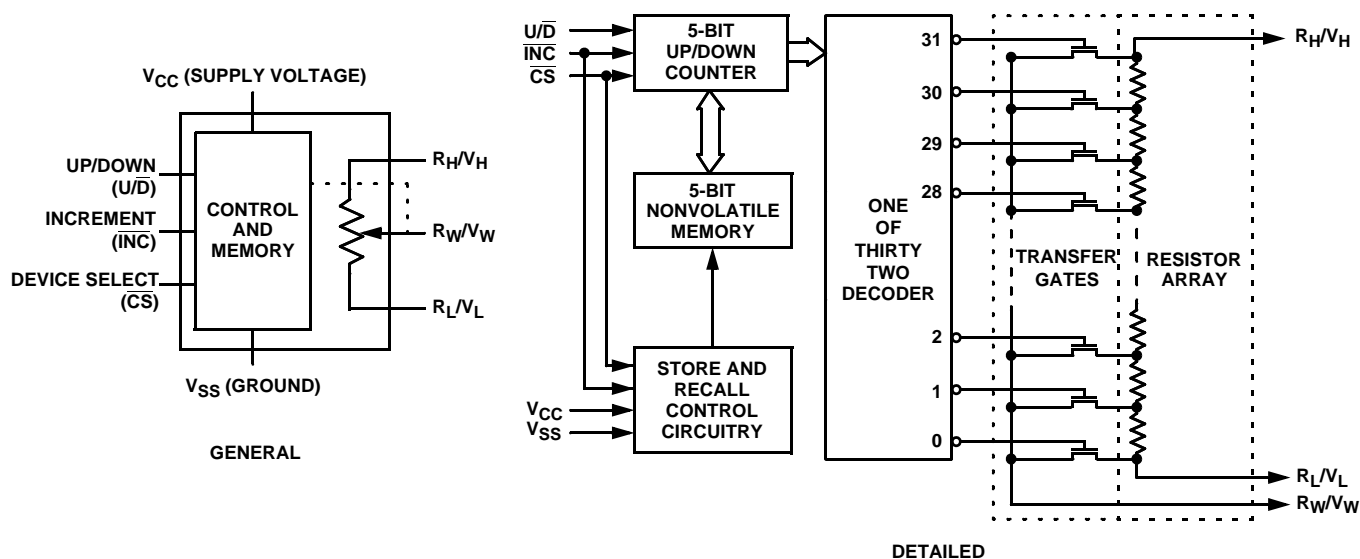
The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Control
- Parameter adjustments
- Signal processing

Features

- Solid-state potentiometer
- 3-wire serial interface
- 32 wiper tap points
 - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements
 - Temperature compensated
 - End to end resistance range $\pm 20\%$
 - Terminal voltages, $-5V$ to $+5V$
- Low power CMOS
 - $V_{CC} = 3V$ or $5V$
 - Active current, $3mA$ max.
 - Standby current, $500\mu A$ max.
- High reliability
 - Endurance, 100,000 data changes per bit
 - Register data retention, 100 years
- R_{TOTAL} values = $1k\Omega$, $10k\Omega$, $50k\Omega$
- Packages
 - 8 Ld SOIC, MSOP and DIP
- Pb-free plus anneal available (RoHS compliant)

Block Diagrams



Ordering Information

PART NUMBER	PART MARKING	V _{CC} RANGE (V)	R _{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE
X9313UM*	313U	4.5 to 5.5	50	0 to 70	8 Ld MSOP
X9313UMZ* (Note)	DDC			0 to 70	8 Ld MSOP (Pb-free)
X9313UMI*	13UI			-40 to 85	8 Ld MSOP
X9313UMIZ* (Note)	DDB			-40 to 85	8 Ld MSOP (Pb-free)
X9313UP	X9313UP			0 to 70	8 Ld PDIP
X9313UPI	X9313UP I			-40 to 85	8 Ld PDIP
X9313US*	X9313U			0 to 70	8 Ld SOIC
X9313USZ* (Note)	X9313U Z			0 to 70	8 Ld SOIC (Pb-free)
X9313USI*	X9313U I			-40 to 85	8 Ld SOIC
X9313USIZ* (Note)	X9313U Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9313USM				0 to 70	8 Ld SOIC
X9313WM*	313W		10	0 to 70	8 Ld MSOP
X9313WMZ* (Note)	DDF			0 to 70	8 Ld MSOP (Pb-free)
X9313WMI*	13WI			-40 to 85	8 Ld MSOP
X9313WMIZ* (Note)	DDE			-40 to 85	8 Ld MSOP (Pb-free)
X9313WP	X9313WP			0 to 70	8 Ld PDIP
X9313WPI	X9313XP I			-40 to 85	8 Ld PDIP
X9313WS*	X9313WS			0 to 70	8 Ld SOIC
X9313WSZ* (Note)	X9313W Z			0 to 70	8 Ld SOIC (Pb-free)
X9313WSI*	X9313WS I			-40 to 85	8 Ld SOIC
X9313WSIZ* (Note)	X9313WS Z I			-40 to 85	8 Ld SOIC (Pb-free)
X9313WSMT2	X9313WS M			0 to 70	8 Ld SOIC Tape and Reel
X9313ZM*	313Z			0 to 70	8 Ld MSOP
X9313ZMZ* (Note)	DDJ			0 to 70	8 Ld MSOP (Pb-free)
X9313ZMI*	13ZI		1	-40 to 85	8 Ld MSOP
X9313ZMIZ* (Note)	DDH			-40 to 85	8 Ld MSOP (Pb-free)
X9313ZP	X9313ZP			0 to 70	8 Ld PDIP
X9313ZPI	X9313ZP I			-40 to 85	8 Ld PDIP
X9313ZS*	X9313ZS			0 to 70	8 Ld SOIC
X9313ZSZ* (Note)	X9313 Z			0 to 70	8 Ld SOIC (Pb-free)
X9313ZSI*	X9313ZS I			-40 to 85	8 Ld SOIC
X9313ZSIZ* (Note)	X9313ZS Z I			-40 to 85	8 Ld SOIC (Pb-free)

Ordering Information (Continued)

PART NUMBER	PART MARKING	V _{CC} RANGE (V)	R _{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE
X9313UM-3*	13UD	3 to 5.5	50	0 to 70	8 Ld MSOP
X9313UMZ-3* (Note)	DDD			0 to 70	8 Ld MSOP (Pb-free)
X9313UMI-3*	13UE			-40 to 85	8 Ld MSOP
X9313UMIZ-3* (Note)	13UE Z			-40 to 85	8 Ld MSOP (Pb-free)
X9313UP-3	X9313UP D			0 to 70	8 Ld PDIP
X9313US-3*	X9313U D			0 to 70	8 Ld SOIC
X9313USZ-3* (Note)	X9313U Z D			0 to 70	8 Ld SOIC (Pb-free)
X9313WM-3*	13WD		10	0 to 70	8 Ld MSOP
X9313WMZ-3* (Note)	DDG			0 to 70	8 Ld MSOP (Pb-free)
X9313WMI-3*	13WE			-40 to 85	8 Ld MSOP
X9313WMIZ-3* (Note)	13WE Z			-40 to 85	8 Ld MSOP (Pb-free)
X9313WP-3	X9313WP D			0 to 70	8 Ld PDIP
X9313WS-3*	X9313W D			0 to 70	8 Ld SOIC
X9313WSZ-3* (Note)	X9313W Z D			0 to 70	8 Ld SOIC (Pb-free)
X9313ZM-3*	13ZD		1	0 to 70	8 Ld MSOP
X9313ZMZ-3* (Note)	DDK			0 to 70	8 Ld MSOP (Pb-free)
X9313ZMI-3*	13ZE			-40 to 85	8 Ld MSOP
X9313ZMIZ-3* (Note)	13ZE Z			-40 to 85	8 Ld MSOP (Pb-free)
X9313ZP-3	X9313ZP D			0 to 70	8 Ld PDIP
X9313ZS-3*	X9313Z D			0 to 70	8 Ld SOIC
X9313ZSZ-3* (Note)	X9313Z Z D			0 to 70	8 Ld SOIC (Pb-free)
X9313ZSI-3*	X9313Z E			-40 to 85	8 Ld SOIC
X9313ZSIZ-3* (Note)	X9313Z Z E			-40 to 85	8 Ld SOIC (Pb-free)

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Add "T1" suffix for tape and reel.

Pin Descriptions

R_H/V_H and R_L/V_L

The high (R_H/V_H) and low (R_L/V_L) terminals of the X9313 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L/V_L and R_H/V_H references the relative position of the terminal in relation to wiper movement direction selected by the $\overline{U/\overline{D}}$ input and not the voltage potential on the terminal.

R_W/V_W

R_W/V_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω at $V_{CC} = 5V$.

Up/Down ($\overline{U/\overline{D}}$)

The $\overline{U/\overline{D}}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment (\overline{INC})

The \overline{INC} input is negative-edge triggered. Toggling \overline{INC} will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the $\overline{U/\overline{D}}$ input.

Chip Select (\overline{CS})

The device is selected when the \overline{CS} input is LOW. The current counter value is stored in nonvolatile memory when \overline{CS} is returned HIGH while the \overline{INC} input is also HIGH. After the store operation is complete the X9313 will be placed in the low power standby mode until the device is selected once again.

Pin Configuration

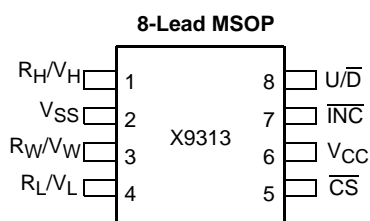
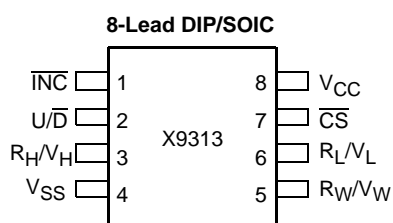


TABLE 1. PIN NAMES

SYMBOL	DESCRIPTION
R_H/V_H	High terminal
R_W/V_W	Wiper terminal
R_L/V_L	Low terminal
V_{SS}	Ground
V_{CC}	Supply voltage
$\overline{U/\overline{D}}$	Up/Down control input
\overline{INC}	Increment control input
\overline{CS}	Chip Select control input

Principles of Operation

There are three sections of the X9313: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{1W} (\overline{INC} to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The \overline{INC} , $\overline{U/\overline{D}}$ and \overline{CS} inputs control the movement of the wiper along the resistor array. With \overline{CS} set LOW the device is selected and enabled to respond to the $\overline{U/\overline{D}}$ and \overline{INC} inputs. HIGH to LOW transitions on \overline{INC} will increment or decrement (depending on the state of the $\overline{U/\overline{D}}$ input) a seven bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.







The value of the counter is stored in nonvolatile memory whenever \overline{CS} transitions HIGH while the \overline{INC} input is also HIGH.

The system may select the X9313, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{\text{INC}}$ LOW while taking $\overline{\text{CS}}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

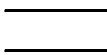




This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of $\text{U}/\overline{\text{D}}$ may be changed while $\overline{\text{CS}}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

TABLE 2. MODE SELECTION

$\overline{\text{CS}}$	$\overline{\text{INC}}$	$\text{U}/\overline{\text{D}}$	MODE
L		H	Wiper up
L		L	Wiper down
	H	X	Store wiper position
H	X	X	Standby current
	L	X	No store, return to standby
	L	H	Wiper up (not recommended)
	L	L	Wiper down (not recommended)

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Absolute Maximum Ratings

Temperature Under Bias -65°C to +135°C
 Storage Temperature -65°C to +150°C
 Voltage on CS, INC, U/D, and
 V_{CC} with respect to V_{SS} -1V to +7V
 Voltage on V_H, V_L, V_W
 with respect to V_{SS} -6V to +7V
 $\Delta V = |V_H - V_L|$:
 X9313Z4V
 X9313W, X9313U10V
 Lead Temperature (soldering 10 seconds) 300°C
 I_W (10 seconds) ±8.8mA

Recommended Operating Conditions

Temperature:
 Commercial 0°C to +70°C
 Industrial -40°C to +85°C
 Supply Voltage (V_{CC}):
 X93135V ±10%
 X9313-3 3V to 5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Potentiometer Characteristics

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	LIMITS			UNIT
			MIN	TYP	MAX	
	End-to-end resistance tolerance				±20	%
V _{VH}	V _H terminal voltage		-5		+5	V
V _{VL}	V _L terminal voltage		-5		+5	V
	Power rating	R _{TOTAL} ≥ 10kΩ			10	mW
		R _{TOTAL} ≥ 1kΩ			16	mW
R _W	Wiper resistance	I _W = 1mA, V _{CC} = 5V		40	100	W
I _W	Wiper current				±4.4	mA
	Noise	Ref: 1kHz		-120		dBV
	Resolution			3		%
	Absolute linearity (Note 1)	R _{W(n)(actual)} - R _{W(n)(expected)}			±1	MI (Note 3)
	Relative linearity (Note 2)	R _{W(n+1)} - (R _{W(n)} + MI)			±0.2	MI (Note 3)
	R _{TOTAL} temperature coefficient			±300		ppm/°C
	Ratiometric temperature coefficient				±20	ppm/°C
C _H /C _L /C _W	Potentiometer capacitances	See Circuit #3		10/10/25		pF

NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = (V_{W(n)(actual)} - V_{W(n)(expected)}) = ±1 MI maximum.
2. Relative linearity is a measure of the error in step size between taps = R_{W(n+1)} - (R_{W(n)} + MI) = ±0.2 MI.
3. 1 MI = minimum increment = R_{TOT} / 31.

DC Operating Characteristics Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	LIMITS			UNIT
			MIN	TYP (Note 4)	MAX	
I_{CC}	V_{CC} active current	$\overline{CS} = V_{IL}$, $U/\overline{D} = V_{IL}$ or V_{IH} and $\overline{INC} = 0.42 / 2.4V$ @ max t_{CYC}		1	3	mA
I_{SB}	Standby supply current	$\overline{CS} = V_{CC} - 0.3V$, U/\overline{D} and $\overline{INC} = V_{SS}$ or $V_{CC} - 0.3V$		200	500	μA
I_{LI}	\overline{CS} , \overline{INC} , U/\overline{D} input leakage current	$V_{IN} = V_{SS}$ to V_{CC}			± 10	μA
V_{IH}	\overline{CS} , \overline{INC} , U/\overline{D} input HIGH current		2		$V_{CC} + 1$	V
V_{IL}	\overline{CS} , \overline{INC} , U/\overline{D} input LOW current		-1		+0.8	V
C_{IN}	\overline{CS} , \overline{INC} , U/\overline{D} input capacitance	$V_{CC} = 5V$, $V_{IN} = V_{SS}$, $T_A = 25^\circ C$, $f = 1MHz$			10	pF

NOTES:

- Typical values are for $T_A = 25^\circ C$ and nominal supply voltage.
- This parameter is periodically sampled and not 100% tested.

Endurance and Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	Years

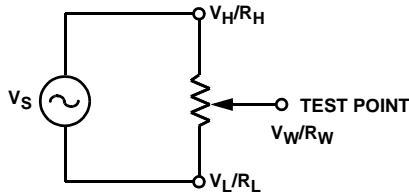


FIGURE 1. TEST CIRCUIT #1

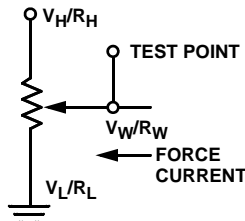


FIGURE 2. TEST CIRCUIT #2

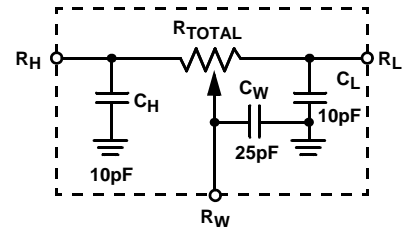


FIGURE 3. CIRCUIT #3 SPICE MACRO MODEL

AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

AC Operating Characteristics Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP (Note 6)	MAX	
t_{CI}	\overline{CS} to \overline{INC} setup	100			ns
t_{ID}	\overline{INC} HIGH to U/\overline{D} change	100			ns
t_{DI}	U/\overline{D} to \overline{INC} setup	2.9			μ s
t_{IL}	\overline{INC} LOW period	1			μ s
t_{IH}	\overline{INC} HIGH period	1			μ s
t_{IC}	\overline{INC} inactive to \overline{CS} inactive	1			μ s
t_{CPH}	\overline{CS} deselect time (STORE)	20			ms
t_{CPH}	\overline{CS} deselect time (NO STORE)	100			ns
t_{IW}	\overline{INC} to V_W change		1	5	μ s
t_{CYC}	\overline{INC} cycle time	4			μ s
t_R, t_F (Note 7)	\overline{INC} input rise and fall time			500	μ s
t_{PU} (Note 7)	Power-up to wiper stable			5	μ s
$t_R V_{CC}$ (Note 7)	V_{CC} power-up rate	0.2		50	V/ms
t_{WR}	Store cycle		5	10	ms

NOTES:

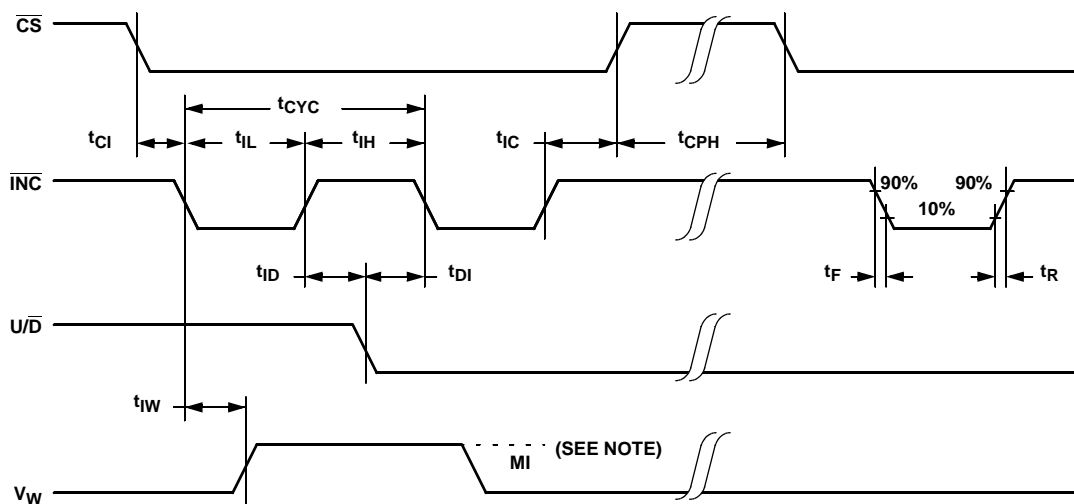
6. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

7. This parameter is not 100% tested.

Power-Up and -Down Requirements

The recommended power-up sequence is to apply V_{CC}/V_{SS} first, then the potentiometer voltages. During power-up, the data sheet parameters for the DCP do not fully apply until 1 millisecond after V_{CC} reaches its final value. The V_{CC} ramp

spec is always in effect. In order to prevent unwanted tap position changes, or an inadvertent store, bring the \overline{CS} and \overline{INC} high before or concurrently with the V_{CC} pin on power-up.

AC Timing

NOTE:

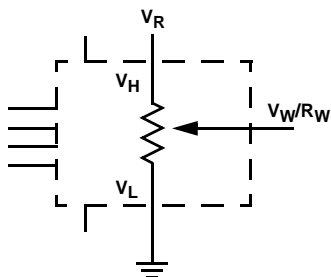
MI IN THE AC TIMING DIAGRAM REFERS TO THE MINIMUM INCREMENTAL CHANGE IN THE V_W OUTPUT DUE TO A CHANGE IN THE WIPER POSITION.

Applications Information

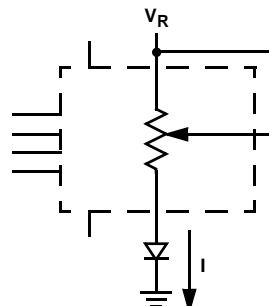
Electronic digitally controlled potentiometers (XDCP) provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of

computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



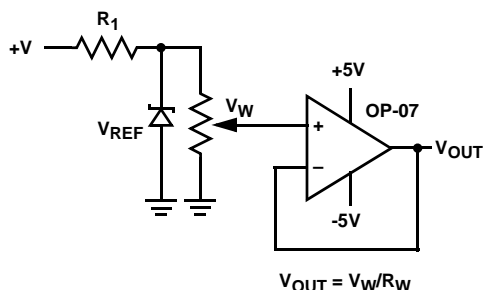
THREE-TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER



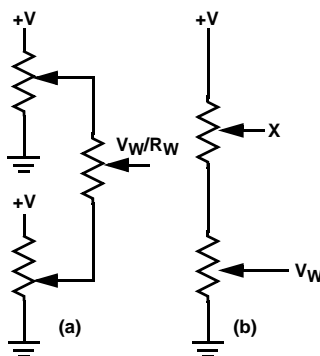
TWO-TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

Basic Circuits

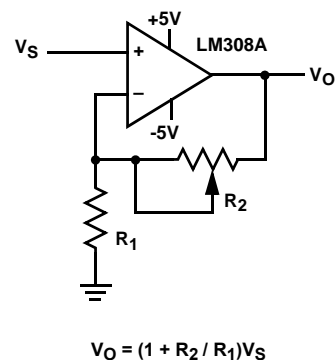
BUFFERED REFERENCE VOLTAGE



CASCADING TECHNIQUES

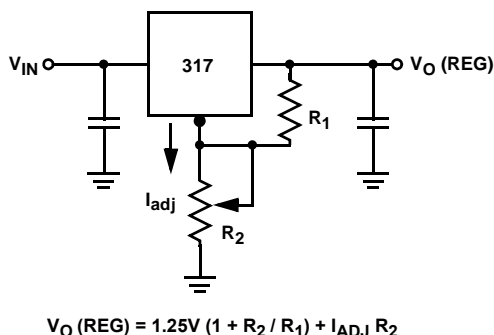


NONINVERTING AMPLIFIER

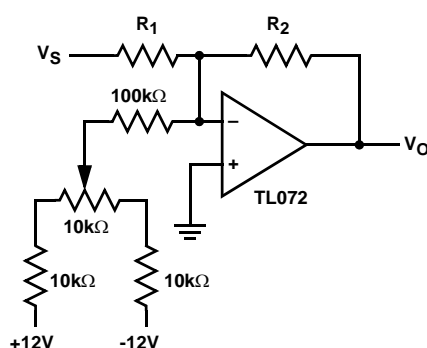


$$V_O = (1 + R_2 / R_1) V_S$$

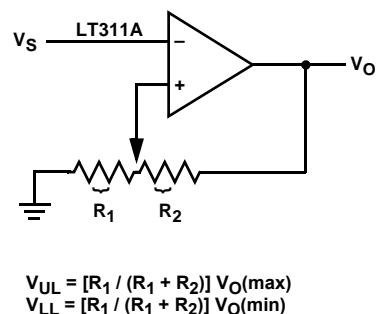
VOLTAGE REGULATOR



OFFSET VOLTAGE ADJUSTMENT



COMPARATOR WITH HYSTERESIS



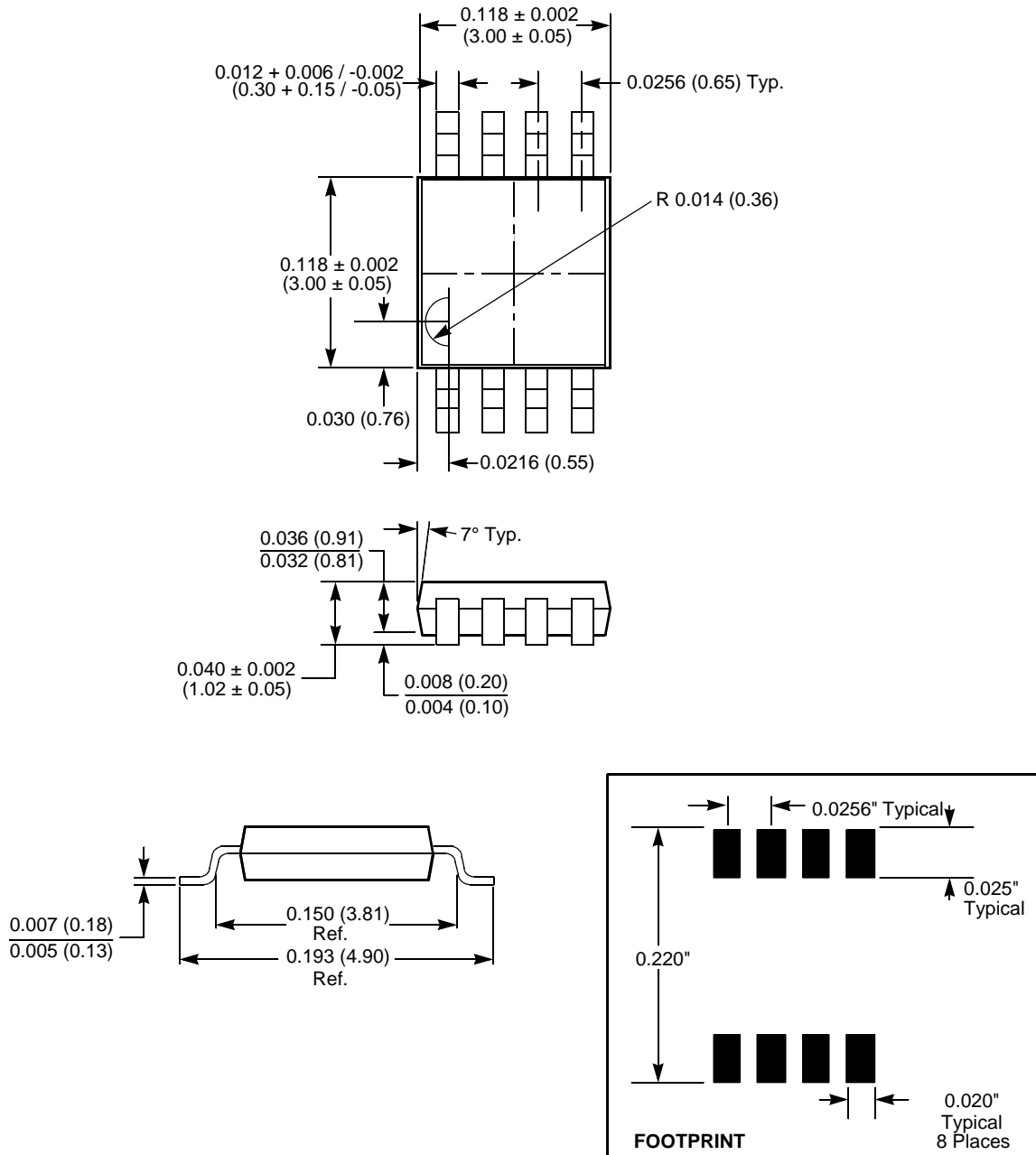
$$V_{UL} = [R_1 / (R_1 + R_2)] V_O(\max)$$

$$V_{LL} = [R_1 / (R_1 + R_2)] V_O(\min)$$

(for additional circuits see AN115)

Packaging Information

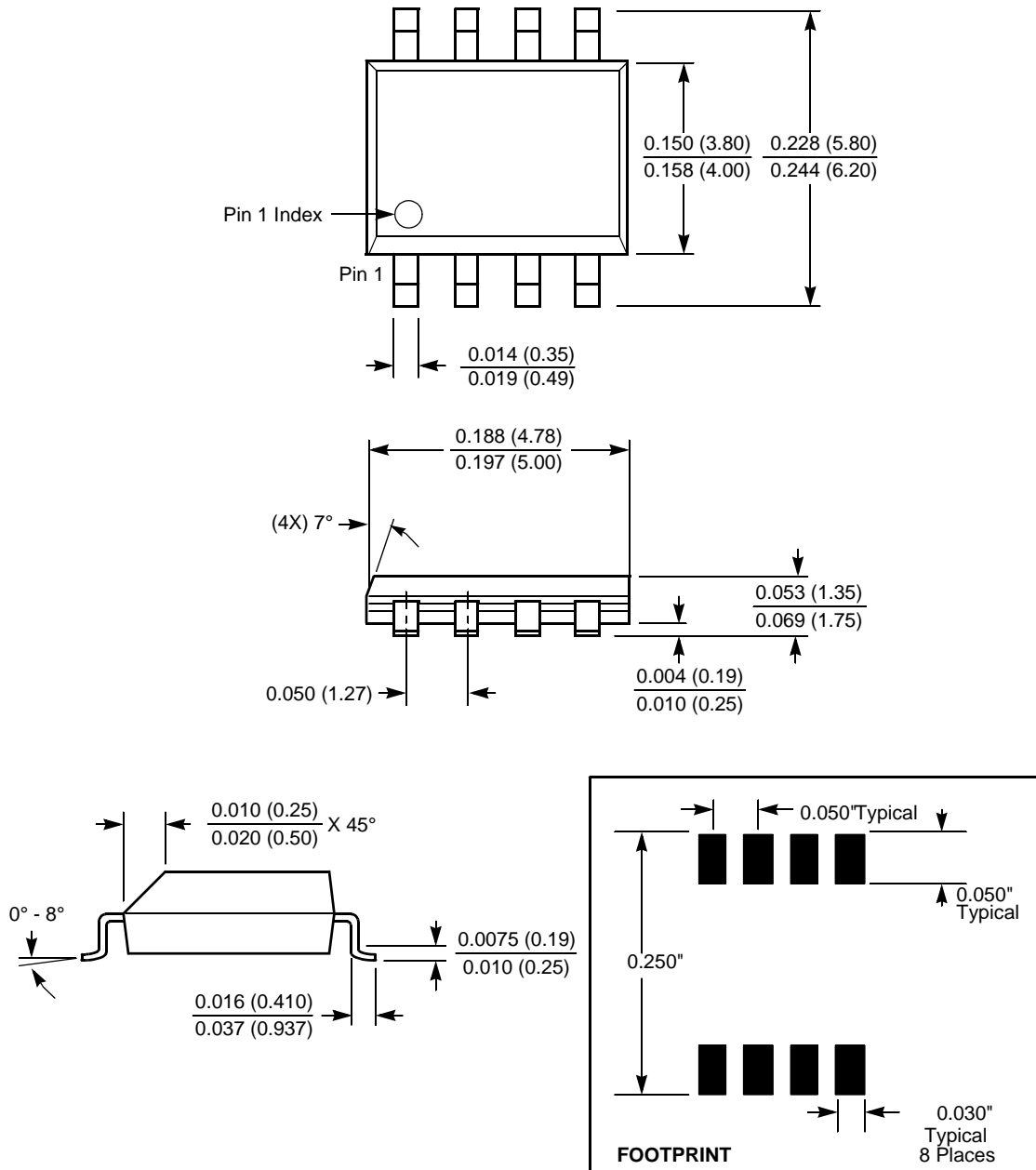
8-LEAD MINIATURE SMALL OUTLINE GULL WING PACKAGE TYPE M



NOTE ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

Packaging Information

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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