TEXAS INSTRUMENTS

PCI2050B

PCI-to-PCI Bridge

Data Manual

October 2005

Connectivity Solutions

SCPS076F

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Contents

List of Illustrations

List of Tables

1 Introduction

The Texas Instruments PCI2050B PCI-to-PCI bridge provides a high performance connection path between two peripheral component interconnect (PCI) buses operating at a maximum bus frequency of 66-MHz. Transactions occur between masters on one and targets on another PCI bus, and the PCI2050B bridge allows bridged transactions to occur concurrently on both buses. The bridge supports burst mode transfers to maximize data throughput, and the two bus traffic paths through the bridge act independently.

The PCI2050B bridge is compliant with the *PCI Local Bus Specification*, and can be used to overcome the electrical loading limits of 10 devices per PCI bus and one PCI device per extension slot by creating hierarchical buses. The PCI2050B provides two-tier internal arbitration for up to nine secondary bus masters and may be implemented with an external bus arbiter.

The CompactPCI™ hot-swap extended PCI capability makes the PCI2050B bridge an ideal solution for multifunction compact PCI cards and adapting single function cards to hot-swap compliance.

The PCI2050B bridge is compliant with the *PCI-to-PCI Bridge Specification* (Revision 1.1). The PCI2050B bridge provides compliance for *PCI Bus Power Management Interface Specification* (Revision 1.1). The PCI2050B bridge has been designed to lead the industry in power conservation and data throughput. An advanced CMOS process achieves low system power consumption while operating at PCI clock rates up to 66-MHz.

1.1 Features

The PCI2050B bridge supports the following features:

- Two 32-bit, 66-MHz PCI buses
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Internal two-tier arbitration for up to nine secondary bus masters and supports an external secondary bus arbiter
- Ten secondary PCI clock outputs
- Independent read and write buffers for each direction
- Burst data transfers with pipeline architecture to maximize data throughput in both directions
- Supports write combing for enhanced data throughput
- Up to three delayed transactions in both directions
- Supports the frame-to-frame delay of only four PCI clocks from one bus to another
- Bus locking propagation
- Predictable latency per *PCI Local Bus Specification*
- Architecture configurable for *PCI Bus Power Management Interface Specification*
- CompactPCI hot-swap functionality
- Secondary bus is driven low during reset
- VGA/palette memory and I/O decoding options
- Advanced submicron, low-power CMOS technology
- 208-terminal PDV, 208-terminal PPM, or 257-terminal MicroStar BGA™ package

1.2 Related Documents

- *Advanced Configuration and Power Interface (ACPI) Specification* (Revision 1.0)
- *IEEE Standard Test Access Port and Boundary-Scan Architecture*
- *PCI Local Bus Specification* (Revision 2.2)
- *PCI-to-PCI Bridge Specification* (Revision 1.1)
- *PCI Bus Power Management Interface Specification* (Revision 1.1)
- *PICMG CompactPCI Hot-Swap Specification* (Revision 1.0)

1.3 Trademarks

1.4 Ordering Information

ORDERING NUMBER	VOLTAGE	TEMPERATURE	PACKAGE
PCI2050BPDV	3.3-V, 5-V Tolerant I/Os	0°C to 70°C	208 QFP
PCI2050BPPM	3.3-V, 5-V Tolerant I/Os	0°C to 70°C	208 QFP
PCI2050BGHK	3.3-V, 5-V Tolerant I/Os	0°C to 70°C	257 BGA
PCI2050BZHK	3.3-V, 5-V Tolerant I/Os	0°C to 70°C	257 RoHS BGA
PCI2050BIPDV	3.3-V, 5-V Tolerant I/Os	−40°C to 85°C	208 QFP
PCI2050BIGHK	3.3-V, 5-V Tolerant I/Os	−40°C to 85°C	257 BGA
PCI2050BIZHK	3.3-V, 5-V Tolerant I/Os	−40°C to 85°C	257 RoHS BGA

2 Terminal Descriptions

The PCI2050B device is available in four packages, a 257-terminal GHK MicroStar BGA™ package, a 257-terminal RoHS-compliant ZHK MicroStar BGA™ package, a 208-terminal PDV package, or a 208-terminal PPM package. The GHK and ZHK packages are mechanically and electrically identical, but the ZHK is a RoHS-compliant design. Throughout the remainder of this manual, only the GHK package designator is used for either the GHK or the ZHK package. Figure 2−1 is the GHK-package terminal diagram. Figure 2−2 is the PDV-package terminal diagram. Figure 2−3 is the PPM-package terminal diagram. Table 2−1 lists terminals on the PDV packaged device in increasing numerical order with the signal name for each. Table 2−2 lists terminals on the PPM packaged device in increasing alphanumerical order with the signal name for each. Table 2−3 lists terminals on the GHK packaged device in increasing alphanumerical order with the signal name for each. Table 2−4, Table 2−5, and Table 2−6 list the signal names in alphabetical order, with corresponding terminal numbers for each package type.

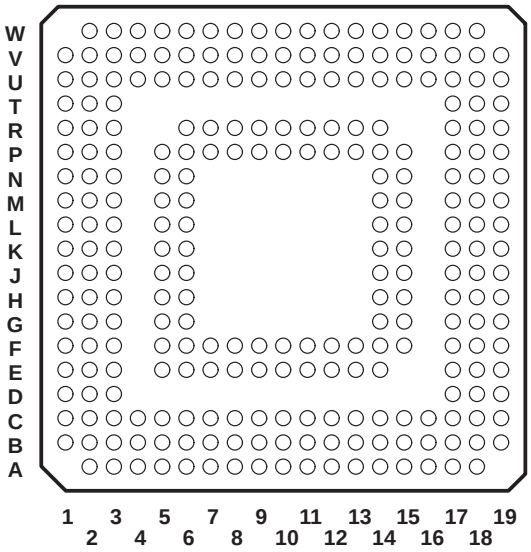


Figure 2−1. PCI2050B GHK/ZHK Terminal Diagram

PDV LOW-PROFILE QUAD FLAT PACKAGE
TOP VIEW

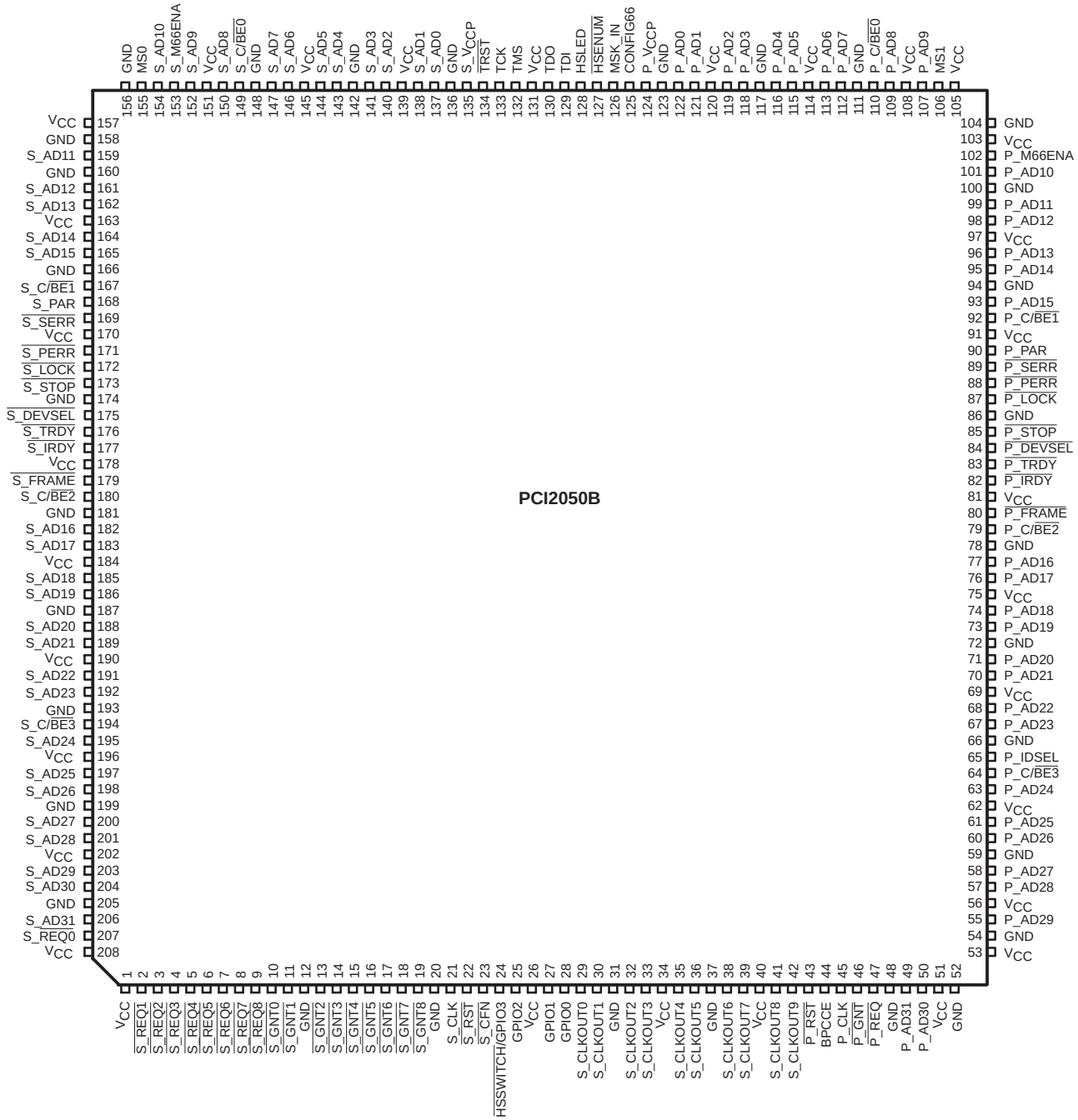


Figure 2−2. PCI2050B PDV Terminal Diagram

PPM QUAD FLAT PACKAGE
TOP VIEW

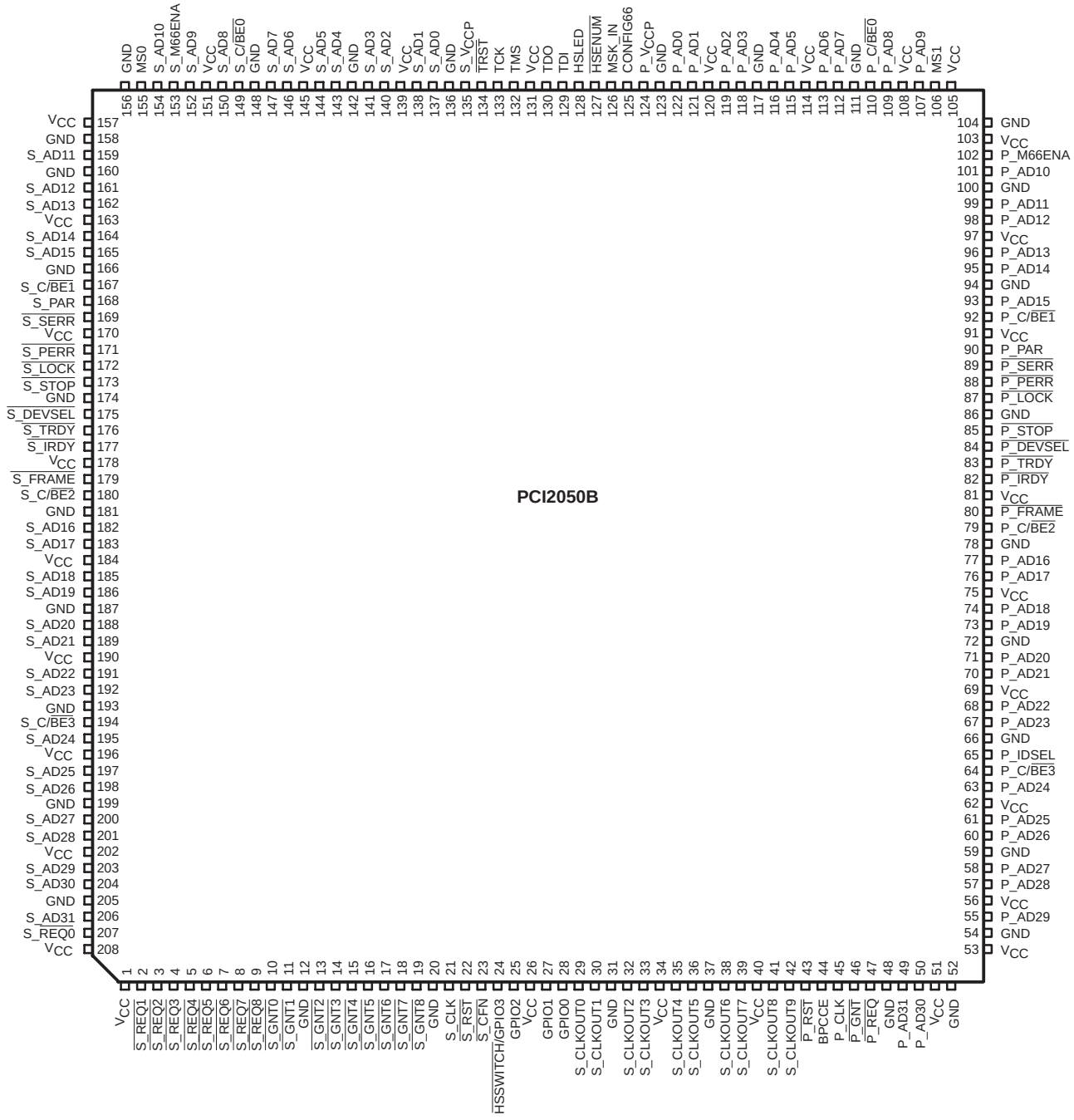


Figure 2−3. PCI2050B PPM Terminal Diagram

Table 2−1. 208-Terminal PDV Signal Names Sorted by Terminal Number

PDV NO.	SIGNAL NAME	PDV NO.	SIGNAL NAME	PDV NO.	SIGNAL NAME	PDV NO.	SIGNAL NAME	PDV NO.	SIGNAL NAME
1	V_{CC}	43	$\overline{\text{P\_RST}}$	85	$\overline{\text{P\_STOP}}$	127	$\overline{\text{HS\_ENUM}}$	169	$\overline{\text{S\_SERR}}$
2	$\overline{\text{S\_REQ1}}$	44	BPCCE	86	GND	128	HS_LED	170	V_{CC}
3	$\overline{\text{S\_REQ2}}$	45	P_CLK	87	$\overline{\text{P\_LOCK}}$	129	TDI	171	$\overline{\text{S\_PERR}}$
4	$\overline{\text{S\_REQ3}}$	46	$\overline{\text{P\_GNT}}$	88	$\overline{\text{P\_PERR}}$	130	TDO	172	$\overline{\text{S\_LOCK}}$
5	$\overline{\text{S\_REQ4}}$	47	$\overline{\text{P\_REQ}}$	89	$\overline{\text{P\_SERR}}$	131	V_{CC}	173	$\overline{\text{S\_STOP}}$
6	$\overline{\text{S\_REQ5}}$	48	GND	90	P_PAR	132	TMS	174	GND
7	$\overline{\text{S\_REQ6}}$	49	P_AD31	91	V_{CC}	133	TCK	175	$\overline{\text{S\_DEVSEL}}$
8	$\overline{\text{S\_REQ7}}$	50	P_AD30	92	P_C/$\overline{\text{BE1}}$	134	$\overline{\text{TRST}}$	176	$\overline{\text{S\_TRDY}}$
9	$\overline{\text{S\_REQ8}}$	51	V_{CC}	93	P_AD15	135	S_V_{CCP}	177	$\overline{\text{S\_IRDY}}$
10	$\overline{\text{S\_GNT0}}$	52	GND	94	GND	136	GND	178	V_{CC}
11	$\overline{\text{S\_GNT1}}$	53	V_{CC}	95	P_AD14	137	S_AD0	179	$\overline{\text{S\_FRAME}}$
12	GND	54	GND	96	P_AD13	138	S_AD1	180	S_C/$\overline{\text{BE2}}$
13	$\overline{\text{S\_GNT2}}$	55	P_AD29	97	V_{CC}	139	V_{CC}	181	GND
14	$\overline{\text{S\_GNT3}}$	56	V_{CC}	98	P_AD12	140	S_AD2	182	S_AD16
15	$\overline{\text{S\_GNT4}}$	57	P_AD28	99	P_AD11	141	S_AD3	183	S_AD17
16	$\overline{\text{S\_GNT5}}$	58	P_AD27	100	GND	142	GND	184	V_{CC}
17	$\overline{\text{S\_GNT6}}$	59	GND	101	P_AD10	143	S_AD4	185	S_AD18
18	$\overline{\text{S\_GNT7}}$	60	P_AD26	102	P_M66ENA	144	S_AD5	186	S_AD19
19	$\overline{\text{S\_GNT8}}$	61	P_AD25	103	V_{CC}	145	V_{CC}	187	GND
20	GND	62	V_{CC}	104	GND	146	S_AD6	188	S_AD20
21	S_CLK	63	P_AD24	105	V_{CC}	147	S_AD7	189	S_AD21
22	$\overline{\text{S\_RST}}$	64	P_C/$\overline{\text{BE3}}$	106	MS1	148	GND	190	V_{CC}
23	$\overline{\text{S\_CFN}}$	65	P_IDSEL	107	P_AD9	149	S_C/$\overline{\text{BE0}}$	191	S_AD22
24	$\overline{\text{HS\_SWITCH}}$/GPIO3	66	GND	108	V_{CC}	150	S_AD8	192	S_AD23
25	GPIO2	67	P_AD23	109	P_AD8	151	V_{CC}	193	GND
26	V_{CC}	68	P_AD22	110	P_C/$\overline{\text{BE0}}$	152	S_AD9	194	S_C/$\overline{\text{BE3}}$
27	GPIO1	69	V_{CC}	111	GND	153	S_M66ENA	195	S_AD24
28	GPIO0	70	P_AD21	112	P_AD7	154	S_AD10	196	V_{CC}
29	S_CLKOUT0	71	P_AD20	113	P_AD6	155	MS0	197	S_AD25
30	S_CLKOUT1	72	GND	114	V_{CC}	156	GND	198	S_AD26
31	GND	73	P_AD19	115	P_AD5	157	V_{CC}	199	GND
32	S_CLKOUT2	74	P_AD18	116	P_AD4	158	GND	200	S_AD27
33	S_CLKOUT3	75	V_{CC}	117	GND	159	S_AD11	201	S_AD28
34	V_{CC}	76	P_AD17	118	P_AD3	160	GND	202	V_{CC}
35	S_CLKOUT4	77	P_AD16	119	P_AD2	161	S_AD12	203	S_AD29
36	S_CLKOUT5	78	GND	120	V_{CC}	162	S_AD13	204	S_AD30
37	GND	79	P_C/$\overline{\text{BE2}}$	121	P_AD1	163	V_{CC}	205	GND
38	S_CLKOUT6	80	$\overline{\text{P\_FRAME}}$	122	P_AD0	164	S_AD14	206	S_AD31
39	S_CLKOUT7	81	V_{CC}	123	GND	165	S_AD15	207	$\overline{\text{S\_REQ0}}$
40	V_{CC}	82	$\overline{\text{P\_IRDY}}$	124	P_V_{CCP}	166	GND	208	V_{CC}
41	S_CLKOUT8	83	$\overline{\text{P\_TRDY}}$	125	CONFIG66	167	S_C/$\overline{\text{BE1}}$		
42	S_CLKOUT9	84	$\overline{\text{P\_DEVSEL}}$	126	MSK_IN	168	S_PAR		

Table 2−2. 208-Terminal PPM Signal Names Sorted by Terminal Number

PPM NO.	SIGNAL NAME	PPM NO.	SIGNAL NAME	PPM NO.	SIGNAL NAME	PPM NO.	SIGNAL NAME	PPM NO.	SIGNAL NAME
1	V_{CC}	43	$\overline{\text{P\_RST}}$	85	$\overline{\text{P\_STOP}}$	127	$\overline{\text{HS\_ENUM}}$	169	$\overline{\text{S\_SERR}}$
2	$\overline{\text{S\_REQ1}}$	44	BPCCE	86	GND	128	HS_LED	170	V_{CC}
3	$\overline{\text{S\_REQ2}}$	45	P_CLK	87	$\overline{\text{P\_LOCK}}$	129	TDI	171	$\overline{\text{S\_PERR}}$
4	$\overline{\text{S\_REQ3}}$	46	$\overline{\text{P\_GNT}}$	88	$\overline{\text{P\_PERR}}$	130	TDO	172	$\overline{\text{S\_LOCK}}$
5	$\overline{\text{S\_REQ4}}$	47	$\overline{\text{P\_REQ}}$	89	$\overline{\text{P\_SERR}}$	131	V_{CC}	173	$\overline{\text{S\_STOP}}$
6	$\overline{\text{S\_REQ5}}$	48	GND	90	P_PAR	132	TMS	174	GND
7	$\overline{\text{S\_REQ6}}$	49	P_AD31	91	V_{CC}	133	TCK	175	$\overline{\text{S\_DEVSEL}}$
8	$\overline{\text{S\_REQ7}}$	50	P_AD30	92	P_C/$\overline{\text{BE1}}$	134	$\overline{\text{TRST}}$	176	$\overline{\text{S\_TRDY}}$
9	$\overline{\text{S\_REQ8}}$	51	V_{CC}	93	P_AD15	135	S_V_{CCP}	177	$\overline{\text{S\_IRDY}}$
10	$\overline{\text{S\_GNT0}}$	52	GND	94	GND	136	GND	178	V_{CC}
11	$\overline{\text{S\_GNT1}}$	53	V_{CC}	95	P_AD14	137	S_AD0	179	$\overline{\text{S\_FRAME}}$
12	GND	54	GND	96	P_AD13	138	S_AD1	180	S_C/$\overline{\text{BE2}}$
13	$\overline{\text{S\_GNT2}}$	55	P_AD29	97	V_{CC}	139	V_{CC}	181	GND
14	$\overline{\text{S\_GNT3}}$	56	V_{CC}	98	P_AD12	140	S_AD2	182	S_AD16
15	$\overline{\text{S\_GNT4}}$	57	P_AD28	99	P_AD11	141	S_AD3	183	S_AD17
16	$\overline{\text{S\_GNT5}}$	58	P_AD27	100	GND	142	GND	184	V_{CC}
17	$\overline{\text{S\_GNT6}}$	59	GND	101	P_AD10	143	S_AD4	185	S_AD18
18	$\overline{\text{S\_GNT7}}$	60	P_AD26	102	P_M66ENA	144	S_AD5	186	S_AD19
19	$\overline{\text{S\_GNT8}}$	61	P_AD25	103	V_{CC}	145	V_{CC}	187	GND
20	GND	62	V_{CC}	104	GND	146	S_AD6	188	S_AD20
21	S_CLK	63	P_AD24	105	V_{CC}	147	S_AD7	189	S_AD21
22	$\overline{\text{S\_RST}}$	64	P_C/$\overline{\text{BE3}}$	106	MS1	148	GND	190	V_{CC}
23	$\overline{\text{S\_CFN}}$	65	P_IDSEL	107	P_AD9	149	S_C/$\overline{\text{BE0}}$	191	S_AD22
24	$\overline{\text{HS\_SWITCH}}$/GPIO3	66	GND	108	V_{CC}	150	S_AD8	192	S_AD23
25	GPIO2	67	P_AD23	109	P_AD8	151	V_{CC}	193	GND
26	V_{CC}	68	P_AD22	110	P_C/$\overline{\text{BE0}}$	152	S_AD9	194	S_C/$\overline{\text{BE3}}$
27	GPIO1	69	V_{CC}	111	GND	153	S_M66ENA	195	S_AD24
28	GPIO0	70	P_AD21	112	P_AD7	154	S_AD10	196	V_{CC}
29	S_CLKOUT0	71	P_AD20	113	P_AD6	155	MS0	197	S_AD25
30	S_CLKOUT1	72	GND	114	V_{CC}	156	GND	198	S_AD26
31	GND	73	P_AD19	115	P_AD5	157	V_{CC}	199	GND
32	S_CLKOUT2	74	P_AD18	116	P_AD4	158	GND	200	S_AD27
33	S_CLKOUT3	75	V_{CC}	117	GND	159	S_AD11	201	S_AD28
34	V_{CC}	76	P_AD17	118	P_AD3	160	GND	202	V_{CC}
35	S_CLKOUT4	77	P_AD16	119	P_AD2	161	S_AD12	203	S_AD29
36	S_CLKOUT5	78	GND	120	V_{CC}	162	S_AD13	204	S_AD30
37	GND	79	P_C/$\overline{\text{BE2}}$	121	P_AD1	163	V_{CC}	205	GND
38	S_CLKOUT6	80	$\overline{\text{P\_FRAME}}$	122	P_AD0	164	S_AD14	206	S_AD31
39	S_CLKOUT7	81	V_{CC}	123	GND	165	S_AD15	207	$\overline{\text{S\_REQ0}}$
40	V_{CC}	82	$\overline{\text{P\_IRDY}}$	124	P_V_{CCP}	166	GND	208	V_{CC}
41	S_CLKOUT8	83	$\overline{\text{P\_TRDY}}$	125	CONFIG66	167	S_C/$\overline{\text{BE1}}$		
42	S_CLKOUT9	84	$\overline{\text{P\_DEVSEL}}$	126	MSK_IN	168	S_PAR		

Table 2−3. 257-Terminal GHK/ZHK Signal Names Sorted by Terminal Number

GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME
A2	NC	C8	V_{CC}	F11	$\overline{\text{S\_FRAME}}$	K14	TMS	P10	P_C/$\overline{\text{BE2}}$
A3	V_{CC}	C9	S_AD18	F12	S_C/$\overline{\text{BE1}}$	K15	V_{CC}	P11	$\overline{\text{P\_TRDY}}$
A4	S_AD31	C10	NC	F13	GND	K17	TDO	P12	$\overline{\text{P\_LOCK}}$
A5	S_AD28	C11	$\overline{\text{S\_IRDY}}$	F14	S_AD9	K18	TDI	P13	P_C/$\overline{\text{BE1}}$
A6	S_AD25	C12	$\overline{\text{S\_LOCK}}$	F15	S_AD10	K19	NC	P14	P_AD12
A7	GND	C13	S_PAR	F17	S_AD8	L1	S_CLKOUT0	P15	V_{CC}
A8	S_AD20	C14	V_{CC}	F18	GND	L2	S_CLKOUT1	P17	P_AD7
A9	V_{CC}	C15	GND	F19	S_AD7	L3	NC	P18	P_AD6
A10	S_C/$\overline{\text{BE2}}$	C16	NC	G1	$\overline{\text{S\_GNT3}}$	L5	S_CLKOUT2	P19	P_AD5
A11	$\overline{\text{S\_DEVSEL}}$	C17	NC	G2	$\overline{\text{S\_GNT2}}$	L6	GND	R1	$\overline{\text{P\_GNT}}$
A12	GND	C18	NC	G3	GND	L14	HS_LED	R2	NC
A13	V_{CC}	C19	NC	G5	$\overline{\text{S\_REQ8}}$	L15	$\overline{\text{HS\_ENUM}}$	R3	P_AD31
A14	GND	D1	NC	G6	$\overline{\text{S\_REQ3}}$	L17	MSK_IN	R6	P_AD29
A15	S_AD13	D2	V_{CC}	G14	S_AD6	L18	CONFIG66	R7	P_AD26
A16	V_{CC}	D3	NC	G15	S_C/$\overline{\text{BE0}}$	L19	P_V_{CCP}	R8	GND
A17	NC	D17	NC	G17	V_{CC}	M1	S_CLKOUT3	R9	P_AD19
A18	NC	D18	NC	G18	S_AD5	M2	V_{CC}	R10	GND
B1	NC	D19	GND	G19	S_AD4	M3	S_CLKOUT4	R11	$\overline{\text{P\_DEVSEL}}$
B2	NC	E1	$\overline{\text{S\_REQ5}}$	H1	$\overline{\text{S\_GNT7}}$	M5	GND	R12	$\overline{\text{P\_PERR}}$
B3	NC	E2	$\overline{\text{S\_REQ4}}$	H2	$\overline{\text{S\_GNT6}}$	M6	S_CLKOUT5	R13	P_AD14
B4	$\overline{\text{S\_REQ0}}$	E3	$\overline{\text{S\_REQ1}}$	H3	$\overline{\text{S\_GNT5}}$	M14	P_AD4	R14	GND
B5	S_AD29	E5†	NC	H5	$\overline{\text{S\_GNT4}}$	M15	V_{CC}	R17	P_AD9
B6	S_AD26	E6	S_AD30	H6	$\overline{\text{S\_GNT1}}$	M17	P_AD1	R18	P_C/$\overline{\text{BE0}}$
B7	S_C/$\overline{\text{BE3}}$	E7	GND	H14	S_AD3	M18	P_AD0	R19	GND
B8	S_AD21	E8	S_AD23	H15	GND	M19	GND	T1	P_AD30
B9	NC	E9	GND	H17	S_AD2	N1	S_CLKOUT6	T2	V_{CC}
B10	GND	E10	S_AD16	H18	V_{CC}	N2	S_CLKOUT7	T3	NC
B11	$\overline{\text{S\_TRDY}}$	E11	V_{CC}	H19	S_AD1	N3	V_{CC}	T17	NC
B12	$\overline{\text{S\_STOP}}$	E12	$\overline{\text{S\_PERR}}$	J1	$\overline{\text{S\_GNT8}}$	N5	BPCCE	T18	V_{CC}
B13	$\overline{\text{S\_SERR}}$	E13	S_AD15	J2	GND	N6	S_CLKOUT8	T19	MS1
B14	S_AD14	E14	S_AD11	J3	S_CLK	N14	P_AD8	U1	GND
B15	S_AD12	E17	MS0	J5	$\overline{\text{S\_RST}}$	N15	V_{CC}	U2	NC
B16	NC	E18	S_M66ENA	J6	$\overline{\text{S\_CFN}}$	N17	GND	U3	NC
B17	NC	E19	V_{CC}	J14	GND	N18	P_AD3	U4	NC
B18	NC	F1	$\overline{\text{S\_GNT0}}$	J15	S_AD0	N19	P_AD2	U5	GND
B19	NC	F2	$\overline{\text{S\_REQ7}}$	J17	S_V_{CCP}	P1	S_CLKOUT9	U6	P_AD27
C1	NC	F3	$\overline{\text{S\_REQ6}}$	J18	$\overline{\text{TRST}}$	P2	$\overline{\text{P\_RST}}$	U7	P_AD24
C2	NC	F5	$\overline{\text{S\_REQ2}}$	J19	TCK	P3	P_CLK	U8	P_AD23
C3	NC	F6	V_{CC}	K1	$\overline{\text{HS\_SWITCH}}$/GPIO3	P5	GND	U9	GND
C4	NC	F7	V_{CC}	K2	GPIO2	P6	$\overline{\text{P\_REQ}}$	U10	P_AD16
C5	GND	F8	S_AD22	K3	V_{CC}	P7	V_{CC}	U11	$\overline{\text{P\_IRDY}}$
C6	S_AD27	F9	S_AD19	K5	GPIO1	P8	V_{CC}	U12	GND
C7	S_AD24	F10	S_AD17	K6	GPIO0	P9	P_AD18	U13	V_{CC}

† Terminal E5 is used as a key to indicate the location of the A1 corner. It is a no-connect terminal.

Table 2−3. 257-Terminal GHK/ZHK Signal Names Sorted by Terminal Number (Continued)

GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME
U14	P_AD13	V4	NC	V13	P_PAR	W4	V_{CC}	W13	$\overline{\text{P\_SERR}}$
U15	P_AD10	V5	NC	V14	GND	W5	P_AD28	W14	P_AD15
U16	NC	V6	GND	V15	P_AD11	W6	P_AD25	W15	V_{CC}
U17	NC	V7	P_C/$\overline{\text{BE3}}$	V16	V_{CC}	W7	P_IDSEL	W16	P_M66ENA
U18	NC	V8	P_AD22	V17	NC	W8	V_{CC}	W17	NC
U19	NC	V9	P_AD20	V18	NC	W9	P_AD21	W18	NC
V1	NC	V10	P_AD17	V19	NC	W10	V_{CC}		
V2	NC	V11	V_{CC}	W2	NC	W11	$\overline{\text{P\_FRAME}}$		
V3	NC	V12	NC	W3	NC	W12	$\overline{\text{P\_STOP}}$		

Table 2−4. 208-Terminal PDV Signal Names Sorted Alphabetically

SIGNAL NAME	PDV NO.	SIGNAL NAME	PDV NO.	SIGNAL NAME	PDV NO.	SIGNAL NAME	PDV NO.	SIGNAL NAME	PDV NO.
BPCCE	44	P_AD0	122	$\overline{\text{P\_LOCK}}$	87	S_C/$\overline{\text{BE0}}$	149	$\overline{\text{S\_SERR}}$	169
CONFIG66	125	P_AD1	121	P_M66ENA	102	S_C/$\overline{\text{BE1}}$	167	$\overline{\text{S\_STOP}}$	173
GND	12	P_AD2	119	P_PAR	90	S_C/$\overline{\text{BE2}}$	180	$\overline{\text{S\_TRDY}}$	176
GND	20	P_AD3	118	$\overline{\text{P\_PERR}}$	88	S_C/$\overline{\text{BE3}}$	194	S_V_{CCP}	135
GND	31	P_AD4	116	$\overline{\text{P\_REQ}}$	47	$\overline{\text{S\_CFN}}$	23	TCK	133
GND	37	P_AD5	115	$\overline{\text{P\_RST}}$	43	S_CLK	21	TDI	129
GND	48	P_AD6	113	$\overline{\text{P\_SERR}}$	89	S_CLKOUT0	29	TDO	130
GND	52	P_AD7	112	$\overline{\text{P\_STOP}}$	85	S_CLKOUT1	30	TMS	132
GND	54	P_AD8	109	$\overline{\text{P\_TRDY}}$	83	S_CLKOUT2	32	$\overline{\text{TRST}}$	134
GND	59	P_AD9	107	P_V_{CCP}	124	S_CLKOUT3	33	V_{CC}	1
GND	66	P_AD10	101	S_AD0	137	S_CLKOUT4	35	V_{CC}	26
GND	72	P_AD11	99	S_AD1	138	S_CLKOUT5	36	V_{CC}	34
GND	78	P_AD12	98	S_AD2	140	S_CLKOUT6	38	V_{CC}	40
GND	86	P_AD13	96	S_AD3	141	S_CLKOUT7	39	V_{CC}	51
GND	94	P_AD14	95	S_AD4	143	S_CLKOUT8	41	V_{CC}	53
GND	100	P_AD15	93	S_AD5	144	S_CLKOUT9	42	V_{CC}	56
GND	104	P_AD16	77	S_AD6	146	$\overline{\text{S\_DEVSEL}}$	175	V_{CC}	62
GND	111	P_AD17	76	S_AD7	147	$\overline{\text{S\_FRAME}}$	179	V_{CC}	69
GND	117	P_AD18	74	S_AD8	150	$\overline{\text{S\_GNT0}}$	10	V_{CC}	75
GND	123	P_AD19	73	S_AD9	152	$\overline{\text{S\_GNT1}}$	11	V_{CC}	81
GND	136	P_AD20	71	S_AD10	154	$\overline{\text{S\_GNT2}}$	13	V_{CC}	91
GND	142	P_AD21	70	S_AD11	159	$\overline{\text{S\_GNT3}}$	14	V_{CC}	97
GND	148	P_AD22	68	S_AD12	161	$\overline{\text{S\_GNT4}}$	15	V_{CC}	103
GND	156	P_AD23	67	S_AD13	162	$\overline{\text{S\_GNT5}}$	16	V_{CC}	105
GND	158	P_AD24	63	S_AD14	164	$\overline{\text{S\_GNT6}}$	17	V_{CC}	108
GND	160	P_AD25	61	S_AD15	165	$\overline{\text{S\_GNT7}}$	18	V_{CC}	114
GND	166	P_AD26	60	S_AD16	182	$\overline{\text{S\_GNT8}}$	19	V_{CC}	120
GND	174	P_AD27	58	S_AD17	183	$\overline{\text{S\_IRDY}}$	177	V_{CC}	131
GND	181	P_AD28	57	S_AD18	185	$\overline{\text{S\_LOCK}}$	172	V_{CC}	139
GND	187	P_AD29	55	S_AD19	186	S_M66ENA	153	V_{CC}	145
GND	193	P_AD30	50	S_AD20	188	S_PAR	168	V_{CC}	151
GND	199	P_AD31	49	S_AD21	189	$\overline{\text{S\_PERR}}$	171	V_{CC}	202
GND	205	P_C/$\overline{\text{BE0}}$	110	S_AD22	191	$\overline{\text{S\_REQ0}}$	207	V_{CC}	208
GPIO0	28	P_C/$\overline{\text{BE1}}$	92	S_AD23	192	$\overline{\text{S\_REQ1}}$	2	V_{CC}	157
GPIO1	27	P_C/$\overline{\text{BE2}}$	79	S_AD24	195	$\overline{\text{S\_REQ2}}$	3	V_{CC}	163
GPIO2	25	P_C/$\overline{\text{BE3}}$	64	S_AD25	197	$\overline{\text{S\_REQ3}}$	4	V_{CC}	170
$\overline{\text{HS\_ENUM}}$	127	P_CLK	45	S_AD26	198	$\overline{\text{S\_REQ4}}$	5	V_{CC}	178
HS_LED	128	$\overline{\text{P\_DEVSEL}}$	84	S_AD27	200	$\overline{\text{S\_REQ5}}$	6	V_{CC}	184
$\overline{\text{HS\_SWITCH}}$/GPIO3	24	$\overline{\text{P\_FRAME}}$	80	S_AD28	201	$\overline{\text{S\_REQ6}}$	7	V_{CC}	190
MS0	155	$\overline{\text{P\_GNT}}$	46	S_AD29	203	$\overline{\text{S\_REQ7}}$	8	V_{CC}	196
MS1	106	P_IDSEL	65	S_AD30	204	$\overline{\text{S\_REQ8}}$	9		
MSK_IN	126	$\overline{\text{P\_IRDY}}$	82	S_AD31	206	$\overline{\text{S\_RST}}$	22		

Table 2−5. 208-Terminal PPM Signal Names Sorted Alphabetically

SIGNAL NAME	PPM NO.	SIGNAL NAME	PPM NO.	SIGNAL NAME	PPM NO.	SIGNAL NAME	PPM NO.	SIGNAL NAME	PPM NO.
BPCCE	44	P_AD0	122	$\overline{\text{P\_LOCK}}$	87	S_C/$\overline{\text{BE0}}$	149	$\overline{\text{S\_SERR}}$	169
CONFIG66	125	P_AD1	121	P_M66ENA	102	S_C/$\overline{\text{BE1}}$	167	$\overline{\text{S\_STOP}}$	173
GND	12	P_AD2	119	P_PAR	90	S_C/$\overline{\text{BE2}}$	180	$\overline{\text{S\_TRDY}}$	176
GND	20	P_AD3	118	$\overline{\text{P\_PERR}}$	88	S_C/$\overline{\text{BE3}}$	194	S_V_{CCP}	135
GND	31	P_AD4	116	$\overline{\text{P\_REQ}}$	47	$\overline{\text{S\_CFN}}$	23	TCK	133
GND	37	P_AD5	115	$\overline{\text{P\_RST}}$	43	S_CLK	21	TDI	129
GND	48	P_AD6	113	$\overline{\text{P\_SERR}}$	89	S_CLKOUT0	29	TDO	130
GND	52	P_AD7	112	$\overline{\text{P\_STOP}}$	85	S_CLKOUT1	30	TMS	132
GND	54	P_AD8	109	$\overline{\text{P\_TRDY}}$	83	S_CLKOUT2	32	$\overline{\text{TRST}}$	134
GND	59	P_AD9	107	P_V_{CCP}	124	S_CLKOUT3	33	V_{CC}	1
GND	66	P_AD10	101	S_AD0	137	S_CLKOUT4	35	V_{CC}	26
GND	72	P_AD11	99	S_AD1	138	S_CLKOUT5	36	V_{CC}	34
GND	78	P_AD12	98	S_AD2	140	S_CLKOUT6	38	V_{CC}	40
GND	86	P_AD13	96	S_AD3	141	S_CLKOUT7	39	V_{CC}	51
GND	94	P_AD14	95	S_AD4	143	S_CLKOUT8	41	V_{CC}	53
GND	100	P_AD15	93	S_AD5	144	S_CLKOUT9	42	V_{CC}	56
GND	104	P_AD16	77	S_AD6	146	$\overline{\text{S\_DEVSEL}}$	175	V_{CC}	62
GND	111	P_AD17	76	S_AD7	147	$\overline{\text{S\_FRAME}}$	179	V_{CC}	69
GND	117	P_AD18	74	S_AD8	150	$\overline{\text{S\_GNT0}}$	10	V_{CC}	75
GND	123	P_AD19	73	S_AD9	152	$\overline{\text{S\_GNT1}}$	11	V_{CC}	81
GND	136	P_AD20	71	S_AD10	154	$\overline{\text{S\_GNT2}}$	13	V_{CC}	91
GND	142	P_AD21	70	S_AD11	159	$\overline{\text{S\_GNT3}}$	14	V_{CC}	97
GND	148	P_AD22	68	S_AD12	161	$\overline{\text{S\_GNT4}}$	15	V_{CC}	103
GND	156	P_AD23	67	S_AD13	162	$\overline{\text{S\_GNT5}}$	16	V_{CC}	105
GND	158	P_AD24	63	S_AD14	164	$\overline{\text{S\_GNT6}}$	17	V_{CC}	108
GND	160	P_AD25	61	S_AD15	165	$\overline{\text{S\_GNT7}}$	18	V_{CC}	114
GND	166	P_AD26	60	S_AD16	182	$\overline{\text{S\_GNT8}}$	19	V_{CC}	120
GND	174	P_AD27	58	S_AD17	183	$\overline{\text{S\_IRDY}}$	177	V_{CC}	131
GND	181	P_AD28	57	S_AD18	185	$\overline{\text{S\_LOCK}}$	172	V_{CC}	139
GND	187	P_AD29	55	S_AD19	186	S_M66ENA	153	V_{CC}	145
GND	193	P_AD30	50	S_AD20	188	S_PAR	168	V_{CC}	151
GND	199	P_AD31	49	S_AD21	189	$\overline{\text{S\_PERR}}$	171	V_{CC}	202
GND	205	P_C/$\overline{\text{BE0}}$	110	S_AD22	191	$\overline{\text{S\_REQ0}}$	207	V_{CC}	208
GPIO0	28	P_C/$\overline{\text{BE1}}$	92	S_AD23	192	$\overline{\text{S\_REQ1}}$	2	V_{CC}	157
GPIO1	27	P_C/$\overline{\text{BE2}}$	79	S_AD24	195	$\overline{\text{S\_REQ2}}$	3	V_{CC}	163
GPIO2	25	P_C/$\overline{\text{BE3}}$	64	S_AD25	197	$\overline{\text{S\_REQ3}}$	4	V_{CC}	170
$\overline{\text{HS\_ENUM}}$	127	P_CLK	45	S_AD26	198	$\overline{\text{S\_REQ4}}$	5	V_{CC}	178
HS_LED	128	$\overline{\text{P\_DEVSEL}}$	84	S_AD27	200	$\overline{\text{S\_REQ5}}$	6	V_{CC}	184
$\overline{\text{HS\_SWITCH}}$/GPIO3	24	$\overline{\text{P\_FRAME}}$	80	S_AD28	201	$\overline{\text{S\_REQ6}}$	7	V_{CC}	190
MS0	155	$\overline{\text{P\_GNT}}$	46	S_AD29	203	$\overline{\text{S\_REQ7}}$	8	V_{CC}	196
MS1	106	P_IDSEL	65	S_AD30	204	$\overline{\text{S\_REQ8}}$	9		
MSK_IN	126	$\overline{\text{P\_IRDY}}$	82	S_AD31	206	$\overline{\text{S\_RST}}$	22		

Table 2−6. 257-Terminal GHK/ZHK Signal Names Sorted Alphabetically

SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.
BPCCE	N5	NC	A18	NC	V19	$\overline{\text{P\_FRAME}}$	W11	S_AD29	B5
CONFIG66	L18	NC	B1	NC	W2	$\overline{\text{P\_GNT}}$	R1	S_AD30	E6
GND	A7	NC	B2	NC	W3	P_IDSEL	W7	S_AD31	A4
GND	A12	NC	B3	NC	W17	$\overline{\text{P\_IRDY}}$	U11	$\overline{\text{S\_CFN}}$	J6
GND	A14	NC	B9	NC	W18	$\overline{\text{P\_LOCK}}$	P12	S_CLK	J3
GND	B10	NC	B16	P_AD0	M18	P_M66ENA	W16	S_CLKOUT0	L1
GND	C5	NC	B17	P_AD1	M17	P_PAR	V13	S_CLKOUT1	L2
GND	C15	NC	B18	P_AD2	N19	$\overline{\text{P\_PERR}}$	R12	S_CLKOUT2	L5
GND	D19	NC	B19	P_AD3	N18	$\overline{\text{P\_REQ}}$	P6	S_CLKOUT3	M1
GND	E7	NC	C1	P_AD4	M14	$\overline{\text{P\_RST}}$	P2	S_CLKOUT4	M3
GND	E9	NC	C2	P_AD5	P19	$\overline{\text{P\_SERR}}$	W13	S_CLKOUT5	M6
GND	F13	NC	C3	P_AD6	P18	$\overline{\text{P\_STOP}}$	W12	S_CLKOUT6	N1
GND	F18	NC	C4	P_AD7	P17	$\overline{\text{P\_TRDY}}$	P11	S_CLKOUT7	N2
GND	G3	NC	C10	P_AD8	N14	P_V_{CCP}	L19	S_CLKOUT8	N6
GND	H15	NC	C16	P_AD9	R17	S_AD0	J15	S_CLKOUT9	P1
GND	J2	NC	C17	P_AD10	U15	S_AD1	H19	S_C/$\overline{\text{BE0}}$	G15
GND	J14	NC	C18	P_AD11	V15	S_AD2	H17	S_C/$\overline{\text{BE1}}$	F12
GND	L6	NC	C19	P_AD12	P14	S_AD3	H14	S_C/$\overline{\text{BE2}}$	A10
GND	M5	NC	D1	P_AD13	U14	S_AD4	G19	S_C/$\overline{\text{BE3}}$	B7
GND	M19	NC	D3	P_AD14	R13	S_AD5	G18	$\overline{\text{S\_DEVSEL}}$	A11
GND	N17	NC	D17	P_AD15	W14	S_AD6	G14	$\overline{\text{S\_FRAME}}$	F11
GND	P5	NC	D18	P_AD16	U10	S_AD7	F19	$\overline{\text{S\_GNT0}}$	F1
GND	R8	NC	E5	P_AD17	V10	S_AD8	F17	$\overline{\text{S\_GNT1}}$	H6
GND	R10	NC	K19	P_AD18	P9	S_AD9	F14	$\overline{\text{S\_GNT2}}$	G2
GND	R14	NC	L3	P_AD19	R9	S_AD10	F15	$\overline{\text{S\_GNT3}}$	G1
GND	R19	NC	R2	P_AD20	V9	S_AD11	E14	$\overline{\text{S\_GNT4}}$	H5
GND	U1	NC	T3	P_AD21	W9	S_AD12	B15	$\overline{\text{S\_GNT5}}$	H3
GND	U5	NC	T17	P_AD22	V8	S_AD13	A15	$\overline{\text{S\_GNT6}}$	H2
GND	U9	NC	U2	P_AD23	U8	S_AD14	B14	$\overline{\text{S\_GNT7}}$	H1
GND	U12	NC	U3	P_AD24	U7	S_AD15	E13	$\overline{\text{S\_GNT8}}$	J1
GND	V6	NC	U4	P_AD25	W6	S_AD16	E10	$\overline{\text{S\_IRDY}}$	C11
GND	V14	NC	U16	P_AD26	R7	S_AD17	F10	$\overline{\text{S\_LOCK}}$	C12
GPIO0	K6	NC	U17	P_AD27	U6	S_AD18	C9	S_M66ENA	E18
GPIO1	K5	NC	U18	P_AD28	W5	S_AD19	F9	S_PAR	C13
GPIO2	K2	NC	U19	P_AD29	R6	S_AD20	A8	$\overline{\text{S\_PERR}}$	E12
$\overline{\text{HS\_ENUM}}$	L15	NC	V1	P_AD30	T1	S_AD21	B8	$\overline{\text{S\_REQ0}}$	B4
HS_LED	L14	NC	V2	P_AD31	R3	S_AD22	F8	$\overline{\text{S\_REQ1}}$	E3
$\overline{\text{HS\_SWITCH}}$/GPIO3	K1	NC	V3	P_CLK	P3	S_AD23	E8	$\overline{\text{S\_REQ2}}$	F5
MSK_IN	L17	NC	V4	P_C/$\overline{\text{BE0}}$	R18	S_AD24	C7	$\overline{\text{S\_REQ3}}$	G6
MS0	E17	NC	V5	P_C/$\overline{\text{BE1}}$	P13	S_AD25	A6	$\overline{\text{S\_REQ4}}$	E2
MS1	T19	NC	V12	P_C/$\overline{\text{BE2}}$	P10	S_AD26	B6	$\overline{\text{S\_REQ5}}$	E1
NC	A2	NC	V17	P_C/$\overline{\text{BE3}}$	V7	S_AD27	C6	$\overline{\text{S\_REQ6}}$	F3
NC	A17	NC	V18	$\overline{\text{P\_DEVSEL}}$	R11	S_AD28	A5	$\overline{\text{S\_REQ7}}$	F2

Table 2−6. 257-Terminal GHK/ZHK Signal Names Sorted Alphabetically (Continued)

SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.	SIGNAL NAME	GHK NO.
$\overline{\text{S\_REQ8}}$	G5	TMS	K14	V_{CC}	E11	V_{CC}	M2	V_{CC}	V11
$\overline{\text{S\_RST}}$	J5	$\overline{\text{TRST}}$	J18	V_{CC}	E19	V_{CC}	N3	V_{CC}	V16
$\overline{\text{S\_SERR}}$	B13	V_{CC}	A3	V_{CC}	F6	V_{CC}	N15	V_{CC}	W4
$\overline{\text{S\_STOP}}$	B12	V_{CC}	A9	V_{CC}	F7	V_{CC}	P7	V_{CC}	W8
$\overline{\text{S\_TRDY}}$	B11	V_{CC}	A13	V_{CC}	M15	V_{CC}	P8	V_{CC}	W10
S_V_{CCP}	J17	V_{CC}	A16	V_{CC}	G17	V_{CC}	P15	V_{CC}	W15
TCK	J19	V_{CC}	C8	V_{CC}	H18	V_{CC}	T2		
TDI	K18	V_{CC}	C14	V_{CC}	K3	V_{CC}	T18		
TDO	K17	V_{CC}	D2	V_{CC}	K15	V_{CC}	U13		

The terminals are grouped in tables by functionality, such as PCI system function and power-supply function (see Table 2−7 through Table 2−15). The terminal numbers also are listed for convenient reference.

Table 2−7. Primary PCI System Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
P_CLK	45	P3	I	Primary PCI bus clock. P_CLK provides timing for all transactions on the primary PCI bus. All primary PCI signals are sampled at rising edge of P_CLK.
$\overline{\text{P\_RST}}$	43	P2	I	PCI reset. When the primary PCI bus reset is asserted, $\overline{\text{P\_RST}}$ causes the bridge to put all output buffers in a high-impedance state and reset all internal registers. When asserted, the device is completely nonfunctional. During $\overline{\text{P\_RST}}$, the secondary interface is driven low. After $\overline{\text{P\_RST}}$ is deasserted, the bridge is in its default state.

Table 2−8. Primary PCI Address and Data Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
P_AD31	49	R3	I/O	Primary address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, P_AD31−P_AD0 contain a 32-bit address or other destination information. During the data phase, P_AD31−P_AD0 contain data.
P_AD30	50	T1		
P_AD29	55	R6		
P_AD28	57	W5		
P_AD27	58	U6		
P_AD26	60	R7		
P_AD25	61	W6		
P_AD24	63	U7		
P_AD23	67	U8		
P_AD22	68	V8		
P_AD21	70	W9		
P_AD20	71	V9		
P_AD19	73	R9		
P_AD18	74	P9		
P_AD17	76	V10		
P_AD16	77	U10		
P_AD15	93	W14		
P_AD14	95	R13		
P_AD13	96	U14		
P_AD12	98	P14		
P_AD11	99	V15		
P_AD10	101	U15		
P_AD9	107	R17		
P_AD8	109	N14		
P_AD7	112	P17		
P_AD6	113	P18		
P_AD5	115	P19		
P_AD4	116	M14		
P_AD3	118	N18		
P_AD2	119	N19		
P_AD1	121	M17		
P_AD0	122	M18		
P_C/$\overline{\text{BE3}}$	64	V7	I/O	Primary bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, P_C/$\overline{\text{BE3}}$−P_C/$\overline{\text{BE0}}$ define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. P_C/$\overline{\text{BE0}}$ applies to byte 0 (P_AD7−P_AD0), P_C/$\overline{\text{BE1}}$ applies to byte 1 (P_AD15−P_AD8), P_C/$\overline{\text{BE2}}$ applies to byte 2 (P_AD23−P_AD16), and P_C/$\overline{\text{BE3}}$ applies to byte 3 (P_AD31−P_AD24).
P_C/$\overline{\text{BE2}}$	79	P10		
P_C/$\overline{\text{BE1}}$	92	P13		
P_C/$\overline{\text{BE0}}$	110	R18		

Table 2−9. Primary PCI Interface Control Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
P_DEVSEL	84	R11	I/O	Primary device select. The bridge asserts P_DEVSEL to claim a PCI cycle as the target device. As a PCI master on the primary bus, the bridge monitors P_DEVSEL until a target responds. If no target responds before time-out occurs, then the bridge terminates the cycle with a master abort.
P_FRAME	80	W11	I/O	Primary cycle frame. P_FRAME is driven by the master of a primary bus cycle. P_FRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When P_FRAME is deasserted, the primary bus transaction is in the final data phase.
P_GNT	46	R1	I	Primary bus grant to bridge. P_GNT is driven by the primary PCI bus arbiter to grant the bridge access to the primary PCI bus after the current data transaction has completed. P_GNT may or may not follow a primary bus request, depending on the primary bus arbitration algorithm.
P_IDSEL	65	W7	I	Primary initialization device select. P_IDSEL selects the bridge during configuration space accesses. P_IDSEL can be connected to one of the upper 24 PCI address lines on the primary PCI bus. Note: There is no IDSEL signal interfacing the secondary PCI bus; thus, the entire configuration space of the bridge can only be accessed from the primary bus.
P_IRDY	82	U11	I/O	Primary initiator ready. P_IRDY indicates ability of the primary bus master to complete the current data phase of the transaction. A data phase is completed on a rising edge of P_CLK where both P_IRDY and P_TRDY are asserted. Until P_IRDY and P_TRDY are both sampled asserted, wait states are inserted.
P_LOCK	87	P12	I/O	Primary PCI bus lock. P_LOCK is used to lock the primary bus and gain exclusive access as a bus master.
P_PAR	90	V13	I/O	Primary parity. In all primary bus read and write cycles, the bridge calculates even parity across the P_AD and P_C/BE buses. As a bus master during PCI write cycles, the bridge outputs this parity indicator with a one-P_CLK delay. As a target during PCI read cycles, the calculated parity is compared to the parity indicator of the master; a miscompare can result in a parity error assertion (P_PERR).
P_PERR	88	R12	I/O	Primary parity error indicator. P_PERR is driven by a primary bus PCI device to indicate that calculated parity does not match P_PAR when P_PERR is enabled through bit 6 of the command register (PCI offset 04h, see Section 4.3).
P_REQ	47	P6	O	Primary PCI bus request. Asserted by the bridge to request access to the primary PCI bus as a master.
P_SERR	89	W13	O	Primary system error. Output pulsed from the bridge when enabled through bit 8 of the command register (PCI offset 04h, see Section 4.3) indicating a system error has occurred. The bridge needs not be the target of the primary PCI cycle to assert this signal. When bit 6 is enabled in the bridge control register (PCI offset 3Eh, see Section 4.32), this signal also pulses, indicating that a system error has occurred on one of the subordinate buses downstream from the bridge.
P_STOP	85	W12	I/O	Primary cycle stop signal. This signal is driven by a PCI target to request that the master stop the current primary bus transaction. This signal is used for target disconnects and is commonly asserted by target devices which do not support burst data transfers.
P_TRDY	83	P11	I/O	Primary target ready. P_TRDY indicates the ability of the primary bus target to complete the current data phase of the transaction. A data phase is completed upon a rising edge of P_CLK where both P_IRDY and P_TRDY are asserted. Until both P_IRDY and P_TRDY are asserted, wait states are inserted.

Table 2−10. Secondary PCI System Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
S_CLKOUT9 S_CLKOUT8 S_CLKOUT7 S_CLKOUT6 S_CLKOUT5 S_CLKOUT4 S_CLKOUT3 S_CLKOUT2 S_CLKOUT1 S_CLKOUT0	42 41 39 38 36 35 33 32 30 29	P1 N6 N2 N1 M6 M3 M1 L5 L2 L1	O	Secondary PCI bus clocks. Provide timing for all transactions on the secondary PCI bus. Each secondary bus device samples all secondary PCI signals at the rising edge of its corresponding S_CLKOUT input.
S_CLK	21	J3	I	Secondary PCI bus clock input. This input synchronizes the PCI2050B device to the secondary bus clocks.
$\overline{\text{S\_CFN}}$	23	J6	I	Secondary external arbiter enable. When this signal is high, the secondary external arbiter is enabled. When the external arbiter is enabled, the PCI2050B $\overline{\text{S\_REQ0}}$ terminal is reconfigured as a secondary bus grant input to the bridge and $\overline{\text{S\_GNT0}}$ is reconfigured as a secondary bus master request to the external arbiter on the secondary bus.
$\overline{\text{S\_RST}}$	22	J5	O	Secondary PCI reset. $\overline{\text{S\_RST}}$ is a logical OR of $\overline{\text{P\_RST}}$ and the state of the secondary bus reset bit (bit 6) of the bridge control register (PCI offset 3Eh, see Section 4.32). $\overline{\text{S\_RST}}$ is asynchronous with respect to the state of the secondary interface CLK signal.

Table 2−11. Secondary PCI Address and Data Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
S_AD31	206	A4	I/O	Secondary address/data bus. These signals make up the multiplexed PCI address and data bus on the secondary interface. During the address phase of a secondary bus PCI cycle, S_AD31−S_AD0 contain a 32-bit address or other destination information. During the data phase, S_AD31−S_AD0 contain data.
S_AD30	204	E6		
S_AD29	203	B5		
S_AD28	201	A5		
S_AD27	200	C6		
S_AD26	198	B6		
S_AD25	197	A6		
S_AD24	195	C7		
S_AD23	192	E8		
S_AD22	191	F8		
S_AD21	189	B8		
S_AD20	188	A8		
S_AD19	186	F9		
S_AD18	185	C9		
S_AD17	183	F10		
S_AD16	182	E10		
S_AD15	165	E13		
S_AD14	164	B14		
S_AD13	162	A15		
S_AD12	161	B15		
S_AD11	159	E14		
S_AD10	154	F15		
S_AD9	152	F14		
S_AD8	150	F17		
S_AD7	147	F19		
S_AD6	146	G14		
S_AD5	144	G18		
S_AD4	143	G19		
S_AD3	141	H14		
S_AD2	140	H17		
S_AD1	138	H19		
S_AD0	137	J15		
S_C/$\overline{BE3}$	194	B7	I/O	Secondary bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a secondary bus PCI cycle, S_C/$\overline{BE3}$−S_C/$\overline{BE0}$ define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. S_C/$\overline{BE0}$ applies to byte 0 (S_AD7−S_AD0), S_C/$\overline{BE1}$ applies to byte 1 (S_AD15−S_AD8), S_C/$\overline{BE2}$ applies to byte 2 (S_AD23−S_AD16), and S_C/$\overline{BE3}$ applies to byte 3 (S_AD31−S_AD24).
S_C/$\overline{BE2}$	180	A10		
S_C/$\overline{BE1}$	167	F12		
S_C/$\overline{BE0}$	149	G15		
$\overline{S\_DEVSEL}$	175	A11	I/O	Secondary device select. The bridge asserts $\overline{S\_DEVSEL}$ to claim a PCI cycle as the target device. As a PCI master on the secondary bus, the bridge monitors $\overline{S\_DEVSEL}$ until a target responds. If no target responds before time-out occurs, then the bridge terminates the cycle with a master abort.
$\overline{S\_FRAME}$	179	F11	I/O	Secondary cycle frame. $\overline{S\_FRAME}$ is driven by the master of a secondary bus cycle. $\overline{S\_FRAME}$ is asserted to indicate that a bus transaction is beginning and data transfers continue while $\overline{S\_FRAME}$ is asserted. When $\overline{S\_FRAME}$ is deasserted, the secondary bus transaction is in the final data phase.
$\overline{S\_GNT8}$	19	J1	O	Secondary bus grant to the bridge. The bridge provides internal arbitration and these signals are used to grant potential secondary PCI bus masters access to the bus. Ten potential masters (including the bridge) can be located on the secondary PCI bus. When the internal arbiter is disabled, $\overline{S\_GNT0}$ is reconfigured as an external secondary bus request signal for the bridge.
$\overline{S\_GNT7}$	18	H1		
$\overline{S\_GNT6}$	17	H2		
$\overline{S\_GNT5}$	16	H3		
$\overline{S\_GNT4}$	15	H5		
$\overline{S\_GNT3}$	14	G1		
$\overline{S\_GNT2}$	13	G2		
$\overline{S\_GNT1}$	11	H6		
$\overline{S\_GNT0}$	10	F1		

Table 2−12. Secondary PCI Interface Control Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
S_IRDY	177	C11	I/O	Secondary initiator ready. S_IRDY indicates the ability of the secondary bus master to complete the current data phase of the transaction. A data phase is completed on a rising edge of S_CLK where both S_IRDY and S_TRDY are asserted; until S_IRDY and S_TRDY are asserted, wait states are inserted.
S_LOCK	172	C12	I/O	Secondary PCI bus lock. S_LOCK is used to lock the secondary bus and gain exclusive access as a master.
S_PAR	168	C13	I/O	Secondary parity. In all secondary bus read and write cycles, the bridge calculates even parity across the S_AD and S_C/BE buses. As a master during PCI write cycles, the bridge outputs this parity indicator with a one-S_CLK delay. As a target during PCI read cycles, the calculated parity is compared to the master parity indicator. A miscompare can result in a parity error assertion (S_PERR).
S_PERR	171	E12	I/O	Secondary parity error indicator. S_PERR is driven by a secondary bus PCI device to indicate that calculated parity does not match S_PAR when enabled through the command register (PCI offset 04h, see Section 4.3).
S_REQ8 S_REQ7 S_REQ6 S_REQ5 S_REQ4 S_REQ3 S_REQ2 S_REQ1 S_REQ0	9 8 7 6 5 4 3 2 207	G5 F2 F3 E1 E2 G6 F5 E3 B4	I	Secondary PCI bus request signals. The bridge provides internal arbitration, and these signals are used as inputs from secondary PCI bus masters requesting the bus. Ten potential masters (including the bridge) can be located on the secondary PCI bus. When the internal arbiter is disabled, the S_REQ0 signal is reconfigured as an external secondary bus grant for the bridge.
S_SERR	169	B13	I	Secondary system error. S_SERR is passed through the primary interface by the bridge if enabled through the bridge control register (PCI offset 3Eh, see Section 4.32). S_SERR is never asserted by the bridge.
S_STOP	173	B12	I/O	Secondary cycle stop signal. S_STOP is driven by a PCI target to request that the master stop the current secondary bus transaction. S_STOP is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers.
S_TRDY	176	B11	I/O	Secondary target ready. S_TRDY indicates the ability of the secondary bus target to complete the current data phase of the transaction. A data phase is completed on a rising edge of S_CLK where both S_IRDY and S_TRDY are asserted; until S_IRDY and S_TRDY are asserted, wait states are inserted.

Table 2−13. JTAG Interface Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
TCK	133	J19	I	JTAG boundary-scan clock. TCK is the clock controlling the JTAG logic.
TDI	129	K18	I	JTAG serial data in. TDI is the serial input through which JTAG instructions and test data enter the JTAG interface. The new data on TDI is sampled on the rising edge of TCK.
TDO	130	K17	O	JTAG serial data out. TDO is the serial output through which test instructions and data from the test logic leave the PCI2050B device.
TMS	132	K14	I	JTAG test mode select. TMS causes state transitions in the test access port controller.
TRST	134	J18	I	JTAG TAP reset. When TRST is asserted low, the TAP controller is asynchronously forced to enter a reset state and initialize the test logic.

Table 2−14. Miscellaneous Terminals

TERMINAL			I/O	DESCRIPTION
NAME	PDV/ PPM NO.	GHK/ ZHK NO.		
BPCCE	44	N5	I	Bus/power clock control management terminal. When this terminal is tied high and the PCI2050B device is placed in the D3 power state, it enables the PCI2050B device to place the secondary bus in the B2 power state. The PCI2050Bdevice disables the secondary clocks and drives them to 0. When tied low, placing the PCI2050B device in the D3 power state has no effect on the secondary bus clocks.
CONFIG66	125	L18	I	Configure 66 MHz operation. This input-only terminal is used to specify if the PCI2050B device is capable of running at 66 MHz. If this terminal is tied high, then device can be run at 66 MHz. If this terminal is tied low, then the PCI2050B device can only function under the 33-MHz PCI configuration.
GPIO3/$\overline{\text{HS\_SWITCH}}$ GPIO2 GPIO1 GPIO0	24 25 27 28	K1 K2 K5 K6	I	General-purpose I/O terminals GPIO3 is $\overline{\text{HS\_SWITCH}}$ in cPCI mode. $\overline{\text{HS\_SWITCH}}$ provides the status of the ejector handle switch to the cPCI logic.
$\overline{\text{HS\_ENUM}}$	127	L15	O	Hot-swap $\overline{\text{ENUM}}$
HS_LED	128	L14	O	Hot-swap LED output
MS0	155	E17	I	Mode select 0
MS1	106	T19	I	Mode select 1
P_M66ENA	102	W16	I	Primary interface 66 MHz enable. This input-only signal designates the primary interface bus speed. This terminal must be pulled low for 33-MHz operation on the primary bus. In this case, S_M66ENA signal will be driven low by the PCI2050B device, forcing the secondary bus to run at 33 MHz. For 66-MHz operation, this terminal must be pulled high.
S_M66ENA	153	E18	I/O	Secondary 66 MHz enable. This signal designates the secondary bus speed. If the P_M66ENA is driven low, then this signal is driven low by the PCI2050B device, forcing secondary bus to run at 33 MHz. If the primary bus is running at 66 MHz (P_M66ENA is high), then S_M66ENA is an input and must be externally pulled high for the secondary bus to operate at 66 MHz or pulled low for secondary bus to operate at 33 MHz. Note that S_M66ENA is an open drained output.

Table 2−15. Power Supply Terminals

TERMINAL			DESCRIPTION
NAME	PDV/PPM NO.	GHK NO.	
GND	12, 20, 31, 37, 48, 52, 54, 59, 66, 72, 78, 86, 94, 100, 104, 111, 117, 123, 136, 142, 148, 156, 158, 160, 166, 174, 181, 187, 193, 199, 205	A7, A12, A14, B10, C5, C15, D19, E7, E9, F13, F18, G3, H15, J2, J14, L6, M5, M19, N17, P5, R8, R10, R14, R19, U1, U5, U9, U12, V6, V14	Device ground terminals
V_{CC}	1, 26, 34, 40, 51, 53, 56, 62, 69, 75, 81, 91, 97, 103, 105, 108, 114, 120, 131, 139, 145, 151, 157, 163, 170, 178, 184, 190, 196, 202, 208	A3, A9, A13, A16, C8, C14, D2, E11, E19, F6, F7, M15, G17, H18, K3, K15, M2, N3, N15, P7, P8, P15, T2, T18, U13, V11, V16, W4, W8, W10, W15	Power-supply terminal for core logic (3.3 V)
P_V_{CCP}(1)	124	L19	Primary bus-signaling environment supply. P_V_{CCP} is used in protection circuitry on primary bus I/O signals.
S_V_{CCP}(1)	135	J17	Secondary bus-signaling environment supply. S_V_{CCP} is used in protection circuitry on secondary bus I/O signals.

NOTE 1: TI recommends that P_V_{CCP} and S_V_{CCP} be powered up first before applying power to V_{CC}.

3 Feature/Protocol Descriptions

The following sections give an overview of the PCI2050B PCI-to-PCI bridge features and functionality. Figure 3−1 shows a simplified block diagram of a typical system implementation using the PCI2050B bridge.

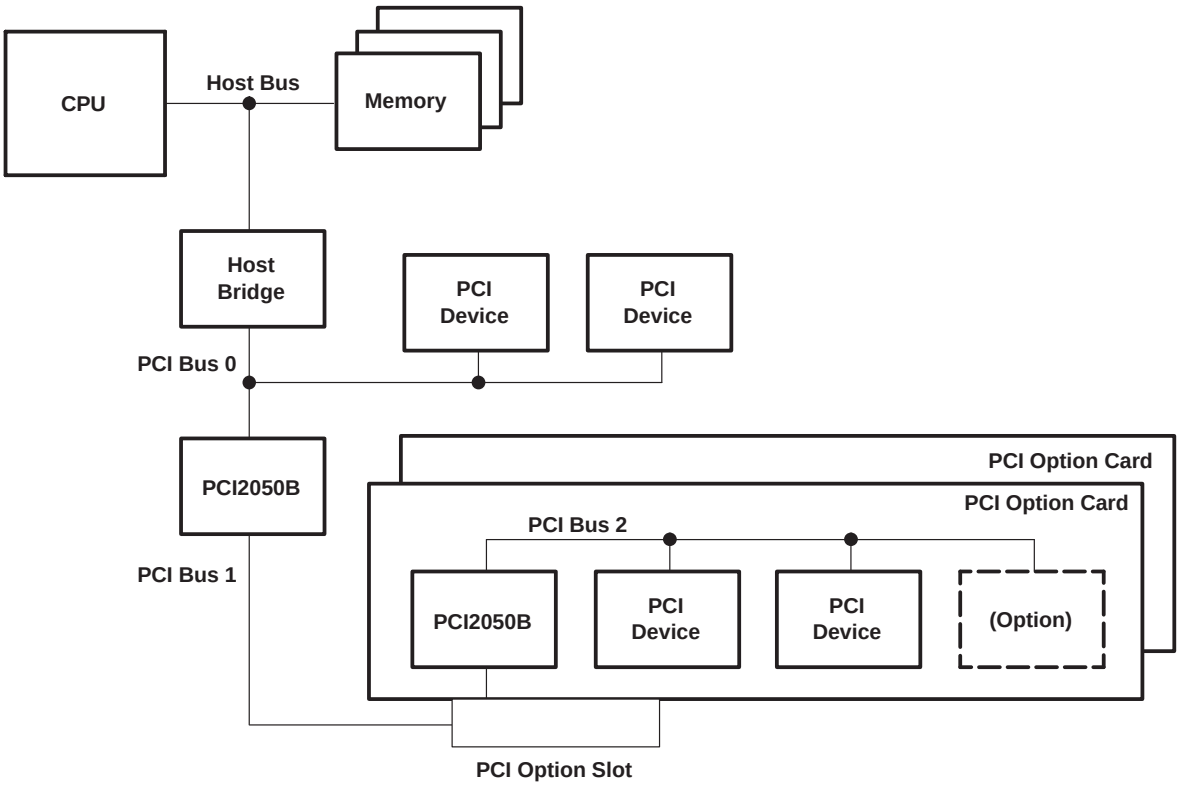


Figure 3−1. System Block Diagram

3.1 Introduction to the PCI2050B Bridge

The PCI2050B device is a bridge between two PCI buses and is compliant with both the *PCI Local Bus Specification* and the *PCI-to-PCI Bridge Specification*. The bridge supports two 32-bit PCI buses operating at a maximum of 66 MHz. The primary and secondary buses operate independently in either 3.3-V or 5-V signaling environment. The core logic of the bridge, however, is powered at 3.3 V to reduce power consumption.

For PCI2050B, the FIFO size is 32 DW for delayed responses (3 each direction) 64 DW posted write and delayed request FIFO (1 each direction).

Host software interacts with the bridge through internal registers. These internal registers provide the standard PCI status and control for both the primary and secondary buses. Many vendor-specific features that exist in the TI extension register set are included in the bridge. The PCI configuration header of the bridge is only accessible from the primary PCI interface.

The bridge provides internal arbitration for the nine possible secondary bus masters, and provides each with a dedicated active low request/grant pair ($\overline{REQ}$/$\overline{GNT}$). The arbiter features a two-tier rotational scheme with the PCI2050B bridge defaulting to the highest priority tier. The PCI2050B device also supports external arbitration.

Upon system power up, power-on self-test (POST) software configures the bridge according to the devices that exist on subordinate buses, and enables performance-enhancing features of the PCI2050B bridge. In a typical system, this is the only communication with the bridge internal register set.

3.1.1 Write Combining

The PCI2050B bridge supports write combining for upstream and downstream transactions. This feature combines separate sequential memory write transactions into a single burst transaction. This feature can only be used if the address of the next memory write transaction is the next sequential address after the address of the last double word of the previous memory transaction. For example, if the current memory transaction ends at address X and next memory transaction starts at address X+1, then the PCI2050B bridge combines both transactions into a single transaction.

The write combining feature of the PCI2050B bridge is enabled by default on power on reset. It can also be disabled by setting bit 0 of the TI diagnostics register at offset F0h to 1.

3.1.2 66-MHz Operation

The PCI2050B bridge supports two 32-bit PCI buses operating at a maximum frequency of 66 MHz. The 66-MHz clocking requires three terminals: P_M66ENA, S_M66ENA, and CONFIG66. To enable 66-MHz operation, the CONFIG66 terminal must be tied high on the board. This sets the 66-MHz capable bit in the primary and secondary status register. The P_M66ENA and S_M66ENA must not be pulled high unless CONFIG66 is also high.

The P_M66ENA and S_M66ENA signals indicate whether the primary or secondary interfaces are working at 66 MHz. This information is needed to control the frequency of the secondary bus. Note that *PCI Local Bus Specification* (Revision 2.2) restricts clock frequency changes above 33 MHz during reset only.

The following frequency combinations are supported on the primary and secondary buses in the PCI2050B device:

- 66-MHz primary bus, 66-MHz secondary bus
- 66-MHz primary bus, 33-MHz secondary bus
- 33-MHz primary bus, 33-MHz secondary bus

The PCI2050B bridge does not support 33-MHz primary/66-MHz secondary bus operation. If CONFIG66 is high and P_M66ENA is low, then the PCI2050B bridge pulls down S_M66ENA to indicate that secondary bus is running at 33 MHz.

The PCI2050B bridge generates the clock signals S_CLKOUT[9:0] for the secondary bus devices and its own interface. It divides the P_CLK by 2 to generate the secondary clock outputs whenever the primary bus is running at 66 MHz and secondary bus is running at 33 MHz. The bridge detects this condition by polling P_M66ENA and S_M66ENA.

3.2 PCI Commands

The bridge responds to PCI bus cycles as a PCI target device based on internal register settings and on the decoding of each address phase. Table 3−1 lists the valid PCI bus cycles and their encoding on the command/byte enable (C/$\overline{BE}$) bus during the address phase of a bus cycle.

Table 3−1. PCI Command Definitions

C/$\overline{BE3}$−C/$\overline{BE0}$	COMMAND
0000	Interrupt acknowledge
0001	Special cycle
0010	I/O read
0011	I/O write
0100	Reserved
0101	Reserved
0110	Memory read
0111	Memory write
1000	Reserved
1001	Reserved
1010	Configuration read
1011	Configuration write
1100	Memory read multiple
1101	Dual address cycle
1110	Memory read line
1111	Memory write and invalidate

The bridge never responds as a PCI target to the interrupt acknowledge, special cycle, or reserved commands. The bridge does, however, initiate special cycles on both interfaces when a type 1 configuration cycle issues the special cycle request. The remaining PCI commands address either memory, I/O, or configuration space. The bridge accepts PCI cycles by asserting $\overline{DEVSEL}$ as a medium-speed device, i.e., $\overline{DEVSEL}$ is asserted two clock cycles after the address phase.

The PCI2050B bridge converts memory write and invalidate commands to memory write commands when forwarding transactions from either the primary or secondary side of the bridge if the bridge cannot guarantee that an entire cache line will be delivered.

3.3 Configuration Cycles

PCI Local Bus Specification defines two types of PCI configuration read and write cycles: type 0 and type 1. The bridge decodes each type differently. Type 0 configuration cycles are intended for devices on the primary bus, while type 1 configuration cycles are intended for devices on some hierarchically subordinate bus. The difference between these two types of cycles is the encoding of the primary PCI (P_AD) bus during the address phase of the cycle. Figure 3−2 shows the P_AD bus encoding during the address phase of a type 0 configuration cycle. The 6-bit register number field represents an 8-bit address with the two lower bits masked to 0, indicating a doubleword boundary. This results in a 256-byte configuration address space per function per device. Individual byte accesses may be selected within a doubleword by using the P_C/$\overline{BE}$ signals during the data phase of the cycle.

31 11	10 8	7 2	1	0
Reserved	Function Number	Register Number	0	0

Figure 3−2. PCI AD31−AD0 During Address Phase of a Type 0 Configuration Cycle

The bridge claims only type 0 configuration cycles when its P_IDSEL terminal is asserted during the address phase of the cycle and the PCI function number encoded in the cycle is 0. If the function number is 1 or greater, then the bridge does not recognize the configuration command. In this case, the bridge does not assert $\overline{P\_DEVSEL}$, and the configuration transaction results in a master abort. The bridge services valid type 0 configuration read or write cycles by accessing internal registers from the bridge configuration header (see Table 4−1).

Because type 1 configuration cycles are issued to devices on subordinate buses, the bridge claims type 1 cycles based on the bus number of the destination bus. The P_AD bus encoding during the address phase of a type 1 cycle is shown in Figure 3−3. The device number and bus number fields define the destination bus and device for the cycle.

31 24	23 16	15 11	10 8	7 2	1	0
Reserved	Bus Number	Device Number	Function Number	Register Number	0	1

Figure 3−3. PCI AD31−AD0 During Address Phase of a Type 1 Configuration Cycle

Several bridge configuration registers shown in Table 4−1 are significant when decoding and claiming type 1 configuration cycles. The destination bus number encoded on the P_AD bus is compared to the values programmed in the bridge configuration registers 18h, 19h, and 1Ah, which are the primary bus number, secondary bus number, and subordinate bus number registers, respectively. These registers default to 00h and are programmed by host software to reflect the bus hierarchy in the system (see Figure 3−4 for an example of a system bus hierarchy and how the PCI2050B bus number registers would be programmed in this case).

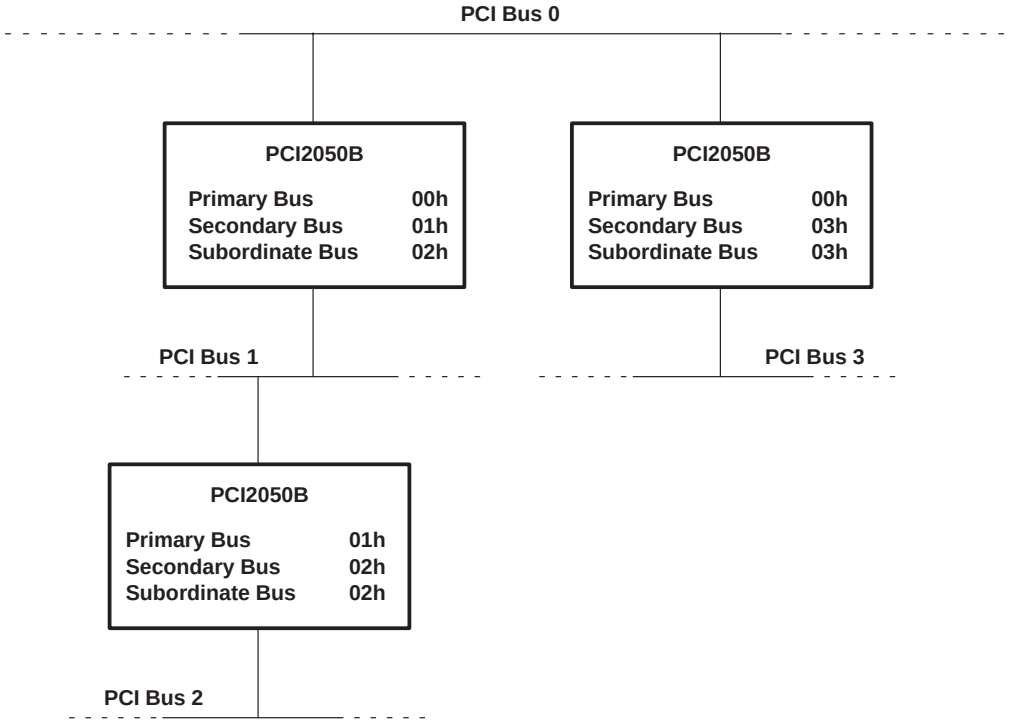


Figure 3−4. Bus Hierarchy and Numbering

When the PCI2050B bridge claims a type 1 configuration cycle that has a bus number equal to its secondary bus number, the PCI2050B bridge converts the type 1 configuration cycle to a type 0 configuration cycle and asserts the proper S_AD line as the IDSEL (see Table 3−2). All other type 1 transactions that access a bus number greater than the bridge secondary bus number but less than or equal to its subordinate bus number are forwarded as type 1 configuration cycles.

Table 3−2. PCI S_AD31−S_AD16 During the Address Phase of a Type 0 Configuration Cycle

DEVICE NUMBER	SECONDARY IDSEL S_AD31−S_AD16	S_AD ASSERTED
0h	0000 0000 0000 0001	16
1h	0000 0000 0000 0010	17
2h	0000 0000 0000 0100	18
3h	0000 0000 0000 1000	19
4h	0000 0000 0001 0000	20
5h	0000 0000 0010 0000	21
6h	0000 0000 0100 0000	22
7h	0000 0000 1000 0000	23
8h	0000 0001 0000 0000	24
9h	0000 0010 0000 0000	25
Ah	0000 0100 0000 0000	26
Bh	0000 1000 0000 0000	27
Ch	0001 0000 0000 0000	28
Dh	0010 0000 0000 0000	29
Eh	0100 0000 0000 0000	30
Fh	1000 0000 0000 0000	31
10h−1Eh	0000 0000 0000 0000	−

3.4 Special Cycle Generation

The bridge is designed to generate special cycles on both buses through a type 1 cycle conversion. During a type 1 configuration cycle, if the bus number field matches the bridge secondary bus number, the device number field is 1Fh, and the function number field is 07h, then the bridge generates a special cycle on the secondary bus with a message that matches the type 1 configuration cycle data. If the bus number is a subordinate bus and not the secondary, then the bridge passes the type 1 special cycle request through to the secondary interface along with the proper message.

Special cycles are never passed through the bridge. Type 1 configuration cycles with a special cycle request can propagate in both directions.

3.5 Secondary Clocks

The PCI2050B bridge provides 10 secondary clock outputs (S_CLKOUT[0:9]). Nine are provided for clocking secondary devices. The tenth clock must be routed back into the PCI2050B S_CLK input to ensure all secondary bus devices see the same clock. Figure 3−5 is a block diagram of the secondary clock function.

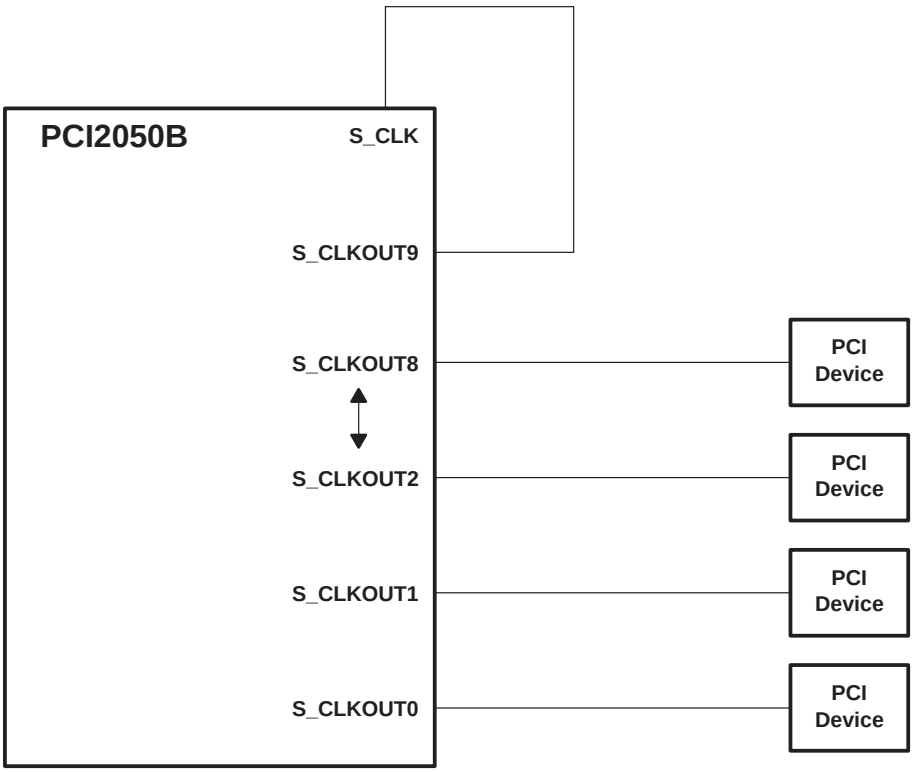


Figure 3−5. Secondary Clock Block Diagram

3.6 Bus Arbitration

The PCI2050B bridge implements bus request ($\overline{\text{P\_REQ}}$) and bus grant ($\overline{\text{P\_GNT}}$) terminals for primary PCI bus arbitration. Nine secondary bus requests and nine secondary bus grants are provided on the secondary of the PCI2050B bridge. Ten potential initiators, including the bridge, can be located on the secondary bus. The PCI2050B bridge provides a two-tier arbitration scheme on the secondary bus for priority bus-master handling.

The two-tier arbitration scheme improves performance in systems in which master devices do not all require the same bandwidth. Any master that requires frequent use of the bus can be programmed to be in the higher priority tier.

3.6.1 Primary Bus Arbitration

The PCI2050B bridge, acting as an initiator on the primary bus, asserts $\overline{\text{P\_REQ}}$ when forwarding transactions upstream to the primary bus. If a target disconnect, a target retry, or a target abort is received in response to a transaction initiated on the primary bus by the PCI2050B bridge, then the device deasserts $\overline{\text{P\_REQ}}$ for two PCI clock cycles.

When the primary bus arbiter asserts $\overline{\text{P\_GNT}}$ in response to a $\overline{\text{P\_REQ}}$ from the PCI2050B bridge, the device initiates a transaction on the primary bus during the next PCI clock cycle after the primary bus is sampled idle.

When $\overline{\text{P\_REQ}}$ is not asserted and the primary bus arbiter asserts $\overline{\text{P\_GNT}}$ to the PCI2050B bridge, the device responds by parking the P_AD31−P_AD0 bus, the C/$\overline{\text{BE3}}$−C/$\overline{\text{BE0}}$ bus, and primary parity (P_PAR) by driving them to valid logic levels. If the PCI2050B bridge is parking the primary bus and wants to initiate a transaction on the bus, then it can start the transaction on the next PCI clock by asserting the primary cycle frame ($\overline{\text{P\_FRAME}}$) while $\overline{\text{P\_GNT}}$ is still asserted. If $\overline{\text{P\_GNT}}$ is deasserted, then the bridge must rearbitrate for the bus to initiate a transaction.

3.6.2 Internal Secondary Bus Arbitration

$\overline{\text{S\_CFN}}$ controls the state of the secondary internal arbiter. The internal arbiter can be enabled by pulling $\overline{\text{S\_CFN}}$ low or disabled by pulling $\overline{\text{S\_CFN}}$ high. The PCI2050B bridge provides nine secondary bus request terminals and nine

secondary bus grant terminals. Including the bridge, there are a total of ten potential secondary bus masters. These request and grant signals are connected to the internal arbiter. When an external arbiter is implemented, S_REQ8−S_REQ1 and S_GNT8−S_GNT1 are placed in a high-impedance mode.

3.6.3 External Secondary Bus Arbitration

An external secondary bus arbiter can be used instead of the PCI2050B internal bus arbiter. When using an external arbiter, the PCI2050B internal arbiter must be disabled by pulling S_CFN high.

When an external secondary bus arbiter is used, the PCI2050B bridge internally reconfigures the S_REQ0 and S_GNT0 signals so that S_REQ0 becomes the secondary bus grant for the bridge and S_GNT0 becomes the secondary bus request for the bridge. This is done because S_REQ0 is an input and can thus provide the grant input to the bridge, and S_GNT0 is an output and can thus provide the request output from the bridge.

When an external arbiter is used, all unused secondary bus grant outputs (S_GNT8−S_GNT1) are placed in a high impedance mode. Any unused secondary bus request inputs (S_REQ8−S_REQ1) must be pulled high to prevent the inputs from oscillating.

3.7 Decode Options

The PCI2050B bridge supports positive decoding on the primary interface and negative decoding on the secondary interface. Positive decoding is a method of address decoding in which a device responds only to accesses within an assigned address range. Negative decoding is a method of address decoding in which a device responds only to accesses outside of an assigned address range.

3.8 System Error Handling

The PCI2050B bridge can be configured to signal a system error (SERR) for a variety of conditions. The P_SERR event disable register (offset 64h, see Section 5.4) and the P_SERR status register (offset 6Ah, see Section 5.9) provide control and status bits for each condition for which the bridge can signal SERR. These individual bits enable SERR reporting for both downstream and upstream transactions.

By default, the PCI2050B bridge will not signal SERR. If the PCI2050B bridge is configured to signal SERR by setting bit 8 in the command register (offset 04h, see Section 4.3), then the bridge signals SERR if any of the error conditions in the P_SERR event disable register occur and that condition is enabled. By default, all error conditions are enabled in the P_SERR event disable register. When the bridge signals SERR, bit 14 in the secondary status register (offset 1Eh, see Section 4.19) is set.

3.8.1 Posted Write Parity Error

If bit 1 in the P_SERR event disable register (offset 64h, see Section 5.4) is 0, then parity errors on the target bus during a posted write are passed to the initiating bus as a SERR. When this occurs, bit 1 of the P_SERR status register (offset 6Ah, see Section 5.9) is set. The status bit is cleared by writing a 1.

3.8.2 Posted Write Time-Out

If bit 2 in the P_SERR event disable register (offset 64h, see Section 5.4) is 0 and the retry timer expires while attempting to complete a posted write, then the PCI2050B bridge signals SERR on the initiating bus. When this occurs, bit 2 of the P_SERR status register (offset 6Ah, see Section 5.9) is set. The status bit is cleared by writing a 1.

3.8.3 Target Abort on Posted Writes

If bit 3 in the P_SERR event disable register (offset 64h, see Section 5.4) is 0 and the bridge receives a target abort during a posted write transaction, then the PCI2050B bridge signals SERR on the initiating bus. When this occurs, bit 3 of the P_SERR status register (offset 6Ah, see Section 5.9) is set. The status bit is cleared by writing a 1.

3.8.4 Master Abort on Posted Writes

If bit 4 in the P_SERR event disable register (PCI offset 64h, see Section 5.4) is 0 and a posted write transaction results in a master abort, then the PCI2050B bridge signals SERR on the initiating bus. When this occurs, bit 4 of the P_SERR status register (PCI offset 6Ah, see Section 5.9) is set. The status bit is cleared by writing a 1.

3.8.5 Master Delayed Write Time-Out

If bit 5 in the P_SERR event disable register (PCI offset 64h, see Section 5.4) is 0 and the retry timer expires while attempting to complete a delayed write, then the PCI2050B bridge signals SERR on the initiating bus. When this occurs, bit 5 of the P_SERR status register (PCI offset 6Ah, see Section 5.9) is set. The status bit is cleared by writing a 1.

3.8.6 Master Delayed Read Time-Out

If bit 6 in the P_SERR event disable register (offset 64h, see Section 5.4) is 0 and the retry timer expires while attempting to complete a delayed read, then the PCI2050B bridge signals SERR on the initiating bus. When this occurs, bit 6 of the P_SERR status register (offset 6Ah, see Section 5.9) is set. The status bit is cleared by writing a 1.

3.8.7 Secondary SERR

The PCI2050B bridge passes SERR from the secondary bus to the primary bus if it is enabled for SERR response, that is, if bit 8 in the command register (PCI offset 04h, see Section 4.3) is set, and if bit 1 in the bridge control register (PCI offset 3Eh, see Section 4.32) is set.

3.9 Parity Handling and Parity Error Reporting

When forwarding transactions, the PCI2050B bridge attempts to pass the data parity condition from one interface to the other unchanged, whenever possible, to allow the master and target devices to handle the error condition.

3.9.1 Address Parity Error

If the parity error response bit (bit 6) in the command register (PCI offset 04h, see Section 4.3) is set, then the PCI2050B bridge signals SERR on address parity errors and target abort transactions.

3.9.2 Data Parity Error

If the parity error response bit (bit 6) in the command register (PCI offset 04h, see Section 4.3) is set, then the PCI2050B bridge signals PERR when it receives bad data. When the bridge detects bad parity, bit 15 (detected parity error) in the status register (PCI offset 06h, see Section 4.4) is set.

If the bridge is configured to respond to parity errors via bit 6 in the command register (PCI offset 04h, see Section 4.3), then bit 8 (data parity error detected) in the status register (PCI offset 06h, see Section 4.4) is set when the bridge detects bad parity. The data parity error detected bit is also set when the bridge, as a bus master, asserts PERR or detects PERR.

3.10 Master and Target Abort Handling

If the PCI2050B bridge receives a target abort during a write burst, then it signals target abort back on the initiator bus. If it receives a target abort during a read burst, then it provides all of the valid data on the initiator bus and disconnects. Target aborts for posted and nonposted transactions are reported as specified in the *PCI-to-PCI Bridge Specification*.

Master aborts for posted and nonposted transactions are reported as specified in the *PCI-to-PCI Bridge Specification*. If a transaction is attempted on the primary bus after a secondary reset is asserted, then the PCI2050B bridge follows bit 5 (master abort mode) in the bridge control register (PCI offset 3Eh, see Section 4.32) for reporting errors.

3.11 Discard Timer

The PCI2050B bridge is free to discard the data or status of a delayed transaction that was completed with a delayed transaction termination when a bus master has not repeated the request within 2^{10} or 2^{15} PCI clocks (approximately 30 μs and 993 μs, respectively). The *PCI Local Bus Specification* recommends that a bridge wait 2^{15} PCI clocks before discarding the transaction data or status.

The PCI2050B bridge implements a discard timer for use in delayed transactions. After a delayed transaction is completed on the destination bus, the bridge may discard it under two conditions. The first condition occurs when a read transaction is made to a region of memory that is inside a defined prefetchable memory region, or when the command is a memory read line or a memory read multiple, implying that the memory region is prefetchable. The other condition occurs when the master originating the transaction (either a read or a write, prefetchable or nonprefetchable) has not retried the transaction within 2^{10} or 2^{15} clocks. The number of clocks is tracked by a timer referred to as the discard timer. When the discard timer expires, the bridge is required to discard the data. The PCI2050B default value for the discard timer is 2^{15} clocks; however, this value can be set to 2^{10} clocks by setting bit 9 in the bridge control register (offset 3Eh, see Section 4.32). For more information on the discard timer, see *error conditions* in the *PCI Local Bus Specification*.

3.12 Delayed Transactions

The bridge supports delayed transactions as defined in *PCI Local Bus Specification*. A target must be able to complete the initial data phase in 16 PCI clocks or less from the assertion of the cycle frame ($\overline{\text{FRAME}}$), and subsequent data phases must complete in eight PCI clocks or less. A delayed transaction consists of three phases:

- An initiator device issues a request.
- The target completes the request on the destination bus and signals the completion to the initiator.
- The initiator completes the request on the originating bus.

If the bridge is the target of a PCI transaction and it must access a slow device to write or read the requested data, and the transaction takes longer than 16 clocks, then the bridge must latch the address, the command, and the byte enables, and then issue a retry to the initiator. The initiator must end the transaction without any transfer of data and is required to retry the transaction later using the same address, command, and byte enables. This is the first phase of the delayed transaction.

During the second phase, if the transaction is a read cycle, the bridge fetches the requested data on the destination bus, stores it internally, and obtains the completion status, thus completing the transaction on the destination bus. If it is a write transaction, then the bridge writes the data and obtains the completion status, thus completing the transaction on the destination bus. The bridge stores the completion status until the master on the initiating bus retries the initial request.

During the third phase, the initiator rearbitrates for the bus. When the bridge sees the initiator retry the transaction, it compares the second request to the first request. If the address, command, and byte enables match the values latched in the first request, then the completion status (and data if the request was a read) is transferred to the initiator. At this point, the delayed transaction is complete. If the second request from the initiator does not match the first request exactly, then the bridge issues another retry to the initiator.

The PCI supports up to three delayed transactions in each direction at any given time.

3.13 Mode Selection

Table 3−3 shows the mode selection via MS0 (PDV/PPM terminal 155, GHK/ZHK terminal E17) and MS1 (PDV/PPM terminal 106, GHK/ZHK terminal T19).

Table 3−3. Configuration via MS0 and MS1

MS0	MS1	MODE
0	0	CompactPCI hot-swap friendly *PCI Bus Power Management Interface Specification* (Revision 1.1) $\overline{\text{HS\_SWITCH}}$/GPIO(3) functions as $\overline{\text{HS\_SWITCH}}$
0	1	CompactPCI hot-swap disabled *PCI Bus Power Management Interface Specification* (Revision 1.1) $\overline{\text{HS\_SWITCH}}$/GPIO(3) functions as GPIO(3)
1	X	Intel™ compatible No cPCI hot swap *PCI Bus Power Management Interface Specification* (Revision 1.0)

3.14 CompactPCI Hot-Swap Support

The PCI2050B bridge is hot-swap friendly silicon that supports all of the hot-swap capable features, contains support for software control, and integrates circuitry required by the *PICMG CompactPCI Hot-Swap Specification*. To be hot-swap capable, the PCI2050B bridge supports the following:

- Compliance with *PCI Local Bus Specification*
- Tolerance of V_{CC} from early power
- Asynchronous reset
- Tolerance of precharge voltage
- I/O buffers that meet modified V/I requirements
- Limited I/O terminal voltage at precharge voltage
- Hot-swap control and status programming via extended PCI capabilities linked list
- Hot-swap terminals: $\overline{\text{HS\_ENUM}}$, $\overline{\text{HS\_SWITCH}}$, and HS_LED

cPCI hot-swap defines a process for installing and removing PCI boards without adversely affecting a running system. The PCI2050B bridge provides this functionality such that it can be implemented on a board that can be removed and inserted in a hot-swap system.

The PCI2050B bridge provides three terminals to support hot-swap when configured to be in hot-swap mode: $\overline{\text{HS\_ENUM}}$ (output), $\overline{\text{HS\_SWITCH}}$ (input), and HS_LED (output). The $\overline{\text{HS\_ENUM}}$ output indicates to the system that an insertion event occurred or that a removal event is about to occur. The $\overline{\text{HS\_SWITCH}}$ input indicates the state of a board ejector handle, and the HS_LED output lights a blue LED to signal insertion- and removal-ready status.

3.15 JTAG Support

The PCI2050B bridge implements a JTAG test port based on IEEE Standard 1149.1, *IEEE Standard Test Access Port and Boundary-Scan Architecture*. The JTAG test port consists of the following:

- A 5-wire test access port
- A test access port controller
- An instruction register
- A bypass register
- A boundary-scan register

3.15.1 Test Port Instructions

The PCI2050B bridge supports the following JTAG instructions:

- EXTEST, BYPASS, and SAMPLE
- HIGHZ and CLAMP
- Private (various private instructions used by TI for test purposes)

Table 3−4 lists and describes the different test port instructions, and gives the op code of each one. The information in Table 3−5 is for implementation of boundary scan interface signals to permit in-circuit testing.

Table 3−4. JTAG Instructions and Op Codes

INSTRUCTION	OP CODE	DESCRIPTION
EXTEST	00000	External test: drives terminals from the boundary scan register
SAMPLE	00001	Sample I/O terminals
CLAMP	00100	Drives terminals from the boundary scan register and selects the bypass register for shifts
HIGHZ	00101	Puts all outputs and I/O terminals except for the TDO terminal in a high-impedance state
BYPASS	11111	Selects the bypass register for shifts

Table 3−5. Boundary Scan Terminal Order

BOUNDARY SCAN REGISTER NUMBER	PDV/PPM TERMINAL NUMBER	GHK/ZHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
0	137	J15	S_AD0	19	Bidirectional
1	138	H19	S_AD1	19	Bidirectional
2	140	H17	S_AD2	19	Bidirectional
3	141	H14	S_AD3	19	Bidirectional
4	143	G19	S_AD4	19	Bidirectional
5	144	G18	S_AD5	19	Bidirectional
6	146	G14	S_AD6	19	Bidirectional
7	147	F19	S_AD7	19	Bidirectional
8	149	G15	S_C/$\overline{\text{BE0}}$	19	Bidirectional
9	150	F17	S_AD8	19	Bidirectional
10	152	F14	S_AD9	19	Bidirectional
11	153	E18	S_M66ENA	19	Bidirectional
12	154	F15	S_AD10	19	Bidirectional
13	155	E17	MS0	−	Input
14	158	E14	S_AD11	19	Bidirectional
15	161	B15	S_AD12	19	Bidirectional
16	162	A15	S_AD13	19	Bidirectional
17	164	B14	S_AD14	19	Bidirectional
18	165	E13	S_AD15	19	Bidirectional
19	−	−	−	−	Control

Table 3−5. Boundary Scan Terminal Order (Continued)

BOUNDARY SCAN REGISTER NUMBER	PDV/PPM TERMINAL NUMBER	GHK/ZHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
20	167	F12	S_C/$\overline{\text{BE1}}$	19	Bidirectional
21	168	C13	S_PAR	19	Bidirectional
22	169	B13	$\overline{\text{S\_SERR}}$	−	Input
23	171	E12	$\overline{\text{S\_PERR}}$	26	Bidirectional
24	172	C12	$\overline{\text{S\_LOCK}}$	26	Bidirectional
25	173	B12	$\overline{\text{S\_STOP}}$	26	Bidirectional
26	−	−	−	−	Control
27	175	A11	$\overline{\text{S\_DEVSEL}}$	26	Bidirectional
28	176	B11	$\overline{\text{S\_TRDY}}$	26	Bidirectional
29	177	C11	$\overline{\text{S\_IRDY}}$	26	Bidirectional
30	179	F11	$\overline{\text{S\_FRAME}}$	26	Bidirectional
31	180	A10	S_C/$\overline{\text{BE2}}$	48	Bidirectional
32	182	E10	S_AD16	48	Bidirectional
33	183	F10	S_AD17	48	Bidirectional
34	185	C9	S_AD18	48	Bidirectional
35	186	F9	S_AD19	48	Bidirectional
36	188	A8	S_AD20	48	Bidirectional
37	189	B8	S_AD21	48	Bidirectional
38	191	F8	S_AD22	48	Bidirectional
39	192	E8	S_AD23	48	Bidirectional
40	194	B7	S_C/$\overline{\text{BE3}}$	48	Bidirectional
41	195	C7	S_AD24	48	Bidirectional
42	197	A6	S_AD25	48	Bidirectional
43	198	B6	S_AD26	48	Bidirectional
44	200	C6	S_AD27	48	Bidirectional
45	201	A5	S_AD28	48	Bidirectional
46	203	B5	S_AD29	48	Bidirectional
47	204	E6	S_AD30	48	Bidirectional
48	−	−	−	−	Control
49	206	A4	S_AD31	48	Bidirectional
50	207	B4	$\overline{\text{S\_REQ0}}$	−	Input
51	2	E3	$\overline{\text{S\_REQ1}}$	−	Input
52	3	F5	$\overline{\text{S\_REQ2}}$	−	Input
53	4	G6	$\overline{\text{S\_REQ3}}$	−	Input
54	5	E2	$\overline{\text{S\_REQ4}}$	−	Input
55	6	E1	$\overline{\text{S\_REQ5}}$	−	Input
56	7	F3	$\overline{\text{S\_REQ6}}$	−	Input
57	8	F2	$\overline{\text{S\_REQ7}}$	−	Input
58	9	G5	$\overline{\text{S\_REQ8}}$	−	Input
59	10	F1	$\overline{\text{S\_GNT0}}$	61	Output
60	11	H6	$\overline{\text{S\_GNT1}}$	61	Output
61	−	−	−	−	Control

Table 3−5. Boundary Scan Terminal Order (Continued)

BOUNDARY SCAN REGISTER NUMBER	PDV/PPM TERMINAL NUMBER	GHK/ZHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
62	13	G2	$\overline{\text{S\_GNT2}}$	61	Output
63	14	G1	$\overline{\text{S\_GNT3}}$	61	Output
64	15	H5	$\overline{\text{S\_GNT4}}$	61	Output
65	16	H3	$\overline{\text{S\_GNT5}}$	61	Output
66	17	H2	$\overline{\text{S\_GNT6}}$	61	Output
67	18	H1	$\overline{\text{S\_GNT7}}$	61	Output
68	19	J1	$\overline{\text{S\_GNT8}}$	61	Output
69	21	J3	S_CLK	−	Input
70	22	J5	$\overline{\text{S\_RST}}$	78	Output
71	23	J6	$\overline{\text{S\_CFN}}$	−	Input
72	24	K1	GPIO3	78	Bidirectional
73	25	K2	GPIO2	78	Bidirectional
74	27	K5	GPIO1	78	Bidirectional
75	28	K6	GPIO0	78	Bidirectional
76	29	L1	S_CLKOUT0	−	Output
77	30	L2	S_CLKOUT1	−	Output
78	−	−	−	−	Output
79	32	L5	S_CLKOUT2	−	Output
80	33	M1	S_CLKOUT3	−	Output
81	35	M3	S_CLKOUT4	−	Output
82	36	M6	S_CLKOUT5	−	Output
83	38	N1	S_CLKOUT6	−	Output
84	39	N2	S_CLKOUT7	−	Output
85	41	N6	S_CLKOUT8	−	Output
86	42	P1	S_CLKOUT9	−	Output
87	43	P2	$\overline{\text{P\_RST}}$	−	Input
88	44	N5	BPCCE	−	Input
89	45	P3	P_CLK	−	Input
90	46	R1	$\overline{\text{P\_GNT}}$	−	Input
91	47	P6	$\overline{\text{P\_REQ}}$	92	Output
92	−	−	−	−	Control
93	49	R3	P_AD31	111	Bidirectional
94	50	T1	P_AD30	111	Bidirectional
95	55	R6	P_AD29	111	Bidirectional
96	57	W5	P_AD28	111	Bidirectional
97	58	U6	P_AD27	111	Bidirectional
98	60	R7	P_AD26	111	Bidirectional
99	61	W6	P_AD25	111	Bidirectional
100	63	U7	P_AD24	111	Bidirectional
101	64	V7	P_C/$\overline{\text{BE3}}$	111	Bidirectional
102	65	W7	P_IDSEL	−	Input
103	67	U8	P_AD23	111	Bidirectional
104	68	V8	P_AD22	111	Bidirectional

Table 3−5. Boundary Scan Terminal Order (Continued)

BOUNDARY SCAN REGISTER NUMBER	PDV/PPM TERMINAL NUMBER	GHK/ZHK TERMINAL NUMBER	TERMINAL NAME	GROUP DISABLE REGISTER	BOUNDARY-SCAN CELL TYPE
105	70	W9	P_AD21	111	Bidirectional
106	71	V9	P_AD20	111	Bidirectional
107	73	R9	P_AD19	111	Bidirectional
108	74	P9	P_AD18	111	Bidirectional
109	76	V10	P_AD17	111	Bidirectional
110	77	U10	P_AD16	111	Bidirectional
111	–	–	–	–	Control
112	79	P10	P_C/$\overline{\text{BE2}}$	111	Bidirectional
113	80	W11	$\overline{\text{P\_FRAME}}$	118	Bidirectional
114	82	U11	$\overline{\text{P\_IRDY}}$	118	Bidirectional
115	83	P11	$\overline{\text{P\_TRDY}}$	118	Bidirectional
116	84	R11	$\overline{\text{P\_DEVSEL}}$	118	Bidirectional
117	85	W12	$\overline{\text{P\_STOP}}$	118	Bidirectional
118	–	–	–	–	Control
119	87	P12	$\overline{\text{P\_LOCK}}$	118	Input
120	88	R12	$\overline{\text{P\_PERR}}$	118	Bidirectional
121	89	W13	$\overline{\text{P\_SERR}}$	142	Output
122	90	V13	P_PAR	142	Bidirectional
123	92	P13	P_C/$\overline{\text{BE1}}$	142	Bidirectional
124	93	W14	P_AD15	142	Bidirectional
125	95	R13	P_AD14	142	Bidirectional
126	96	U14	P_AD13	142	Bidirectional
127	98	P14	P_AD12	142	Bidirectional
128	99	V15	P_AD11	142	Bidirectional
129	101	U15	P_AD10	142	Bidirectional
130	106	T19	MS1	–	Input
131	107	R17	P_AD9	142	Bidirectional
132	109	N14	P_AD8	142	Bidirectional
133	110	R18	P_C/$\overline{\text{BE0}}$	142	Bidirectional
134	112	P17	P_AD7	142	Bidirectional
135	113	P18	P_AD6	142	Bidirectional
136	115	P19	P_AD5	142	Bidirectional
137	116	M14	P_AD4	142	Bidirectional
138	118	N18	P_AD3	142	Bidirectional
139	119	N19	P_AD2	142	Bidirectional
140	121	M17	P_AD1	142	Bidirectional
141	122	M18	P_AD0	142	Bidirectional
142	–	–	–	–	–
143	126	L17	MSK_IN	–	Input
144	–	–	–	–	Control
145	127	L15	$\overline{\text{HS\_ENUM}}$	144	Output
146	128	L14	HS_LED	144	Output

3.16 GPIO Interface

The PCI2050B bridge implements a four-terminal general-purpose I/O interface. Besides functioning as a general-purpose I/O interface, the GPIO terminals can read in the secondary clock mask and stop the bridge from accepting I/O and memory transactions.

3.16.1 Secondary Clock Mask

The PCI2050B bridge uses GPIO0, GPIO2, and MSK_IN to shift in the secondary clock mask from an external shift register. A secondary clock mask timing diagram is shown in Figure 3−6. Table 3−6 lists the format for clock mask data.

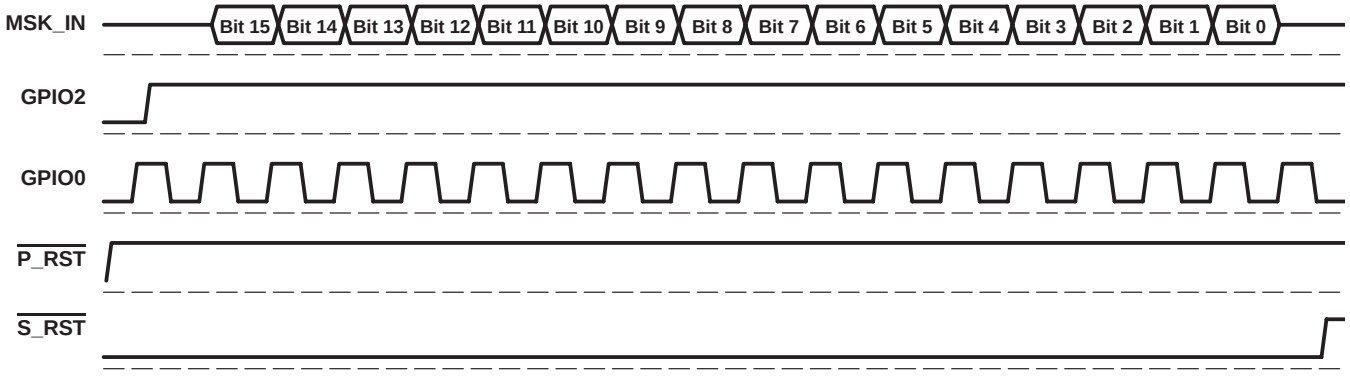


Figure 3−6. Clock Mask Read Timing After Reset

Table 3−6. Clock Mask Data Format

BIT	CLOCK
[0:1]	S_CLKOUT0
[2:3]	S_CLKOUT1
[4:5]	S_CLKOUT2
[6:7]	S_CLKOUT3
8	S_CLKOUT4
9	S_CLKOUT5
10	S_CLKOUT6
11	S_CLKOUT7
12	S_CLKOUT8
13	S_CLKOUT9 (PCI2050B S_CLK input)
[14:15]	Reserved

3.16.2 Transaction Forwarding Control

The PCI2050B bridge will stop forwarding I/O and memory transactions if bit 5 of the chip control register (offset 40h, see Section 5.1) is set to 1 and GPIO3 is driven high. The bridge completes all queued posted writes and delayed requests, but delayed completions are not returned until GPIO3 is driven low and transaction forwarding is resumed. The bridge continues to accept configuration cycles in this mode. This feature is not available when in CompactPCI hot-swap mode because GPIO3 is used as the $\overline{\text{HS\_SWITCH}}$ input in this mode.

3.17 PCI Power Management

The *PCI Power Management Specification* establishes the infrastructure required to let the operating system control the power of PCI functions. This is done by defining a standard PCI interface and operations to manage the power of PCI functions on the bus. The PCI bus and the PCI functions can be assigned one of four software visible power management states, which result in varying levels of power savings.

The four power management states of PCI functions are D0—fully on state, D1 and D2—intermediate states, and D3—off state. Similarly, bus power states of the PCI bus are B0−B3. The bus power states B0−B3 are derived from the device power state of the originating PCI2050B device.

For the operating system to manage the device power states on the PCI bus, the PCI function supports four power management operations:

- Capabilities reporting
- Power status reporting
- Setting the power state
- System wake-up

The operating system identifies the capabilities of the PCI function by traversing the new capabilities list. The presence of the new capabilities list is indicated by bit 4 in the status register (offset 06h, see Section 4.4) which provides access to the capabilities list.

3.17.1 Behavior in Low-Power States

The PCI2050B bridge supports D0, D1, D2, and $D3_{hot}$ power states when in TI mode. The PCI2050B bridge only supports D0 and D3 power states when in Intel mode. The PCI2050B bridge is fully functional only in D0 state. In the lower power states, the bridge does not accept any memory or I/O transactions. These transactions are aborted by the master. The bridge accepts type 0 configuration cycles in all power states except $D3_{cold}$. The bridge also accepts type 1 configuration cycles but does not pass these cycles to the secondary bus in any of the lower power states. Type 1 configuration writes are discarded and reads return all 1s. All error reporting is done in the low power states. When in D2 and $D3_{hot}$ states, the bridge turns off all secondary clocks for further power savings.

When going from $D3_{hot}$ to D0, an internal reset is generated. This reset initializes all PCI configuration registers to their default values. The TI specific registers (40h − FFh) are not reset. Power management registers also are not reset.

4 Bridge Configuration Header

The PCI2050B bridge is a single-function PCI device. The configuration header is in compliance with the *PCI-to-PCI Bridge Specification* (Revision 1.1). Table 4−1 shows the PCI configuration header, which includes the predefined portion of the bridge configuration space. The PCI configuration offset is shown in the right column under the OFFSET heading.

Table 4−1. Bridge Configuration Header

REGISTER NAME				OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class code			Revision ID	08h
BIST	Header type	Primary latency timer	Cache line size	0Ch
Base address 0				10h
Base address 1				14h
Secondary bus latency timer	Subordinate bus number	Secondary bus number	Primary bus number	18h
Secondary status		I/O limit	I/O base	1Ch
Memory limit		Memory base		20h
Prefetchable memory limit		Prefetchable memory base		24h
Prefetchable base upper 32 bits				28h
Prefetchable limit upper 32 bits				2Ch
I/O limit upper 16 bits		I/O base upper 16 bits		30h
Reserved			Capability pointer	34h
Expansion ROM base address				38h
Bridge control		Interrupt pin	Interrupt line	3Ch
Arbiter control		Extended diagnostic	Chip control	40h
Reserved				44h−60h
GPIO input data	GPIO output enable	GPIO output data	P_SERR event disable	64h
Reserved	P_SERR status	Secondary clock control		68h
Reserved				6Ch−D8h
Power management capabilities		PM next item pointer	PM capability ID	DCh
Data	PMCSR bridge support	Power management control/status		E0h
Reserved	Hot swap control status	HS next item pointer	HS capability ID	E4h
Reserved				E8h−ECh
Reserved			Diagnostics	F0h
Reserved				F4h−FFh

4.1 Vendor ID Register

This 16-bit value is allocated by the PCI Special Interest Group (SIG) and identifies TI as the manufacturer of this device. The vendor ID assigned to TI is 104Ch.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Vendor ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

Register: **Vendor ID**
Type: Read-only
Offset: 00h
Default: 104Ch

4.2 Device ID Register

This 16-bit value is allocated by the vendor and identifies the PCI device. The device ID for the PCI2050B bridge is AC28h.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Device ID															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	1	0	1	0	1	1	0	0	0	0	1	0	1	0	0	0

Register: **Device ID**
Type: Read-only
Offset: 02h
Default: AC28h

4.3 Command Register

The command register provides control over the bridge interface to the primary PCI bus. VGA palette snooping is enabled through this register, and all other bits adhere to the definitions in the *PCI Local Bus Specification*. Table 4−2 describes the bit functions in the command register.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Command															
Type	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Command**
Type: Read-only, Read/Write
Offset: 04h
Default: 0000h

Table 4−2. Command Register Description

BIT	TYPE	FUNCTION
15−10	R	Reserved
9	R/W	Fast back-to-back enable. This bit defaults to 0.
8	R/W	System error ($\overline{\text{SERR}}$) enable. Bit 8 controls the enable for the $\overline{\text{SERR}}$ driver on the primary interface. 0 = Disable $\overline{\text{SERR}}$ driver on primary interface (default) 1 = Enable the $\overline{\text{SERR}}$ driver on primary interface
7	R	Wait cycle control. Bit 7 controls address/data stepping by the bridge on both interfaces. The bridge does not support address/data stepping and this bit is hardwired to 0.
6	R/W	Parity error response enable. Bit 6 controls the bridge response to parity errors. 0 = Parity error response disabled (default) 1 = Parity error response enabled
5	R/W	VGA palette snoop enable. When set, the bridge passes I/O writes on the primary PCI bus with addresses 3C6h, 3C8h, and 3C9h inclusive of ISA aliases (that is, only bits AD9−AD0 are included in the decode).
4	R	Memory write and invalidate enable. In a PCI-to-PCI bridge, bit 4 must be read-only and return 0 when read.
3	R	Special cycle enable. A PCI-to-PCI bridge cannot respond as a target to special cycle transactions, so bit 3 is defined as read-only and must return 0 when read.
2	R/W	Bus master enable. Bit 2 controls the ability of the bridge to initiate a cycle on the primary PCI bus. When bit 2 is 0, the bridge does not respond to any memory or I/O transactions on the secondary interface since they cannot be forwarded to the primary PCI bus. 0 = Bus master capability disabled (default) 1 = Bus master capability enabled
1	R/W	Memory space enable. Bit 1 controls the bridge response to memory accesses for both prefetchable and nonprefetchable memory spaces on the primary PCI bus. Only when bit 1 is set will the bridge forward memory accesses to the secondary bus from a primary bus initiator. 0 = Memory space disabled (default) 1 = Memory space enabled
0	R/W	I/O space enable. Bit 0 controls the bridge response to I/O accesses on the primary interface. Only when bit 0 is set will the bridge forward I/O accesses to the secondary bus from a primary bus initiator. 0 = I/O space disabled (default) 1 = I/O space enabled

4.4 Status Register

The status register provides device information to the host system. Bits in this register are cleared by writing a 1 to the respective bit; writing a 0 to a bit location has no effect. Table 4−3 describes the status register.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Status															
Type	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0

Register: **Status**
Type: Read-only, Read/Write
Offset: 06h
Default: 0290h

Table 4−3. Status Register Description

BIT	TYPE	FUNCTION
15	R/W	Detected parity error. Bit 15 is set when a parity error is detected.
14	R/W	Signaled system error ($\overline{\text{SERR}}$). Bit 14 is set if $\overline{\text{SERR}}$ is enabled in the command register (offset 04h, see Section 4.3) and the bridge signals a system error (SERR). See Section 3.8, *System Error Handling*. 0 = No SERR signaled (default) 1 = Signals SERR
13	R/W	Received master abort. Bit 13 is set when a cycle initiated by the bridge on the primary bus has been terminated by a master abort. 0 = No master abort received (default) 1 = Master abort received
12	R/W	Received target abort. Bit 12 is set when a cycle initiated by the bridge on the primary bus has been terminated by a target abort. 0 = No target abort received (default) 1 = Target abort received
11	R/W	Signaled target abort. Bit 11 is set by the bridge when it terminates a transaction on the primary bus with a target abort. 0 = No target abort signaled by the bridge (default) 1 = Target abort signaled by the bridge
10−9	R	DEVSEL timing. These read-only bits encode the timing of $\overline{\text{P\_DEVSEL}}$ and are hardwired 01b, indicating that the bridge asserts this signal at a medium speed.
8	R/W	Data parity error detected. Bit 8 is encoded as: 0 = The conditions for setting this bit have not been met. No parity error detected. (default) 1 = A data parity error occurred and the following conditions were met: a. $\overline{\text{P\_PERR}}$ was asserted by any PCI device including the bridge. b. The bridge was the bus master during the data parity error. c. The parity error response bit (bit 6) was set in the command register (offset 04h, see Section 4.3).
7	R	Fast back-to-back capable. The bridge supports fast back-to-back transactions as a target; therefore, bit 7 is hardwired to 1.
6	R	User-definable feature (UDF) support. The PCI2050B bridge does not support the user-definable features; therefore, bit 6 is hardwired to 0.
5	R	66-MHz capable. Bit 5 indicates whether the primary interface is 66-MHz capable. It reads as 0 when CONFIG66 is tied low to indicate that the PCI2050B bridge is not 66 MHz capable and reads as 1 when CONFIG66 is tied high to indicate that the primary bus is 66 MHz capable.
4	R	Capabilities list. Bit 4 is read-only and is hardwired to 1, indicating that capabilities additional to standard PCI are implemented. The linked list of PCI power management capabilities is implemented by this function.
3−0	R	Reserved. Bits 3−0 return 0s when read.

4.5 Revision ID Register

The revision ID register indicates the silicon revision of the PCI2050B bridge.

Bit	7	6	5	4	3	2	1	0
Name	Revision ID							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	1	0

Register: **Revision ID**
Type: Read-only
Offset: 08h
Default: 02h (reflects the current revision of the silicon)

4.6 Class Code Register

This register categorizes the PCI2050B bridge as a PCI-to-PCI bridge device (0604h) with a 00h programming interface.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Class code																							
	Base class								Sub class								Programming interface							
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Register: **Class code**
Type: Read-only
Offset: 09h
Default: 06 0400h

4.7 Cache Line Size Register

The cache line size register is programmed by host software to indicate the system cache line size needed by the bridge for memory read line, memory read multiple, and memory write and invalidate transactions. The PCI2050B bridge supports cache line sizes up to and including 16 doublewords for memory write and invalidate. If the cache line size is larger than 16 doublewords, the command is converted to a memory write command.

Bit	7	6	5	4	3	2	1	0
Name	Cache line size							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **Cache line size**
Type: Read/Write
Offset: 0Ch
Default: 00h

4.8 Primary Latency Timer Register

The latency timer register specifies the latency timer for the bridge in units of PCI clock cycles. When the bridge is a primary PCI bus initiator and asserts $\overline{\text{P\_FRAME}}$, the latency timer begins counting from 0. If the latency timer expires before the bridge transaction has terminated, then the bridge terminates the transaction when its $\overline{\text{P\_GNT}}$ is deasserted.

Bit	7	6	5	4	3	2	1	0
Name	Latency timer							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **Latency timer**
Type: Read/Write
Offset: 0Dh
Default: 00h

4.9 Header Type Register

The header type register is read-only and returns 01h when read, indicating that the PCI2050B configuration space adheres to the PCI-to-PCI bridge configuration. Only the layout for bytes 10h−3Fh of configuration space is considered.

Bit	7	6	5	4	3	2	1	0
Name	Header type							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

Register: **Header type**
Type: Read-only
Offset: 0Eh
Default: 01h

4.10 BIST Register

The PCI2050B bridge does not support built-in self test (BIST). The BIST register is read-only and returns the value 00h when read.

Bit	7	6	5	4	3	2	1	0
Name	BIST							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Register: **BIST**
Type: Read-only
Offset: 0Fh
Default: 00h

4.11 Base Address Register 0

The bridge requires no additional resources. Base address register 0 is read-only and returns 0s when read.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Base address register 0															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Base address register 0															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Base address register 0**
Type: Read-only
Offset: 10h
Default: 0000 0000h

4.12 Base Address Register 1

The bridge requires no additional resources. Base address register 1 is read-only and returns 0s when read.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Base address register 1															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Base address register 1															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Base address register 1**
Type: Read-only
Offset: 14h
Default: 0000 0000h

4.13 Primary Bus Number Register

The primary bus number register indicates the primary bus number to which the bridge is connected. The bridge uses this register, in conjunction with the secondary bus number and subordinate bus number registers, to determine when to forward PCI configuration cycles to the secondary buses.

Bit	7	6	5	4	3	2	1	0
Name	Primary bus number							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **Primary bus number**
Type: Read/Write
Offset: 18h
Default: 00h

4.14 Secondary Bus Number Register

The secondary bus number register indicates the secondary bus number to which the bridge is connected. The PCI2050B bridge uses this register, in conjunction with the primary bus number and subordinate bus number registers, to determine when to forward PCI configuration cycles to the secondary buses. Configuration cycles directed to the secondary bus are converted to type 0 configuration cycles.

Bit	7	6	5	4	3	2	1	0
Name	Secondary bus number							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **Secondary bus number**
Type: Read/Write
Offset: 19h
Default: 00h

4.15 Subordinate Bus Number Register

The subordinate bus number register indicates the bus number of the highest numbered bus beyond the primary bus existing behind the bridge. The PCI2050B bridge uses this register, in conjunction with the primary bus number and secondary bus number registers, to determine when to forward PCI configuration cycles to the subordinate buses. Configuration cycles directed to a subordinate bus (not the secondary bus) remain type 1 cycles as the cycle crosses the bridge.

Bit	7	6	5	4	3	2	1	0
Name	Subordinate bus number							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **Subordinate bus number**
Type: Read/write
Offset: 1Ah
Default: 00h

4.16 Secondary Bus Latency Timer Register

The secondary bus latency timer specifies the latency time for the bridge in units of PCI clock cycles. When the bridge is a secondary PCI bus initiator and asserts $\overline{\text{S\_FRAME}}$, the latency timer begins counting from 0. If the latency timer expires before the bridge transaction has terminated, then the bridge terminates the transaction when its $\overline{\text{S\_GNT}}$ is deasserted. The PCI-to-PCI bridge $\overline{\text{S\_GNT}}$ is an internal signal and is removed when another secondary bus master arbitrates for the bus.

Bit	7	6	5	4	3	2	1	0
Name	Secondary bus latency timer							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **Secondary bus latency timer**
Type: Read/Write
Offset: 1Bh
Default: 00h

4.17 I/O Base Register

The I/O base register is used in decoding I/O addresses to pass through the bridge. The bridge supports 32-bit I/O addressing; thus, bits 3−0 are read-only and default to 0001b. The upper four bits are writable and correspond to address bits AD15−AD12. The lower 12 address bits of the I/O base address are considered 0. Thus, the bottom of the defined I/O address range is aligned on a 4K-byte boundary. The upper 16 address bits of the 32-bit I/O base address corresponds to the contents of the I/O base upper 16 bits register (offset 30h, see Section 4.26).

Bit	7	6	5	4	3	2	1	0
Name	I/O base							
Type	R/W	R/W	R/W	R/W	R	R	R	R
Default	0	0	0	0	0	0	0	1

Register: **I/O base**
Type: Read-only, Read/Write
Offset: 1Ch
Default: 01h

4.18 I/O Limit Register

The I/O limit register is used in decoding I/O addresses to pass through the bridge. The bridge supports 32-bit I/O addressing; thus, bits 3−0 are read-only and default to 0001b. The upper four bits are writable and correspond to address bits AD15−AD12. The lower 12 address bits of the I/O limit address are considered FFFh. Thus, the top of the defined I/O address range is aligned on a 4K-byte boundary. The upper 16 address bits of the 32-bit I/O limit address corresponds to the contents of the I/O limit upper 16 bits register (offset 32h, see Section 4.27).

Bit	7	6	5	4	3	2	1	0
Name	I/O limit							
Type	R/W	R/W	R/W	R/W	R	R	R	R
Default	0	0	0	0	0	0	0	1

Register: **I/O limit**
Type: Read-only, Read/Write
Offset: 1Dh
Default: 01h

4.19 Secondary Status Register

The secondary status register is similar in function to the status register (offset 06h, see Section 4.4); however, its bits reflect status conditions of the secondary interface. Bits in this register are cleared by writing a 1 to the respective bit.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Secondary status															
Type	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0

Register: **Secondary status**
Type: Read-only, Read/Write
Offset: 1Eh
Default: 0280h

Table 4−4. Secondary Status Register Description

BIT	TYPE	FUNCTION
15	R/W	Detected parity error. Bit 15 is set when a parity error is detected on the secondary interface. 0 = No parity error detected on the secondary bus (default) 1 = Parity error detected on the secondary bus
14	R/W	Received system error. Bit 14 is set when the secondary interface detects $\overline{\text{S\_SERR}}$ asserted. Note that the bridge never asserts $\overline{\text{S\_SERR}}$. 0 = No $\overline{\text{S\_SERR}}$ detected on the secondary bus (default) 1 = $\overline{\text{S\_SERR}}$ detected on the secondary bus
13	R/W	Received master abort. Bit 13 is set when a cycle initiated by the bridge on the secondary bus has been terminated by a master abort. 0 = No master abort received (default) 1 = Bridge master aborted the cycle
12	R/W	Received target abort. Bit 12 is set when a cycle initiated by the bridge on the secondary bus has been terminated by a target abort. 0 = No target abort received (default) 1 = Bridge received a target abort
11	R/W	Signaled target abort. Bit 11 is set by the bridge when it terminates a transaction on the secondary bus with a target abort. 0 = No target abort signaled (default) 1 = Bridge signaled a target abort
10−9	R	DEVSEL timing. These read-only bits encode the timing of $\overline{\text{S\_DEVSEL}}$ and are hardwired to 01b, indicating that the bridge asserts this signal at a medium speed.
8	R/W	Data parity error detected. 0 = The conditions for setting this bit have not been met 1 = A data parity error occurred and the following conditions were met: a. $\overline{\text{S\_PERR}}$ was asserted by any PCI device including the bridge. b. The bridge was the bus master during the data parity error. c. The parity error response bit (bit 1) was set in the bridge control register (offset 3Eh, see Section 4.32).
7	R	Fast back-to-back capable. Bit 7 is hardwired to 1.
6	R	User-definable feature (UDF) support. Bit 6 is hardwired to 0.
5	R	66-MHz capable. Bit 5 is hardwired to 0.
4−0	R	Reserved. Bits 4−0 return 0s when read.

4.20 Memory Base Register

The memory base register defines the base address of a memory-mapped I/O address range used by the bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits of this register are read/write and correspond to the address bits AD31−AD20. The lower 20 address bits are considered 0s; thus, the address range is aligned to a 1M-byte boundary. The bottom four bits are read-only and return 0s when read.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Memory base															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Memory base**
Type: Read-only, Read/Write
Offset: 20h
Default: 0000h

4.21 Memory Limit Register

The memory limit register defines the upper-limit address of a memory-mapped I/O address range used to determine when to forward memory transactions from one interface to the other. The upper 12 bits of this register are read/write and correspond to the address bits AD31−AD20. The lower 20 address bits are considered 1s; thus, the address range is aligned to a 1M-byte boundary. The bottom four bits are read-only and return 0s when read.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Memory limit															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Memory limit**
Type: Read-only, Read/Write
Offset: 22h
Default: 0000h

4.22 Prefetchable Memory Base Register

The prefetchable memory base register defines the base address of a prefetchable memory address range used by the bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits of this register are read/write and correspond to the address bits AD31−AD20. The lower 20 address bits are considered 0; thus, the address range is aligned to a 1M-byte boundary. The bottom four bits are read-only and return 0s when read.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Prefetchable memory base															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Prefetchable memory base**
Type: Read-only, Read/Write
Offset: 24h
Default: 0000h

4.23 Prefetchable Memory Limit Register

The prefetchable memory limit register defines the upper-limit address of a prefetchable memory address range used to determine when to forward memory transactions from one interface to the other. The upper 12 bits of this register are read/write and correspond to the address bits AD31−AD20. The lower 20 address bits are considered 1s; thus, the address range is aligned to a 1M-byte boundary. The bottom four bits are read-only and return 0s when read.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Prefetchable memory limit															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Prefetchable memory limit**
Type: Read-only, Read/Write
Offset: 26h
Default: 0000h

4.24 Prefetchable Base Upper 32 Bits Register

The prefetchable base upper 32 bits register plus the prefetchable memory base register defines the base address of the 64-bit prefetchable memory address range used by the bridge to determine when to forward memory transactions from one interface to the other. The prefetchable base upper 32 bits register must be programmed to all zeros when 32-bit addressing is being used.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Prefetchable base upper 32 bits															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	Prefetchable base upper 32 bits															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Prefetchable base upper 32 bits**
Type: Read/Write
Offset: 28h
Default: 0000 0000h

4.25 Prefetchable Limit Upper 32 Bits Register

The prefetchable limit upper 32 bits register plus the prefetchable memory limit register defines the base address of the 64-bit prefetchable memory address range used by the bridge to determine when to forward memory transactions from one interface to the other. The prefetchable limit upper 32 bits register must be programmed to all zeros when 32-bit addressing is being used.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Prefetchable limit upper 32 bits															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Prefetchable limit upper 32 bits															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Prefetchable limit upper 32 bits**
Type: Read/Write
Offset: 2Ch
Default: 0000 0000h

4.26 I/O Base Upper 16 Bits Register

The I/O base upper 16 bits register specifies the upper 16 bits corresponding to AD31−AD16 of the 32-bit address that specifies the base of the I/O range to forward from the primary PCI bus to the secondary PCI bus.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I/O base upper 16 bits															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **I/O base upper 16 bits**
Type: Read/Write
Offset: 30h
Default: 0000h

4.27 I/O Limit Upper 16 Bits Register

The I/O limit upper 16 bits register specifies the upper 16 bits corresponding to AD31−AD16 of the 32-bit address that specifies the upper limit of the I/O range to forward from the primary PCI bus to the secondary PCI bus.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I/O limit upper 16 bits															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **I/O limit upper 16 bits**
Type: Read/Write
Offset: 32h
Default: 0000h

4.28 Capability Pointer Register

The capability pointer register provides the pointer to the PCI configuration header where the PCI power management register block resides. The capability pointer provides access to the first item in the linked list of capabilities. The capability pointer register is read-only and returns DCh when read, indicating the power management registers are located at PCI header offset DCh.

Bit	7	6	5	4	3	2	1	0
Name	Capability pointer register							
Type	R	R	R	R	R	R	R	R
Default	1	1	0	1	1	1	0	0

Register: **Capability pointer**
Type: Read-only
Offset: 34h
Default: DCh

4.29 Expansion ROM Base Address Register

The PCI2050B bridge does not implement the expansion ROM remapping feature. The expansion ROM base address register returns all 0s when read.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Expansion ROM base address															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Expansion ROM base address															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Expansion ROM base address**
Type: Read-only
Offset: 38h
Default: 0000 0000h

4.30 Interrupt Line Register

The interrupt line register is read/write and is used to communicate interrupt line routing information. Since the bridge does not implement an interrupt signal terminal, this register defaults to 00h.

Bit	7	6	5	4	3	2	1	0
Name	Interrupt line							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **Interrupt line**
Type: Read/Write
Offset: 3Ch
Default: 00h

4.31 Interrupt Pin Register

The bridge default state does not implement any interrupt terminals. Reads from bits 7−0 of this register return 0s.

Bit	7	6	5	4	3	2	1	0
Name	Interrupt pin							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Register: **Interrupt pin**
Type: Read-only
Offset: 3Dh
Default: 00h

4.32 Bridge Control Register

The bridge control register provides many of the same controls for the secondary interface that are provided by the command register for the primary interface. Some bits affect the operation of both interfaces.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Bridge control															
Type	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Bridge control**
Type: Read-only, Read/Write
Offset: 3Eh
Default: 0000h

Table 4−5. Bridge Control Register Description

BIT	TYPE	FUNCTION
15−12	R	Reserved. Bits 15−12 return 0s when read.
11	R/W	Discard timer $\overline{\text{SERR}}$ enable. 0 = $\overline{\text{SERR}}$ signaling disabled for primary discard time-outs (default) 1 = $\overline{\text{SERR}}$ signaling enabled for primary discard time-outs
10	R/W	Discard timer status. Once set, this bit must be cleared by writing 1 to this bit. 0 = No discard timer error (default) 1 = Discard timer error. Either primary or secondary discard timer expired and a delayed transaction was discarded from the queue in the bridge.
9	R/W	Secondary discard timer. Selects the number of PCI clocks that the bridge waits for a master on the secondary interface to repeat a delayed transaction request. 0 = Secondary discard timer counts 2^{15} PCI clock cycles (default) 1 = Secondary discard timer counts 2^{10} PCI clock cycles
8	R/W	Primary discard timer. Selects the number of PCI clocks that the bridge waits for a master on the primary interface to repeat a delayed transaction request. 0 = Primary discard timer counts 2^{15} PCI clock cycles (default) 1 = Primary discard timer counts 2^{10} PCI clock cycles
7	R	Fast back-to-back capable. The bridge never generates fast back-to-back transactions to different secondary devices. Bit 7 returns 0 when read.
6	R/W	Secondary bus reset. When bit 6 is set, the secondary reset signal ($\overline{\text{S\_RST}}$) is asserted. $\overline{\text{S\_RST}}$ is deasserted by resetting this bit. Bit 6 is encoded as: 0 = Do not force the assertion of $\overline{\text{S\_RST}}$ (default). 1 = Force the assertion of $\overline{\text{S\_RST}}$.

Table 4−5. Bridge Control Register Description (continued)

BIT	TYPE	FUNCTION
5	R/W	Master abort mode. Bit 5 controls how the bridge responds to a master abort that occurs on either interface when the bridge is the master. If this bit is set, the posted write transaction has completed on the requesting interface, and SERR enable (bit 8) of the command register (offset 04h, see Section 4.3) is 1, then P_SERR is asserted when a master abort occurs. If the transaction has not completed, then a target abort is signaled. If the bit is cleared, then all 1s are returned on reads and write data is accepted and discarded when a transaction that crosses the bridge is terminated with master abort. The default state of bit 5 after a reset is 0. 0 = Do not report master aborts (return FFFF FFFFh on reads and discard data on writes) (default). 1 = Report master aborts by signaling target abort if possible, or if SERR is enabled via bit 1 of this register, by asserting SERR.
4	R	Reserved. Returns 0 when read. Writes have no effect.
3	R/W	VGA enable. When bit 3 is set, the bridge positively decodes and forwards VGA-compatible memory addresses in the video frame buffer range 000A 0000h−000B FFFFh, I/O addresses in the range 03B0h−03BBh, and 03C0−03DFh from the primary to the secondary interface, independent of the I/O and memory address ranges. When this bit is set, the bridge blocks forwarding of these addresses from the secondary to the primary. Reset clears this bit. Bit 3 is encoded as: 0 = Do not forward VGA-compatible memory and I/O addresses from the primary to the secondary interface (default). 1 = Forward VGA-compatible memory and I/O addresses from the primary to the secondary, independent of the I/O and memory address ranges and independent of the ISA enable bit.
2	R/W	ISA enable. When bit 2 is set, the bridge blocks the forwarding of ISA I/O transactions from the primary to the secondary, addressing the last 768 bytes in each 1K-byte block. This applies only to the addresses (defined by the I/O window registers) that are located in the first 64K bytes of PCI I/O address space. From the secondary to the primary, I/O transactions are forwarded if they address the last 768 bytes in each 1K-byte block in the address range specified in the I/O window registers. Bit 2 is encoded as: 0 = Forward all I/O addresses in the address range defined by the I/O base and I/O limit registers (default). 1 = Block forwarding of ISA I/O addresses in the address range defined by the I/O base and I/O limit registers when these I/O addresses are in the first 64K bytes of PCI I/O address space and address the top 768 bytes of each 1K-byte block.
1	R/W	SERR enable. Bit 1 controls the forwarding of secondary interface SERR assertions to the primary interface. Only when this bit is set does the bridge forward S_SERR to the primary bus signal P_SERR. For the primary interface to assert SERR, bit 8 of the command register (offset 04h, see Section 4.3) must be set. 0 = SERR disabled (default) 1 = SERR enabled
0	R/W	Parity error response enable. Bit 0 controls the bridge response to parity errors on the secondary interface. When this bit is set, the bridge asserts S_PERR to report parity errors on the secondary interface. 0 = Ignore address and parity errors on the secondary interface (default). 1 = Enable parity error reporting and detection on the secondary interface.

5 Extension Registers

The TI extension registers are those registers that lie outside the standard PCI-to-PCI bridge device configuration space (i.e., registers 40h−FFh in PCI configuration space in the PCI2050B bridge). These registers can be accessed through configuration reads and writes. The TI extension registers add flexibility and performance benefits to the standard PCI-to-PCI bridge. Mapping of the extension registers is contained in Table 4−1.

5.1 Chip Control Register

The chip control register contains read/write and read-only bits and has a default value of 00h. This register is used to control the functionality of certain PCI transactions.

Bit	7	6	5	4	3	2	1	0
Name	Chip control							
Type	R	R	R/W	R/W	R	R	R/W	R
Default	0	0	0	0	0	0	0	0

Register: **Chip control**
Type: Read/Write, Read-only
Offset: 40h
Default: 00h

Table 5−1. Chip Control Register Description

BIT	TYPE	FUNCTION
7−6	R	Reserved. Bits 7−6 return 0s when read.
5	R/W	Transaction forwarding control for I/O and memory cycles. 0 = Transaction forwarding controlled by bits 0 and 1 of the command register (offset 04h, see Section 4.3) (default). 1 = Transaction forwarding is disabled if GPIO3 is driven high.
4	R/W	Memory read prefetch. When set, bit 4 enables the memory read prefetch. 0 = Upstream memory reads are disabled (default). 1 = Upstream memory reads are enabled
3−2	R	Reserved. Bits 3 and 2 return 0s when read.
1	R/W	Memory write and memory write and invalidate disconnect control. 0 = Disconnects on queue full or 4-KB boundaries (default) 1 = Disconnects on queue full, 4-KB boundaries and cacheline boundaries.
0	R	Reserved. Bit 0 returns 0 when read.

5.2 Extended Diagnostic Register

The extended diagnostic register is read or write and has a default value of 00h. Bit 0 of this register is used to reset both the PCI2050B bridge and the secondary bus.

Bit	7	6	5	4	3	2	1	0
Name	Extended diagnostic							
Type	R	R	R	R	R	R	R	W
Default	0	0	0	0	0	0	0	0

Register: **Extended diagnostic**
Type: Read-only, Write-only
Offset: 41h
Default: 00h

Table 5−2. Extended Diagnostic Register Description

BIT	TYPE	FUNCTION
7−1	R	Reserved. Bits 7−1 return 0s when read.
0	W	Writing a 1 to this bit causes the PCI2050B bridge to set bit 6 of the bridge control register (offset 3Eh, see Section 4.32) and then internally reset the PCI2050B bridge. Bit 6 of the bridge control register is not reset by the internal reset. Bit 0 is self-clearing.

5.3 Arbiter Control Register

The arbiter control register is used for the bridge internal arbiter. The arbitration scheme used is a two-tier rotational arbitration. The PCI2050B bridge is the only secondary bus initiator that defaults to the higher priority arbitration tier.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Arbiter control															
Type	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Register: **Arbiter control**
Type: Read-only, Read/Write
Offset: 42h
Default: 0200h

Table 5−3. Arbiter Control Register Description

BIT	TYPE	FUNCTION
15−10	R	Reserved. Bits 15−10 return 0s when read.
9	R/W	Bridge tier select. This bit determines in which tier the PCI2250 bridge is placed in the two-tier arbitration scheme. 0 = Low priority tier 1 = High priority tier (default)
8	R/W	$\overline{\text{GNT8}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT8}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
7	R/W	$\overline{\text{GNT7}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT7}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
6	R/W	$\overline{\text{GNT6}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT6}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
5	R/W	$\overline{\text{GNT5}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT5}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
4	R/W	$\overline{\text{GNT4}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT4}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
3	R/W	$\overline{\text{GNT3}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT3}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
2	R/W	$\overline{\text{GNT2}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT2}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
1	R/W	$\overline{\text{GNT1}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT1}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier
0	R/W	$\overline{\text{GNT0}}$ tier select. This bit determines in which tier the $\overline{\text{S\_GNT0}}$ is placed in the arbitration scheme. This bit is encoded as: 0 = Low priority tier (default) 1 = High priority tier

5.4 P_SERR Event Disable Register

The P_SERR event disable register is used to enable/disable the SERR event on the primary interface. All events are enabled by default.

Bit	7	6	5	4	3	2	1	0
Name	P_SERR event disable							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Register: **P_SERR event disable**
Type: Read-only, Read/Write
Offset: 64h
Default: 00h

Table 5−4. P_SERR Event Disable Register Description

BIT	TYPE	FUNCTION
7	R	Reserved. Bit 7 returns 0 when read.
6	R/W	Master delayed read time-out. 0 = P_SERR signaled on a master time-out after 2^{24} retries on a delayed read (default). 1 = P_SERR is not signaled on a master time-out.
5	R/W	Master delayed write time-out. 0 = P_SERR signaled on a master time-out after 2^{24} retries on a delayed write (default). 1 = P_SERR is not signaled on a master time-out.
4	R/W	Master abort on posted write transactions. When set, bit 4 enables P_SERR reporting on master aborts on posted write transactions. 0 = Master aborts on posted writes enabled (default) 1 = Master aborts on posted writes disabled
3	R/W	Target abort on posted writes. When set, bit 3 enables P_SERR reporting on target aborts on posted write transactions. 0 = Target aborts on posted writes enabled (default). 1 = Target aborts on posted writes disabled.
2	R/W	Master posted write time-out. 0 = P_SERR signaled on a master time-out after 2^{24} retries on a posted write (default). 1 = P_SERR is not signaled on a master time-out.
1	R/W	Posted write parity error. 0 = P_SERR signaled on a posted write parity error (default). 1 = P_SERR is not signaled on a posted write parity error.
0	R	Reserved. Bit 0 returns 0 when read.

5.5 GPIO Output Data Register

The GPIO output data register controls the data driven on the GPIO terminals configured as outputs. If both an output-high bit and an output-low bit are set for the same GPIO terminal, the output-low bit takes precedence. The output data bits have no effect on a GPIO terminal that is programmed as an input.

Bit	7	6	5	4	3	2	1	0
Name	GPIO output data							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **GPIO output data**
Type: Read/Write
Offset: 65h
Default: 00h

Table 5−5. GPIO Output Data Register Description

BIT	TYPE	FUNCTION
7	R/W	GPIO3 output high. Writing a 1 to this bit causes the GPIO signal to be driven high. Writing a 0 has no effect.
6	R/W	GPIO2 output high. Writing a 1 to this bit causes the GPIO signal to be driven high. Writing a 0 has no effect.
5	R/W	GPIO1 output high. Writing a 1 to this bit causes the GPIO signal to be driven high. Writing a 0 has no effect.
4	R/W	GPIO0 output high. Writing a 1 to this bit causes the GPIO signal to be driven high. Writing a 0 has no effect.
3	R/W	GPIO3 output low. Writing a 1 to this bit causes the GPIO signal to be driven low. Writing a 0 has no effect.
2	R/W	GPIO2 output low. Writing a 1 to this bit causes the GPIO signal to be driven low. Writing a 0 has no effect.
1	R/W	GPIO1 output low. Writing a 1 to this bit causes the GPIO signal to be driven low. Writing a 0 has no effect.
0	R/W	GPIO0 output low. Writing a 1 to this bit causes the GPIO signal to be driven low. Writing a 0 has no effect.

5.6 GPIO Output Enable Register

The GPIO output enable register controls the direction of the GPIO signal. By default all GPIO terminals are inputs. If both an output-enable bit and an input-enable bit are set for the same GPIO terminal, the input-enable bit takes precedence.

Bit	7	6	5	4	3	2	1	0
Name	GPIO output enable							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register: **GPIO output enable**
Type: Read/Write
Offset: 66h
Default: 00h

Table 5−6. GPIO Output Enable Register Description

BIT	TYPE	FUNCTION
7	R/W	GPIO3 output enable. Writing a 1 to this bit causes the GPIO signal to be configured as an output. Writing a 0 has no effect.
6	R/W	GPIO2 output enable. Writing a 1 to this bit causes the GPIO signal to be configured as an output. Writing a 0 has no effect.
5	R/W	GPIO1 output enable. Writing a 1 to this bit causes the GPIO signal to be configured as an output. Writing a 0 has no effect.
4	R/W	GPIO0 output enable. Writing a 1 to this bit causes the GPIO signal to be configured as an output. Writing a 0 has no effect.
3	R/W	GPIO3 input enable. Writing a 1 to this bit causes the GPIO signal to be configured as an input. Writing a 0 has no effect.
2	R/W	GPIO2 input enable. Writing a 1 to this bit causes the GPIO signal to be configured as an input. Writing a 0 has no effect.
1	R/W	GPIO1 input enable. Writing a 1 to this bit causes the GPIO signal to be configured as an input. Writing a 0 has no effect.
0	R/W	GPIO0 input enable. Writing a 1 to this bit causes the GPIO signal to be configured as an input. Writing a 0 has no effect.

5.7 GPIO Input Data Register

The GPIO input data register returns the current state of the GPIO terminals when read.

Bit	7	6	5	4	3	2	1	0
Name	GPIO input data							
Type	R	R	R	R	R	R	R	R
Default	X	X	X	X	0	0	0	0

Register: **GPIO input data**
Type: Read-only
Offset: 67h
Default: X0h

Table 5−7. GPIO Input Data Register Description

BIT	TYPE	FUNCTION
7−4	R	GPIO3−GPIO0 input data. These four bits return the current state of the GPIO terminals.
3−0	R	Reserved. Bits 3−0 return 0s when read.

5.8 Secondary Clock Control Register

The secondary clock control register is used to control the secondary clock outputs.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Secondary clock control															
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Secondary clock control**
Type: Read-only, Read/Write
Offset: 68h
Default: 0000h

Table 5−8. Secondary Clock Control Register Description

BIT	TYPE	FUNCTION
15−14	R	Reserved. These bits return 0 when read.
13	R/W	S_CLKOUT9 disable. 0 = S_CLKOUT9 enabled (default). 1 = S_CLKOUT9 disabled and driven high.
12	R/W	S_CLKOUT8 disable. 0 = S_CLKOUT8 enabled (default). 1 = S_CLKOUT8 disabled and driven high.
11	R/W	S_CLKOUT7 disable. 0 = S_CLKOUT7 enabled (default). 1 = S_CLKOUT7 disabled and driven high.
10	R/W	S_CLKOUT6 disable. 0 = S_CLKOUT6 enabled (default). 1 = S_CLKOUT6 disabled and driven high.
9	R/W	S_CLKOUT5 disable. 0 = S_CLKOUT5 enabled (default). 1 = S_CLKOUT5 disabled and driven high.
8	R/W	S_CLKOUT4 disable. 0 = S_CLKOUT4 enabled (default). 1 = S_CLKOUT4 disabled and driven high.
7−6	R/W	S_CLKOUT3 disable. 00, 01, 10 = S_CLKOUT3 enabled (00 is the default). 11 = S_CLKOUT3 disabled and driven high.
5−4	R/W	S_CLKOUT2 disable. 00, 01, 10 = S_CLKOUT2 enabled (00 is the default). 11 = S_CLKOUT2 disabled and driven high.
3−2	R/W	S_CLKOUT1 disable. 00, 01, 10 = S_CLKOUT1 enabled (00 is the default). 11 = S_CLKOUT1 disabled and driven high.
1−0	R/W	S_CLKOUT0 disable. 00, 01, 10 = S_CLKOUT0 enabled (00 is the default). 11 = S_CLKOUT0 disabled and driven high.

5.9 P_SERR Status Register

The P_SERR status register indicates what caused a SERR event on the primary interface.

Bit	7	6	5	4	3	2	1	0
Name	P_SERR status							
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Register: **P_SERR status**
Type: Read-only Read/Write
Offset: 6Ah
Default: 00h

Table 5−9. P_SERR Status Register Description

BIT	TYPE	FUNCTION
7	R	Reserved. Bit 7 returns 0 when read.
6	R/W	Master delayed read time-out. A 1 indicates that $\overline{\text{P\_SERR}}$ was signaled because of a master time-out after 2^{24} retries on a delayed read.
5	R/W	Master delayed write time-out. A 1 indicates that $\overline{\text{P\_SERR}}$ was signaled because of a master time-out after 2^{24} retries on a delayed write.
4	R/W	Master abort on posted write transactions. A 1 indicates that $\overline{\text{P\_SERR}}$ was signaled because of a master abort on a posted write.
3	R/W	Target abort on posted writes. A 1 indicates that $\overline{\text{P\_SERR}}$ was signaled because of a target abort on a posted write.
2	R/W	Master posted write time-out. A 1 indicates that $\overline{\text{P\_SERR}}$ was signaled because of a master time-out after 2^{24} retries on a posted write.
1	R/W	Posted write parity error. A 1 indicates that $\overline{\text{P\_SERR}}$ was signaled because of parity error on a posted write.
0	R	Reserved. Bit 0 returns 0 when read.

5.10 Power-Management Capability ID Register

The power-management capability ID register identifies the linked list item as the register for PCI power management. The power-management capability ID register returns 01h when read, which is the unique ID assigned by the PCI SIG for the PCI location of the capabilities pointer and the value.

Bit	7	6	5	4	3	2	1	0
Name	Power-management capability ID							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	1

Register: **Power-management capability ID**
Type: Read-only
Offset: DCh
Default: 01h

5.11 Power-Management Next-Item Pointer Register

The power-management next-item pointer register is used to indicate the next item in the linked list of PCI power-management capabilities. The next-item pointer returns E4h in CompactPCI mode, indicating that the PCI2050B bridge supports more than one extended capability, but in all other modes returns 00h, indicating that only one extended capability is provided.

Bit	7	6	5	4	3	2	1	0
Name	Power-management next-item pointer							
Type	R	R	R	R	R	R	R	R
Default	1	1	1	0	0	1	0	0

Register: **Power-management next-item pointer**
Type: Read-only
Offset: DDh
Default: E4h cPCI mode
00h All other modes

5.12 Power-Management Capabilities Register

The power management capabilities register contains information on the capabilities of the PCI2050B functions related to power management. The PCI2050B function supports D0, D1, D2, and D3 power states when MS1 is low. The PCI2050B bridge does not support any power states when MS1 is high.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Power-management capabilities															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0

Register: **Power-management capabilities**
Type: Read-only
Offset: DEh
Default: 0602h or 0001h

Table 5−10. Power-Management Capabilities Register Description

BIT	TYPE	FUNCTION
15−11	R	$\overline{\text{PME}}$ support. This five-bit field indicates the power states that the device supports asserting $\overline{\text{PME}}$. A 0 for any of these bits indicates that the PCI2050B bridge cannot assert $\overline{\text{PME}}$ from that power state. For the PCI2050B bridge, these five bits return 00000b when read, indicating that $\overline{\text{PME}}$ is not supported.
10	R	D2 support. This bit returns 1 when MS0 is 0, indicating that the bridge function supports the D2 device power state. This bit returns 0 when MS0 is 1, indicating that the bridge function does not support the D2 device power state.
9	R	D1 support. This bit returns 1 when MS0 is 0, indicating that the bridge function supports the D1 device power state. This bit returns 0 when MS0 is 1, indicating that the bridge function does not support the D1 device power state.
8−6	R	Reserved. Bits 8−6 return 0s when read.
5	R	Device specific initialization. This bit returns 0 when read, indicating that the bridge function does not require special initialization (beyond the standard PCI configuration header) before the generic class device driver is able to use it.
4	R	Auxiliary power source. This bit returns a 0 when read because the PCI2050B bridge does not support $\overline{\text{PME}}$ signaling.
3	R	PMECLK. This bit returns a 0 when read because the $\overline{\text{PME}}$ signaling is not supported.
2−0	R	Version. This three-bit register returns the *PCI Bus Power Management Interface Specification* revision. 001 = Revision 1.0, MS0 = 1 010 = Revision 1.1, MS0 = 0

5.13 Power-Management Control/Status Register

The power-management control/status register determines and changes the current power state of the PCI2050B bridge. The contents of this register are not affected by the internally generated reset caused by the transition from $D3_{hot}$ to D0 state.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Power-management control/status															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: **Power-management control/status**
Type: Read-only, Read/Write
Offset: E0h
Default: 0000h

Table 5−11. Power-Management Control/Status Register

BIT	TYPE	FUNCTION
15	R	$\overline{\text{PME}}$ status. This bit returns a 0 when read because the PCI2050B bridge does not support $\overline{\text{PME}}$.
14−13	R	Data scale. This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the data register. These bits return only 00b, because the data register is not implemented.
12−9	R	Data select. This 4-bit field is used to select which data is to be reported through the data register and data-scale field. These bits return only 0000b, because the data register is not implemented.
8	R	$\overline{\text{PME}}$ enable. This bit returns a 0 when read because the PCI2050B bridge does not support $\overline{\text{PME}}$ signaling.
7−2	R	Reserved. Bits 7−2 return 0s when read.
1−0	R/W	Power state. This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of this is given below: 00 = D0 01 = D1 10 = D2 11 = $D3_{hot}$

5.14 PMCSR Bridge Support Register

The PMCSR bridge support register is required for all PCI bridges and supports PCI-bridge-specific functionality.

Bit	7	6	5	4	3	2	1	0
Name	PMCSR bridge support							
Type	R	R	R	R	R	R	R	R
Default	X	X	0	0	0	0	0	0

Register: **PMCSR bridge support**
Type: Read-only
Offset: E2h
Default: X0h

Table 5−12. PMCSR Bridge Support Register Description

BIT	TYPE	FUNCTION
7	R	Bus power control enable. This bit returns the value of the MS1/BCC input. 0 = Bus power/ clock control disabled. 1 = Bus power/clock control enabled.
6	R	B2/B3 support for $D3_{hot}$. This bit returns the value of MS1/BCC input. When this bit is 1, the secondary clocks are stopped when the device is placed in $D3_{hot}$. When this bit is 0, the secondary clocks remain on in all device states. Note: If the primary clock is stopped, then the secondary clocks stop because the primary clock is used to generate the secondary clocks.
5−0	R	Reserved.

5.15 Data Register

The data register is an optional, 8-bit read-only register that provides a mechanism for the function to report state-dependent operating data such as power consumed or heat dissipation. The PCI2050B bridge does not implement the data register.

Bit	7	6	5	4	3	2	1	0
Name	Data							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Register: **Data**
Type: Read-only
Offset: E3h
Default: 00h

5.16 HS Capability ID Register

The HS capability ID register identifies the linked list item as the register for cPCI hot-swap capabilities. The register returns 06h when read, which is the unique ID assigned by the PICMG for PCI location of the capabilities pointer and the value. In Intel™-compatible mode, this register is read-only and defaults to 00h.

Bit	7	6	5	4	3	2	1	0
Name	HS capability ID							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	1	1	0

Register: **HS capability ID**
Type: Read-only
Offset: E4h
Default: 06h TI mode
00h Intel-compatible mode

5.17 HS Next-Item Pointer Register

The HS next-item pointer register is used to indicate the next item in the linked list of cPCI hot swap capabilities. Because this is the last extended capability that the PCI2050B bridge supports, the next-item pointer returns all 0s.

Bit	7	6	5	4	3	2	1	0
Name	HS next-item pointer							
Type	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Register: **HS next-item pointer**
Type: Read-only
Offset: E5h
Default: 00h

5.18 Hot-Swap Control Status Register

The hot-swap control status register contains control and status information for cPCI hot swap resources.

Bit	7	6	5	4	3	2	1	0
Name	Hot swap control status							
Type	R	R	R	R	R/W	R	R/W	R
Default	0	0	0	0	0	0	0	0

Register: **Hot-swap control status**
Type: Read-only, Read/Write
Offset: E6h
Default: 00h

Table 5−13. Hot-Swap Control Status Register Description

BIT	TYPE	FUNCTION
7	R	$\overline{\text{ENUM}}$ insertion status. When set, the $\overline{\text{ENUM}}$ output is driven by the PCI2050B bridge. This bit defaults to 0, and is set after a PCI reset occurs, the pre-load of serial ROM is complete, the ejector handle is closed, and bit 6 is 0. Thus, this bit is set following an insertion when the board implementing the PCI2050B bridge is ready for configuration. This bit cannot be set under software control.
6	R	$\overline{\text{ENUM}}$ extraction status. When set, the $\overline{\text{ENUM}}$ output is driven by the PCI2050B bridge. This bit defaults to 0, and is set when the ejector handle is opened and bit 7 is 0. Thus, this bit is set when the board implementing the PCI2050B bridge is about to be removed. This bit cannot be set under software control.
5−4	R	Reserved. Bits 5 and 4 return 0s when read.
3	R/W	LED ON/OFF. This bit defaults to 0, and controls the external LED indicator (HS_LED) under normal conditions. However, for a duration following a $\overline{\text{PCI\_RST}}$, the HS_LED output is driven high by the PCI2050B bridge and this bit is ignored. When this bit is interpreted, a 1 causes HS_LED high and a 0 causes HS_LED low. Following $\overline{\text{PCI\_RST}}$, the HS_LED output is driven high by the PCI2050B bridge until the ejector handle is closed. When these conditions are met, the HS_LED is under software control via this bit.
2	R	Reserved. Bit 2 returns 0 when read.
1	R/W	$\overline{\text{ENUM}}$ interrupt mask. This bit allows the $\overline{\text{HS\_ENUM}}$ output to be masked by software. Bits 6 and 7 are set independently from this bit. 0 = Enable $\overline{\text{HS\_ENUM}}$ output 1 = Mask $\overline{\text{HS\_ENUM}}$ output
0	R	Reserved. Bit 0 returns 0 when read.

5.19 Diagnostics Register

The diagnostics register enables or disables posted write combing of the PCI2050B bridge.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Diagnostics															
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register: TI Diagnostics
Type: Read-only, read/write (see individual bit descriptions)
Offset: F0h
Default: 0000h

Table 5−14. Diagnostics Register Description

BIT	TYPE	FUNCTION
15−1	R	Reserved. Bits 15−1 return 0s when read.
0	R/W	Disable posted write combining. 0 = Enable posted write combining (default) 1 = Disable posted write combining

6 Electrical Characteristics

6.1 Absolute Maximum Ratings Over Operating Temperature Ranges †

Supply voltage range: V_{CC} . . . . . −0.5 V to 3.6 V
: P_V_{CCP} . . . . . −0.5 V to 6 V
: S_V_{CCP} . . . . . −0.5 V to 6 V
Input voltage range, V_I: CMOS‡ . . . . . −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I: PCI§ . . . . . −0.5 V to 6 V
Output voltage range, V_O: CMOS‡ . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O: PCI§ . . . . . −0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2) . . . . . ±20 mA
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Virtual junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ CMOS terminals are 23−25, 27−30, 32, 33, 35, 36, 38, 39, 41, 42, 126−130, 132−134 for PDV- and PPM-packaged devices, and J6, J18, J19, K1, K2, K5, K6. K14, K17, K18, L1, L2, L5, L14, L15, L17,M1, M3, M6, N1, N2, N6, P1 for the GHK- and ZHK-packaged devices.

§ All signal terminals other than CMOS terminals are PCI terminals.

NOTES: 1. Applies for external input and bidirectional buffers. PCI terminals are measured with respect to V_{CCP} instead of V_{CC}. The limit is specified for a dc condition.

2. Applies for external input and bidirectional buffers. PCI terminals are measured with respect to V_{CCP} instead of V_{CC}. The limit is specified for a dc condition.

6.2 Recommended Operating Conditions (see Note 3)

			OPERATION	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (core)	Commercial	3.3 V	3	3.3	3.6	V
P_V_{CCP}	PCI primary bus I/O clamping rail voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
S_V_{CCP}	PCI secondary bus I/O clamping rail voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
V_{IH}†	High-level input voltage	PCI	3.3 V	0.5 V_{CCP}		V_{CCP}	V
			5 V	2		V_{CCP}	
		CMOS		0.7 V_{CC}		V_{CC}	
		CLK¶		0.57 V_{CCP}		V_{CCP}	
		P_RST_L		0.77 V_{CCP}		V_{CCP}	
		TRST_L		0.9 V_{CC}		V_{CC}	
V_{IL}†	Low-level input voltage	PCI	3.3 V	0		0.3 V_{CCP}	V
			5 V	0		0.8	
		CMOS		0		0.2 V_{CC}	
		CLK¶		0		0.2 V_{CCP}	
V_I	Input voltage	PCI		0		V_{CCP}	V
		CMOS		0		V_{CCP}	
V_O‡	Output voltage	Output voltage		0		V_{CC}	V
t_t	Input transition time (t_r and t_f)	PCI		1		4	ns
		CMOS		0		6	
T_A	Operating ambient temperature range	PCI2050B		0	25	70	°C
		PCI2050BI		−40	25	85	
T_J§	Virtual junction temperature			0	25	115	°C

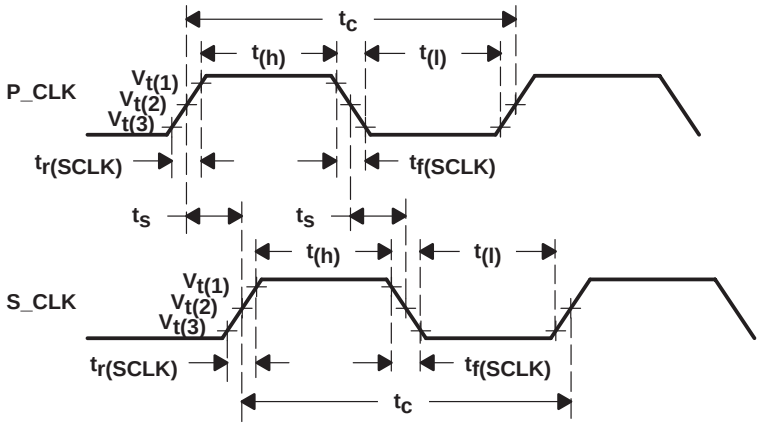
NOTES: 3. Unused terminals (input or I/O) must be held high or low to prevent them from floating.
† Applies to external input and bidirectional buffers without hysteresis
‡ Applies to external output buffers
§ These junction temperatures reflect simulation conditions. The customer is responsible for verifying junction temperature.
¶ CLK includes P_CLK and S_CLK terminals.

6.3 Electrical Characteristics Over Recommended Operating Conditions

PARAMETER		TERMINALS	OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	PCI	3.3 V	I_{OH} = −0.5 mA	0.9 V_{CC}		V
			5 V	I_{OH} = −2 mA	2.4		
		CMOS1†		I_{OH} = −4 mA	2.1		
		CMOS2‡		I_{OH} = −8 mA	2.1		
V_{OL}	Low-level output voltage	PCI	3.3 V	I_{OL} = 1.5 mA		0.1 V_{CC}	V
			5 V	I_{OH} = −2 mA		0.55	
		CMOS1†		I_{OH} = 4 mA		0.5	
		CMOS2‡		I_{OH} = 8 mA		0.5	
I_{IH}	High-level input current	Input terminals		$V_I = V_{CCP}$		10	µA
		I/O terminals§		$V_I = V_{CCP}$		10	
I_{IL}	Low-level input current	Input terminals		V_I = GND		−1	µA
		I/O terminals§		V_I = GND		−10	
		Pu terminals¶		V_I = GND		−60	
I_{OZ}	High-impedance output current	Output terminals		$V_O = V_{CCP}$ or GND		±10	µA

† CMOS1 includes terminals 24, 25, 27, 28 for PDV- and PDM-packaged devices and K1, K2, K5, K6 for the GHK- and ZHK-packaged devices.
‡ CMOS2 includes terminals 29, 30, 33, 35, 36, 38, 39, 41, 42, 128, 130 for PDV- and PDM-packaged devices and K17, L1, L2, L5, L14, M1, M3, M6, N1, N2, N6, P1 for the GHK- and ZHK-packaged devices.
§ For I/O terminals, the input leakage current (I_{IL} and I_{IH}) includes the I_{OZ} leakage of the disabled output.
¶ Pu terminals include TDI, TMS, and TRST_L. These are pulled up with internal resistors.

6.4 66-MHz PCI Clock Signal AC Parameters

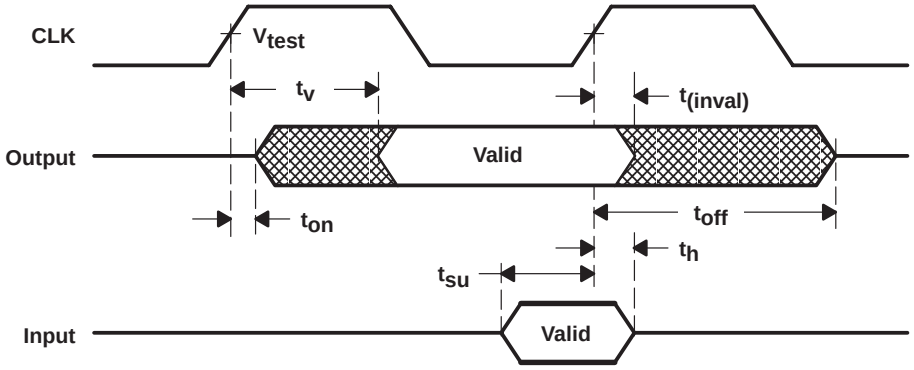


NOTE: $V_{t(1)}$ = 2.0 V for 5-V clocks; 0.5 V_{CC} for 3.3-V clocks
$V_{t(2)}$ = 1.5 V for 5-V clocks; 0.4 V_{CC} for 3.3-V clocks
$V_{t(3)}$ = 0.8 V for 5-V clocks; 0.3 V_{CC} for 3.3-V clocks

Figure 6−1. PCI Clock Signal AC Parameter Measurements

PARAMETER		MIN	MAX	UNIT
t_c	P_CLK, S_CLK cycle time	15	30	ns
$t_{(h)}$	P_CLK, S_CLK high time	6		ns
$t_{(l)}$	P_CLK, S_CLK low time	6		ns
$t_{(PSS)}$	P_CLK, S_CLK slew rate (0.2 V_{CC} to 0.6 V_{CC})	1.5	4	V/ns
$t_{d(SCLK)}$	Delay from P_CLK to S_CLK	0	7	ns
$t_{r(SCLK)}$	P_CLK rising to S_CLK rising	0	7	ns
$t_{f(SCLK)}$	P_CLK falling to S_CLK falling	0	7	ns
$t_{d(skew)}$	S_CLK0 duty cycle skew from P_CLK duty cycle		0.750	ns
t_{sk}	S_CLKx to SCLKy		0.500	ns

6.5 66-MHz PCI Signal Timing



NOTE: V_{test} = 1.5 V for 5-V signals; 0.4 V_{CC} for 3.3-V signals

Figure 6−2. PCI Signal Timing Measurement Conditions

PARAMETER		MIN	MAX	UNIT
$t_{v(bus)}$	CLK to signal valid delay—bused signals (see Notes 4, 5, and 6)	2	6	ns
$t_{v(ptp)}$	CLK to signal valid delay—point-to-point (see Notes 4, 5, and 6)	2	6	ns
t_{on}	Float to active delay (see Notes 4, 5, and 6)	2		ns
t_{off}	Active to float delay (see Notes 4, 5, and 6)		14	ns
$t_{su(bus)}$	Input setup time to CLK—bused signal (see Notes 4, 5, and 6)	3		ns
$t_{su(ptp)}$	Input setup time to CLK—point-to-point (see Notes 4, 5, and 6)	5		ns
t_h	Input signal hold time from CLK (see Notes 4 and 5)	0		ns

NOTES: 4. See Figure 6−2
5. All primary interface signals are synchronized to P_CLK and all secondary interface signals are synchronized to S_CLK.
6. Bused signals are as follows:
P_AD, P_C/BE, P_PAR, P_PERR, P_SERR, P_FRAME, P_IRDY, P_TRDY, P_LOCK, P_DEVSEL, P_STOP, P_IDSEL, S_AD, S_C/BE, S_PAR, S_PERR, S_SERR, S_FRAME, S_IRDY, S_TRDY, S_LOCK, S_DEVSEL, S_STOP

Point-to-point signals are as follows:
P_REQ, S_REQx, P_GNT, S_GNTx

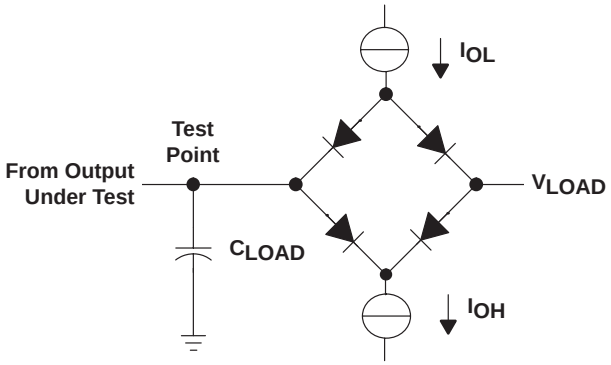
6.6 Parameter Measurement Information

LOAD CIRCUIT PARAMETERS

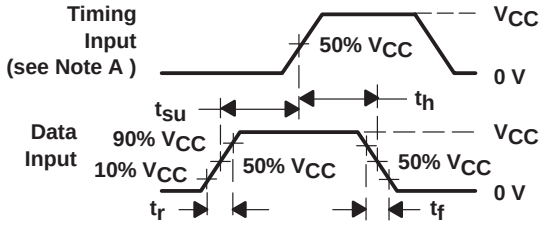
TIMING PARAMETER		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	50	8	−8	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	50	8	−8	1.5
	t_{PLZ}				
t_{pd}		50	8	−8	‡

† C_{LOAD} includes the typical load-circuit distributed capacitance.

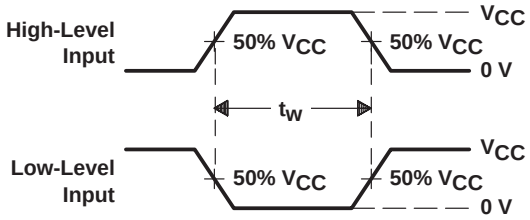
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}}$ = 50 Ω, where V_{OL} = 0.6 V, I_{OL} = 8 mA



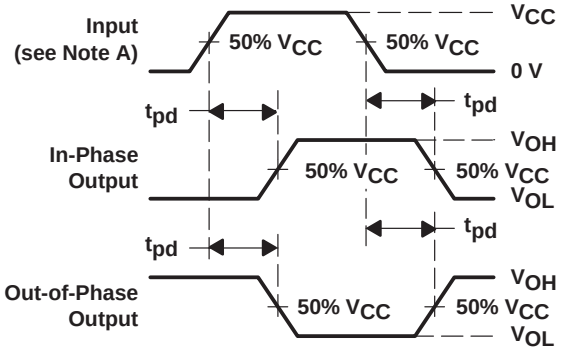
LOAD CIRCUIT



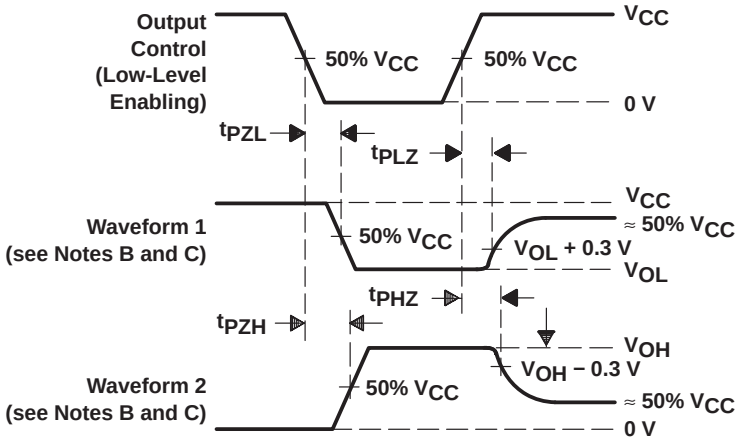
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, $t_r \le 6$ ns, $t_f \le 6$ ns.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 6−3. Load Circuit and Voltage Waveforms

6.7 PCI Bus Parameter Measurement Information

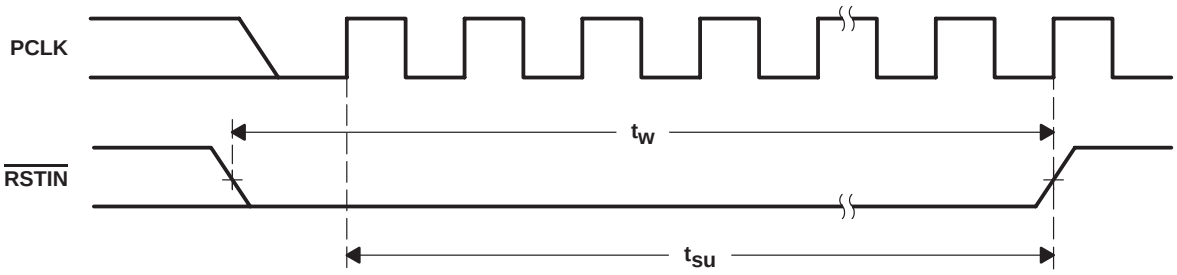
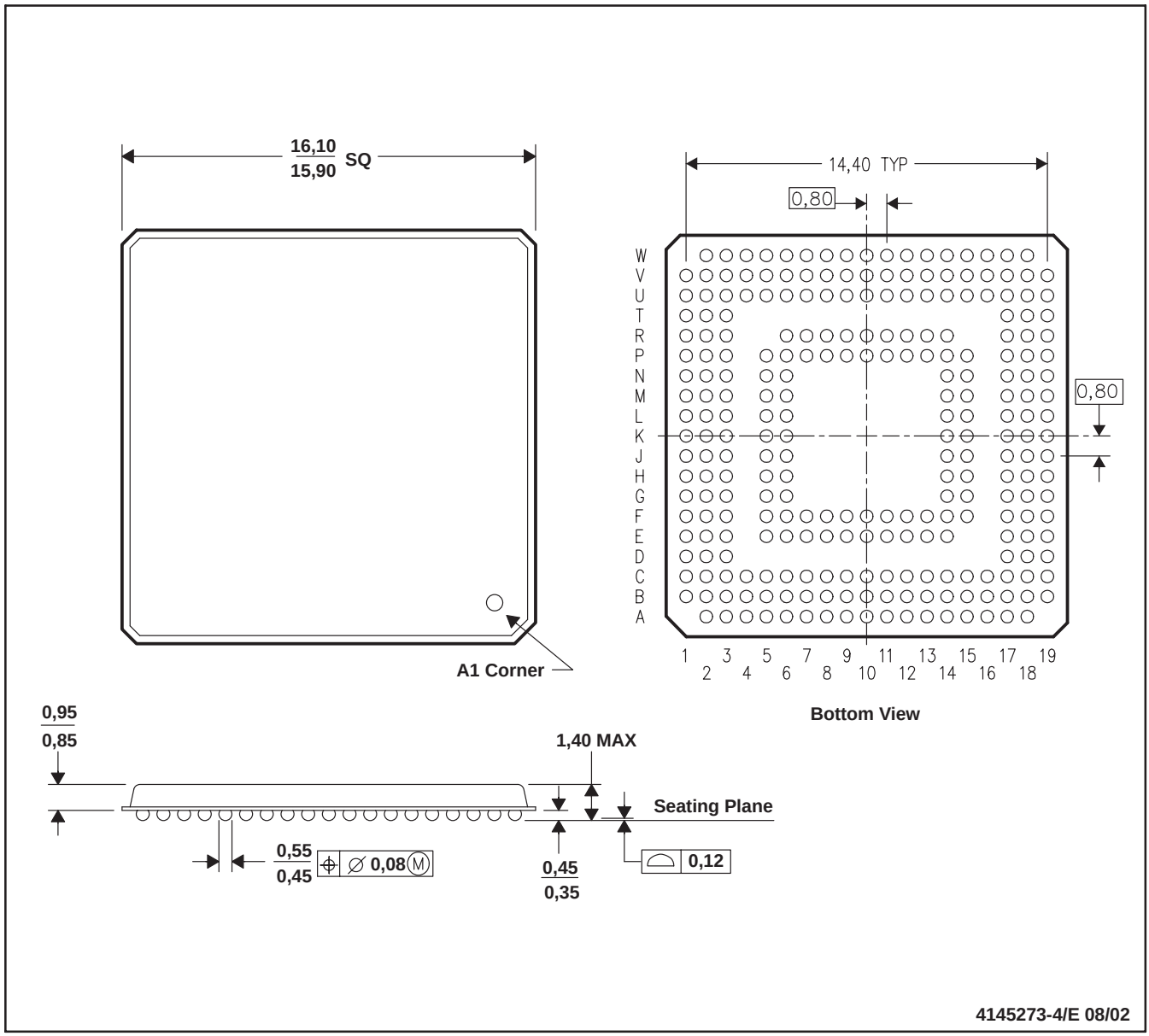


Figure 6−4. $\overline{\text{RSTIN}}$ Timing Waveforms

7 Mechanical Data

The PCI2050B device is packaged either in a GHK 257-ball MicroStar BGA™, a 208-terminal PDV package, a 208-terminal PPM package, or a RoHS-compliant ZHK 257-ball MicroStar BGA™. The following shows the mechanical dimensions for the GHK, PDV, PPM, and ZHK packages. The GHK and ZHK packages are mechanically identical; therefore, only the GHK mechanical drawing is shown.

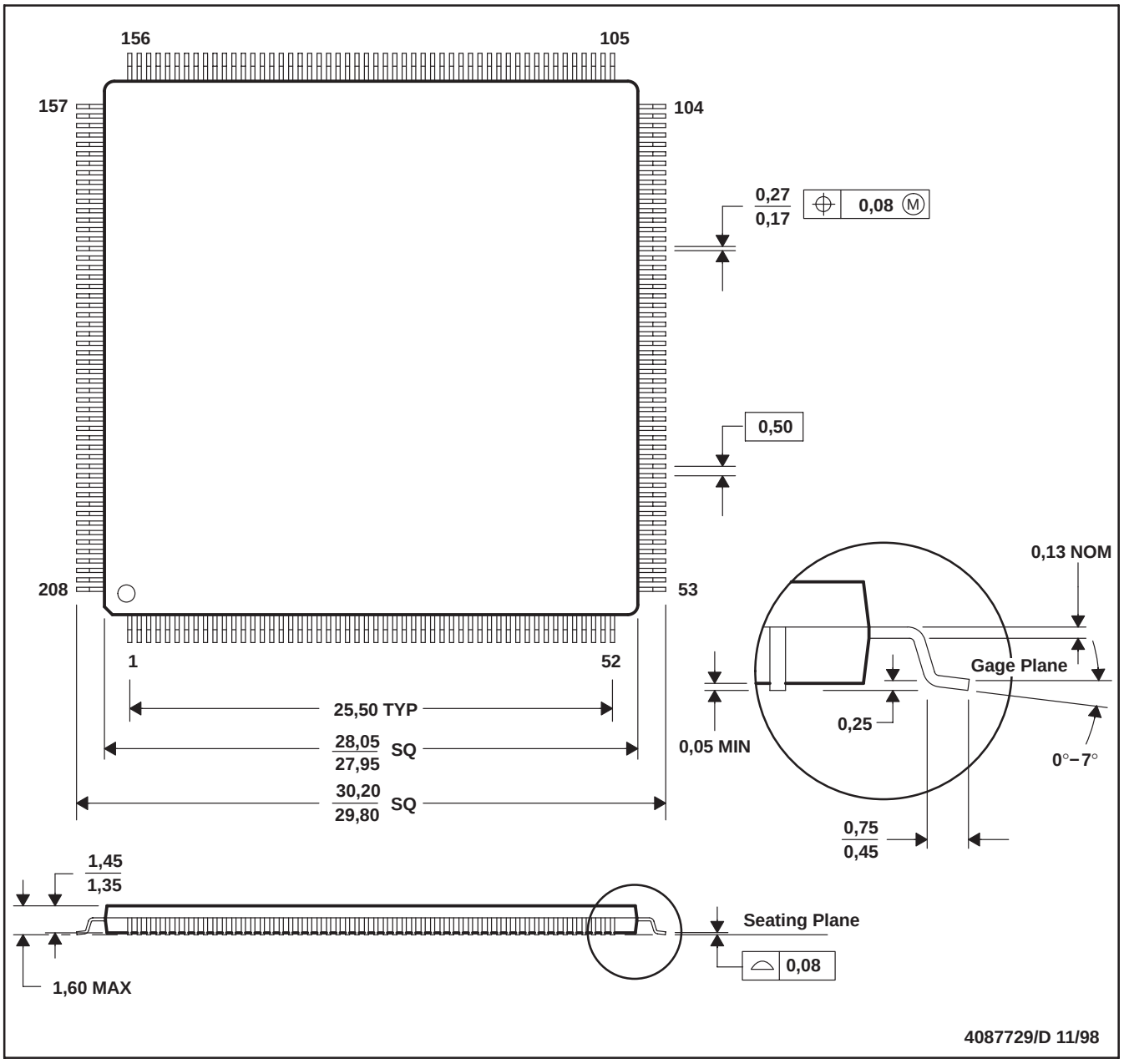
GHK (S-PBGA-N257) PLASTIC BALL GRID ARRAY



NOTES: D. All linear dimensions are in millimeters.
E. This drawing is subject to change without notice.
F. MicroStar BGA™ configuration.

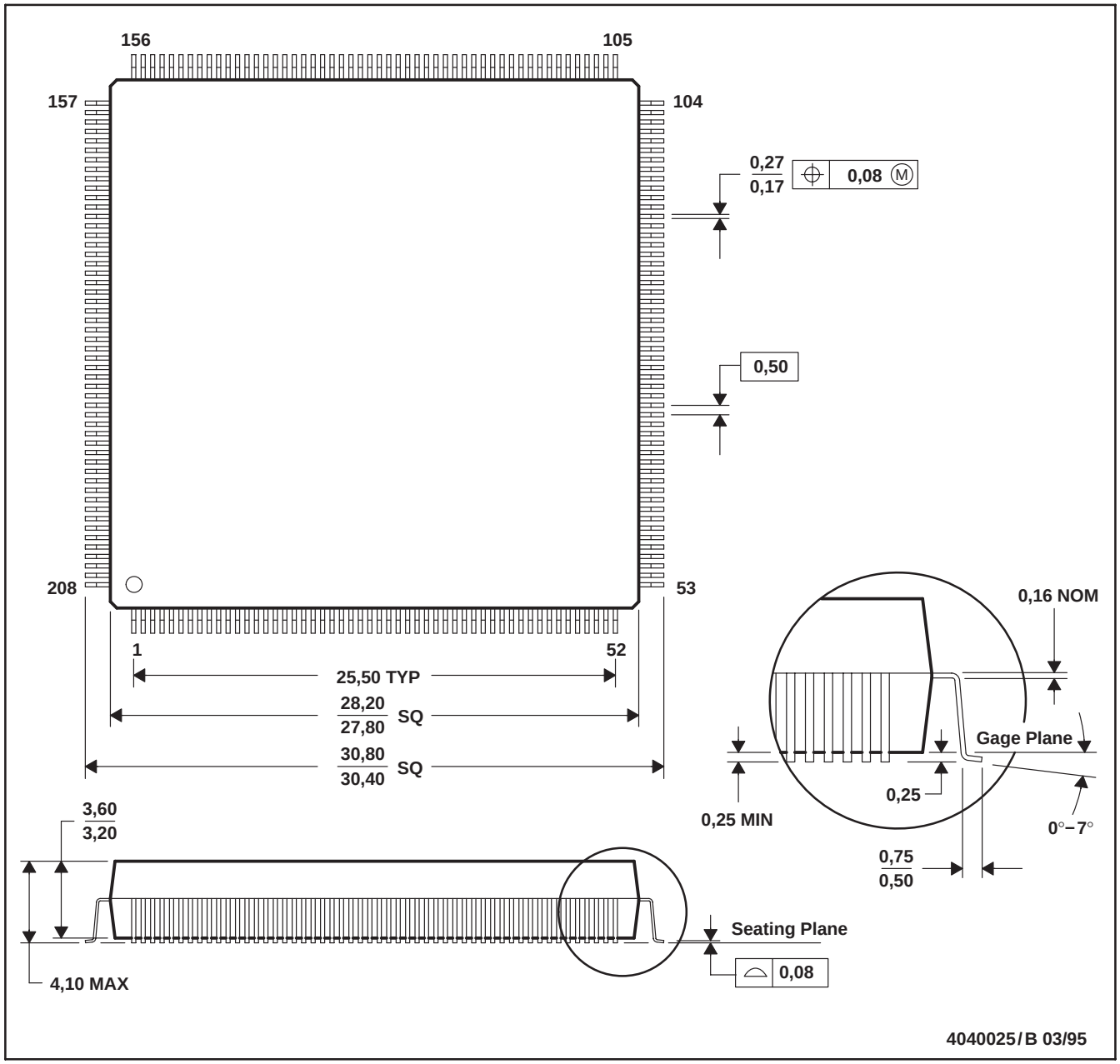
MicroStar BGA is a trademark of Texas Instruments.

PDV (LF-PQFP-G208) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PPM (S-PQFP-G208) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-143

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCI2050BGHK	ACTIVE	BGA	GHK	257	90	TBD	Call TI	Level-3-220C-168 HR
PCI2050BIGHK	ACTIVE	BGA	GHK	257	90	TBD	Call TI	Level-3-220C-168 HR
PCI2050BIPDV	ACTIVE	LQFP	PDV	208	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCI2050BIZHK	ACTIVE	BGA MICROSTAR	ZHK	257	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
PCI2050BPDV	ACTIVE	LQFP	PDV	208	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCI2050BPDVG4	ACTIVE	LQFP	PDV	208	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCI2050BPPM	ACTIVE	QFP	PPM	208	24	TBD	CU	Level-4-220C-72 HR
PCI2050BZHK	ACTIVE	BGA MICROSTAR	ZHK	257	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.