

# FSA2467

## 0.4W Low Voltage Dual SPDT Analog Switch

### General Description

The FSA2467 is a Quad Single Pole Double Throw (SPDT) analog switch. The FSA2467 operates from a single 1.65V to 4.3V supply. The FSA2467 features an ultra-low On Resistance of 0.4W at a +2.7V supply and 25°C. This device is fabricated with sub-micron CMOS technology to achieve fast switching speeds and is designed for break-before-make operation.

FSA2467 features very low quiescent current even when the control voltage is lower than the  $V_{CC}$  supply. This feature services the mobile handset applications very well allowing for the direct interface with baseband processor general purpose I/Os.

### Features

- Typical 0.4W On Resistance ( $R_{ON}$ ) for +2.7V supply
- FSA2467 features less than 12μA  $I_{CCT}$  current when S Input is lower than  $V_{CC}$
- 0.25W maximum  $R_{ON}$  flatness for +2.7V supply
- 3x3mm 16-lead Pb-Free MLP package
- Broad  $V_{CC}$  operating range
- Low THD (0.02% typical for 32W load)

### Applications

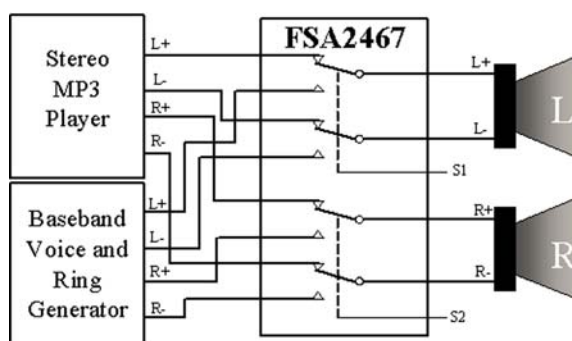
- Cell Phone
- PDA
- Portable Media Player

### Ordering Code:

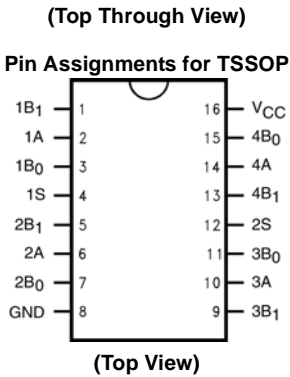
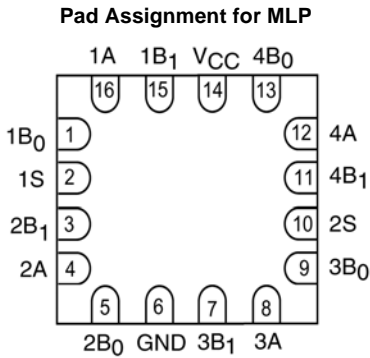
Order Number	Package Number	Package Description
FSA2467MPX	MLP16B	Pb-Free 16-Terminal Molded Leadless Package (MLP) Quad, JEDEC MO-220, 3mm Square
FSA2467MTC (Preliminary)	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Pb-Free package per JEDEC J-STD-020B.

### Application Diagram



Connection Diagrams



Truth Table

Control Input(s)	Function
L	nB <sub>0</sub> Connected to nA
H	nB <sub>1</sub> Connected to nA

H = HIGH Logic Level      L = LOW Logic Level

Pin Descriptions

Pin Names	Function
nA, nB <sub>0</sub> , nB <sub>1</sub>	Data Ports
nS	Control Input

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
Switch Voltage ( $V_S$ ) (Note 2)	-0.5V to $V_{CC} + 0.3V$
Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +4.6V
Input Diode Current	-50 mA
Switch Current	350 mA
Peak Switch Current (Pulsed at 1 ms duration, <10% Duty Cycle)	500 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	+150°C
Lead Temperature ( $T_L$ )	
Soldering, 10 seconds	+260°C
ESD	
Human Body Model	4500V

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	1.65V to 4.3V
Control Input Voltage ( $V_{IN}$ ) (Note 3)	0V to $V_{CC}$
Switch Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 3:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics** (All typical values are @ 25°C unless otherwise specified)

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	Input Voltage High	4.3				1.4		V	
		2.7 to 3.6				1.3			
		2.3 to 2.7				1.1			
		1.65 to 1.95				0.9			
$V_{IL}$	Input Voltage Low	4.3					0.7	V	
		2.7 to 3.6					0.5		
		2.3 to 2.7					0.4		
		1.65 to 1.95					0.4		
$I_{IN}$	Control Input Leakage	1.65 to 4.3				-0.5	0.5	$\mu\text{A}$	$V_{IN} = 0V \text{ to } V_{CC}$
$I_{NO(OFF)}$ , $I_{NC(OFF)}$	OFF-Leakage Current of Port $nB_0$ and $nB_1$	1.95 to 4.3	-10.0		10.0	-50.0	50.0	nA	$nA = 0.3V$ , $V_{CC} - 0.3V$ $nB_0$ or $nB_1 = 0.3V$ , $V_{CC} - 0.3V$ or Floating
$I_{A(ON)}$	ON Leakage Current of Port A	1.95 to 4.3	-10.0		10.0	-50.0	50.0	nA	$nA = 0.3V$ , $V_{CC} - 0.3V$ $nB_0$ or $nB_1 = 0.3V$ , $V_{CC} - 0.3V$ or Floating
$R_{ON}$	Switch On Resistance (Note 4)	4.3		0.4			0.6	W	$I_{OUT} = 100 \text{ mA}$ , $nB_0$ or $nB_1 = 0V$ , 0.8V, 1.8V, 2.7V
		2.7		0.4			0.6		
		2.3		0.55			0.95		
		1.8		0.8			2.0		
$\Delta R_{ON}$	On Resistance Matching Between Channels (Note 5)	2.7		0.04			0.1	W	$I_{OUT} = 100 \text{ mA}$ , $nB_0$ or $nB_1 = 0.8V$
		2.3		0.03			0.1		$I_{OUT} = 100 \text{ mA}$ , $nB_0$ or $nB_1 = 0.7V$
$R_{FLAT(ON)}$	On Resistance Flatness (Note 6)	2.7					0.25	W	$I_{OUT} = 100 \text{ mA}$ , $nB_0$ or $nB_1 = 0V \text{ to } V_{CC}$
		2.3					0.3		
$I_{CC}$	Quiescent Supply Current	4.3	-100		100	-500	500	nA	$V_{IN} = 0V \text{ or } V_{CC}$ , $I_{OUT} = 0V$
$I_{CCT}$	Quiescent Supply Current	4.3		7.0	12.0		15.0	$\mu\text{A}$	$V_{IN} = 1.8$
				3.0	6.0		7.0		$V_{IN} = 2.6$

**Note 4:** On Resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.

**Note 5:**  $\Delta R_{ON} = R_{ONmax} - R_{ONmin}$  measured at identical  $V_{CC}$ , temperature, and voltage.

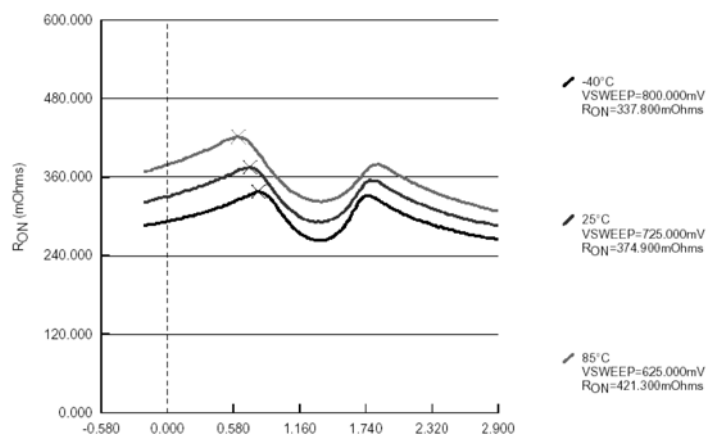
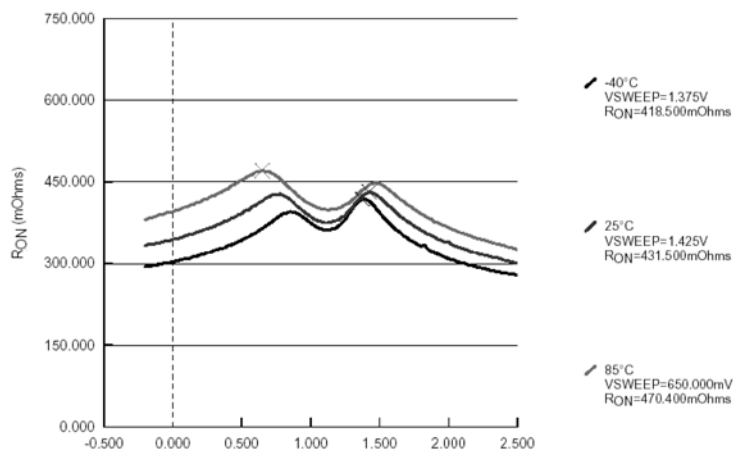
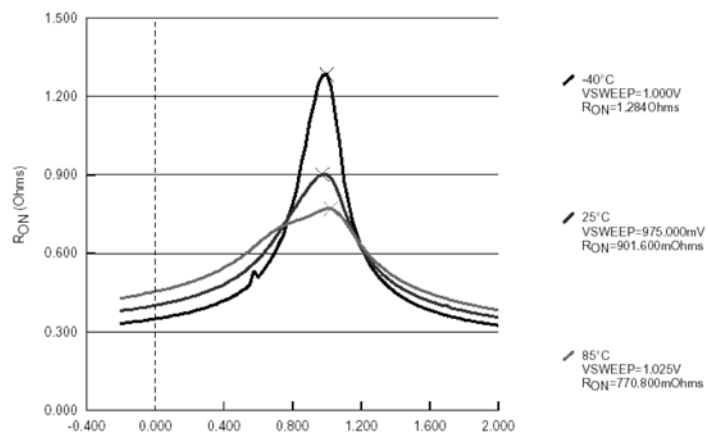
**Note 6:** Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

## AC Electrical Characteristics (All typical value are @ 25°C unless otherwise specified)

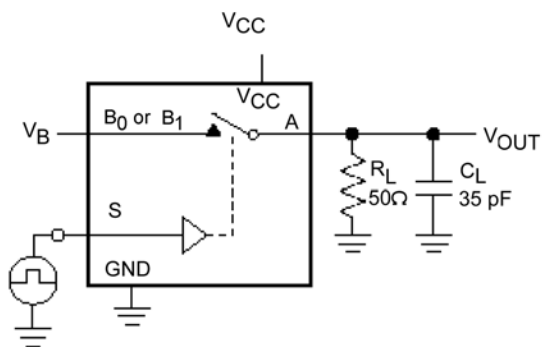
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t <sub>ON</sub>	Turn ON Time	3.6 to 4.3		50.0			60.0	ns	nB <sub>0</sub> or nB <sub>1</sub> = 1.5V, R <sub>L</sub> = 50W, C <sub>L</sub> = 35 pF	Figure 4
		2.7 to 3.6		65.0			75.0			
		2.3 to 2.7		80.0			90.0			
t <sub>OFF</sub>	Turn OFF Time	3.6 to 4.3		32.0			40.0	ns	nB <sub>0</sub> or nB <sub>1</sub> = 1.5V, R <sub>L</sub> = 50W, C <sub>L</sub> = 35 pF	Figure 4
		2.7 to 3.6		42.0			50.0			
		2.3 to 2.7		52.0			60.0			
t <sub>B-M</sub>	Break-Before-Make Time	3.6 to 4.3		12.0				ns	nB <sub>0</sub> or nB <sub>1</sub> = 1.5V, R <sub>L</sub> = 50W, C <sub>L</sub> = 35 pF	Figure 5
		2.7 to 3.6		15.0						
		2.3 to 2.7		20.0						
Q	Charge Injection	3.6 to 4.3		15.0				pC	C <sub>L</sub> = 100 pF, V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0W	Figure 7
		2.7 to 3.6		10.0					C <sub>L</sub> = 100 pF, V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0W	
		2.3 to 2.7		8.0					C <sub>L</sub> = 100 pF, V <sub>GEN</sub> = 0V, R <sub>GEN</sub> = 0W	
OIRR	OFF-Isolation	3.6 to 4.3		-75.0				dB	f = 100kHz, R <sub>L</sub> = 50W, C <sub>L</sub> = 5 pF (Stray)	Figure 6
		2.7 to 3.6		-75.0						
		2.3 to 2.7		-75.0						
Xtalk	Crosstalk	3.6 to 4.3		-75.0				dB	f = 100kHz, R <sub>L</sub> = 50W, C <sub>L</sub> = 5 pF (Stray)	Figure 6
		2.7 to 3.6		-75.0						
		2.3 to 2.7		-75.0						
BW	-3db Bandwidth	2.3 to 4.3		85.0				MHz	R <sub>L</sub> = 50W	Figure 9
THD	Total Harmonic Distortion	3.6 to 4.3		0.02				%	R <sub>L</sub> = 32W, V <sub>IN</sub> = 2V P.P, f= 20Hz to 20kHz	Figure 10
		2.7 to 3.6		0.02					R <sub>L</sub> = 32W, V <sub>IN</sub> = 1.5V P.P, f= 20Hz to 20kHz	
		2.3 to 2.7		0.02					R <sub>L</sub> = 32W, V <sub>IN</sub> = 1.2V P.P, f= 20Hz to 20kHz	

## Capacitance

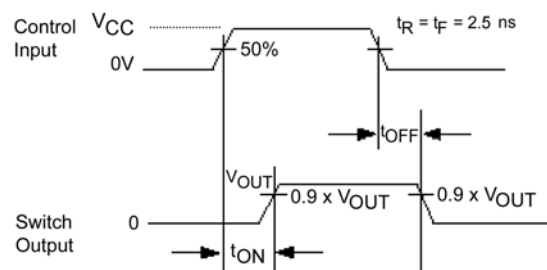
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = 40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
C <sub>IN</sub>	Control Pin Input Capacitance	0.0		1.5				pF	f = 1MHz (see Figure 8)
C <sub>OFF</sub>	B Port OFF Capacitance	3.3		32.0				pF	f = 1MHz (see Figure 8)
C <sub>ON</sub>	A Port ON Capacitance	3.3		118				pF	f = 1MHz (see Figure 8)

FIGURE 1.  $R_{ON}$  at 2.7V  $V_{CC}$ FIGURE 2.  $R_{ON}$  at 2.3V  $V_{CC}$ FIGURE 3.  $R_{ON}$  at 1.8V  $V_{CC}$

## AC Loading and Waveforms

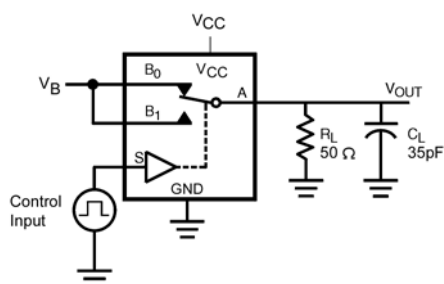


$C_L$  includes Fixture and Stray Capacitance



Logic Input Waveforms Inverted for Switches that have the Opposite Logic Sense

FIGURE 4. Turn-On/Turn-Off Timing



$C_L$  Includes Fixture and Stray Capacitance

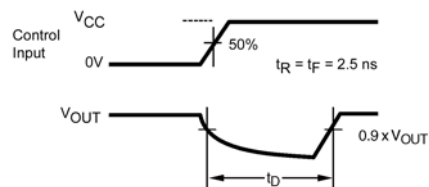
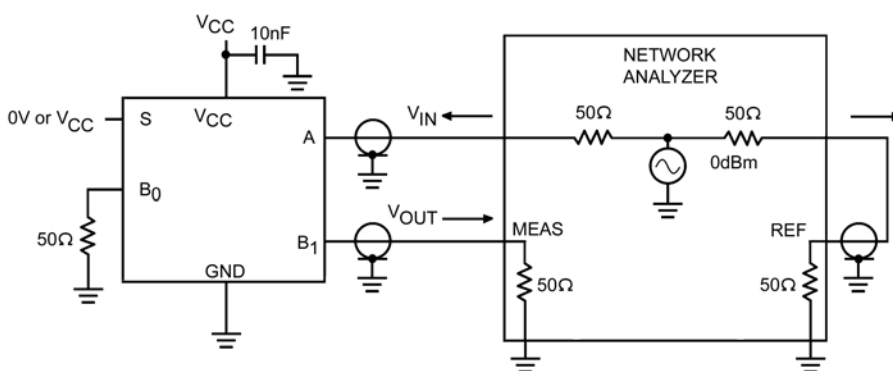


FIGURE 5. Break-Before-Make Timing



$$\begin{aligned} \text{OFF-ISOLATION} &= 20 \log \frac{V_{OUT}}{V_{IN}} \\ \text{ON-LOSS} &= 20 \log \frac{V_{OUT}}{V_{IN}} \\ \text{CROSSTALK} &= 20 \log \frac{V_{OUT}}{V_{IN}} \end{aligned}$$

FIGURE 6. OFF Isolation and Crosstalk

## AC Loading and Waveforms (Continued)

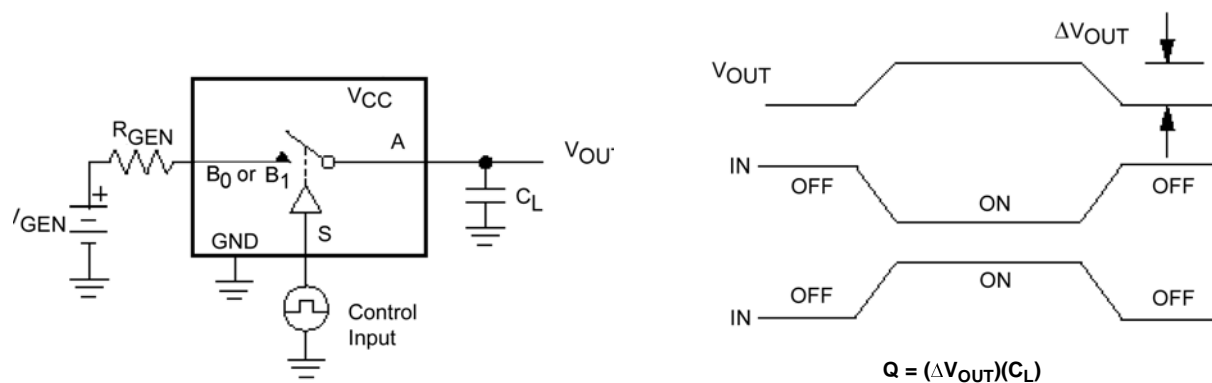


FIGURE 7. Charge Injection

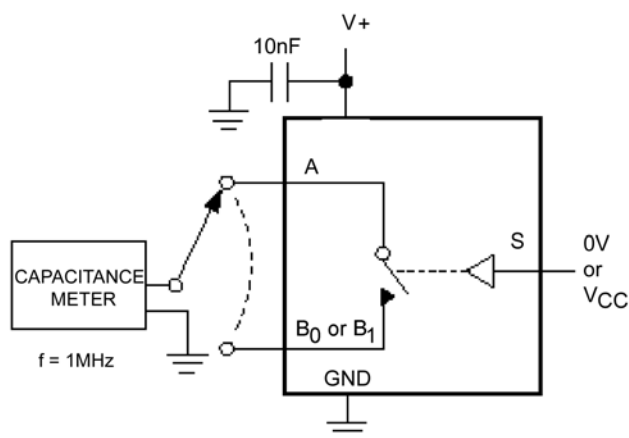


FIGURE 8. ON/OFF Capacitance Measurement Setup

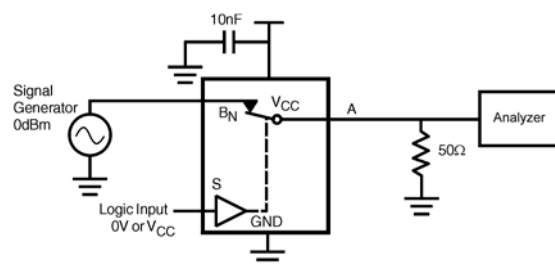


FIGURE 9. Bandwidth

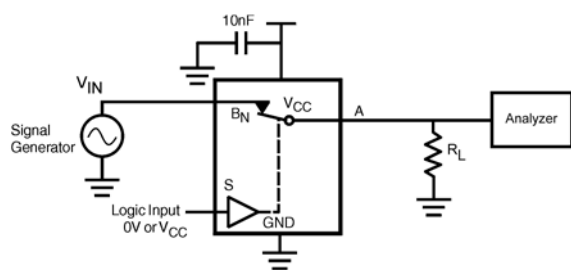
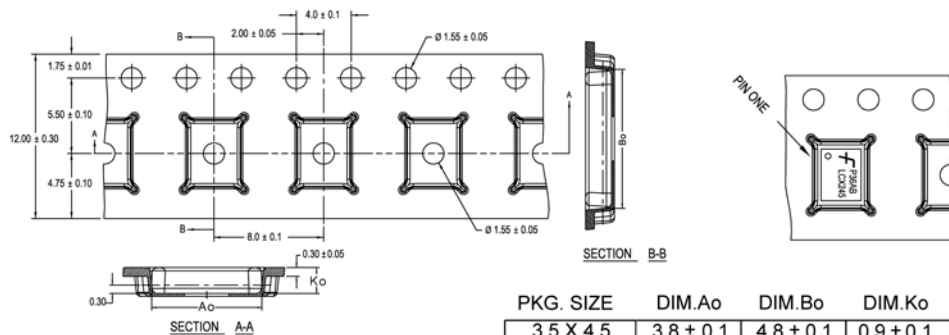


FIGURE 10. Harmonic Distortion

## Tape and Reel Specification

### Tape Format For MLP

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
MPX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

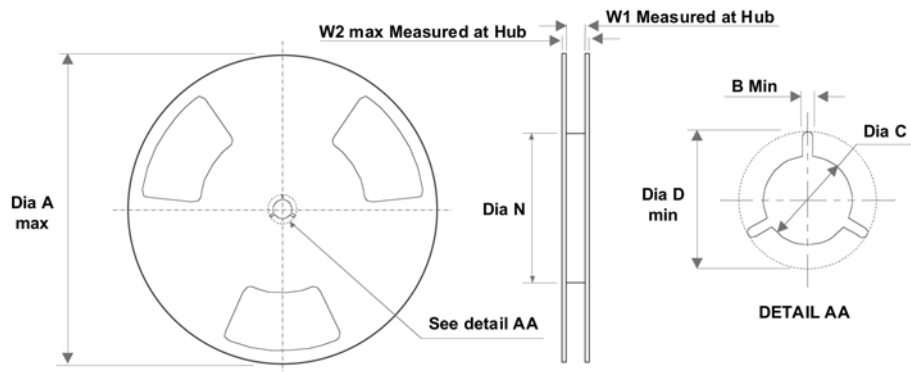


DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is  $\pm 0.002[0.05]$  for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

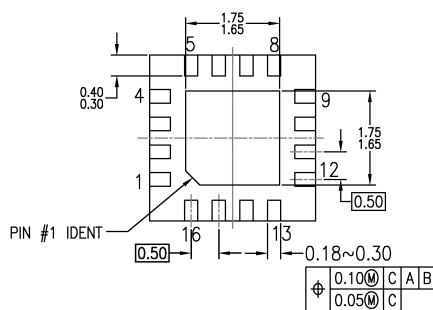
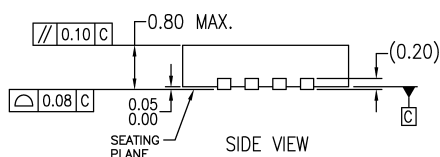
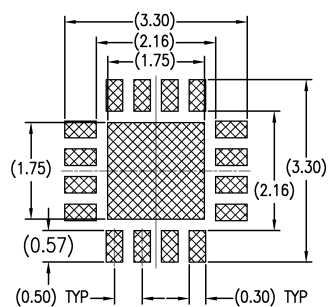
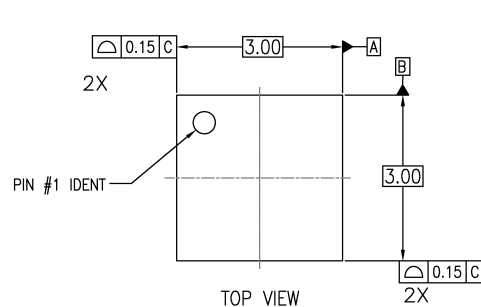
### REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)



# Physical Dimensions inches (millimeters) unless otherwise noted



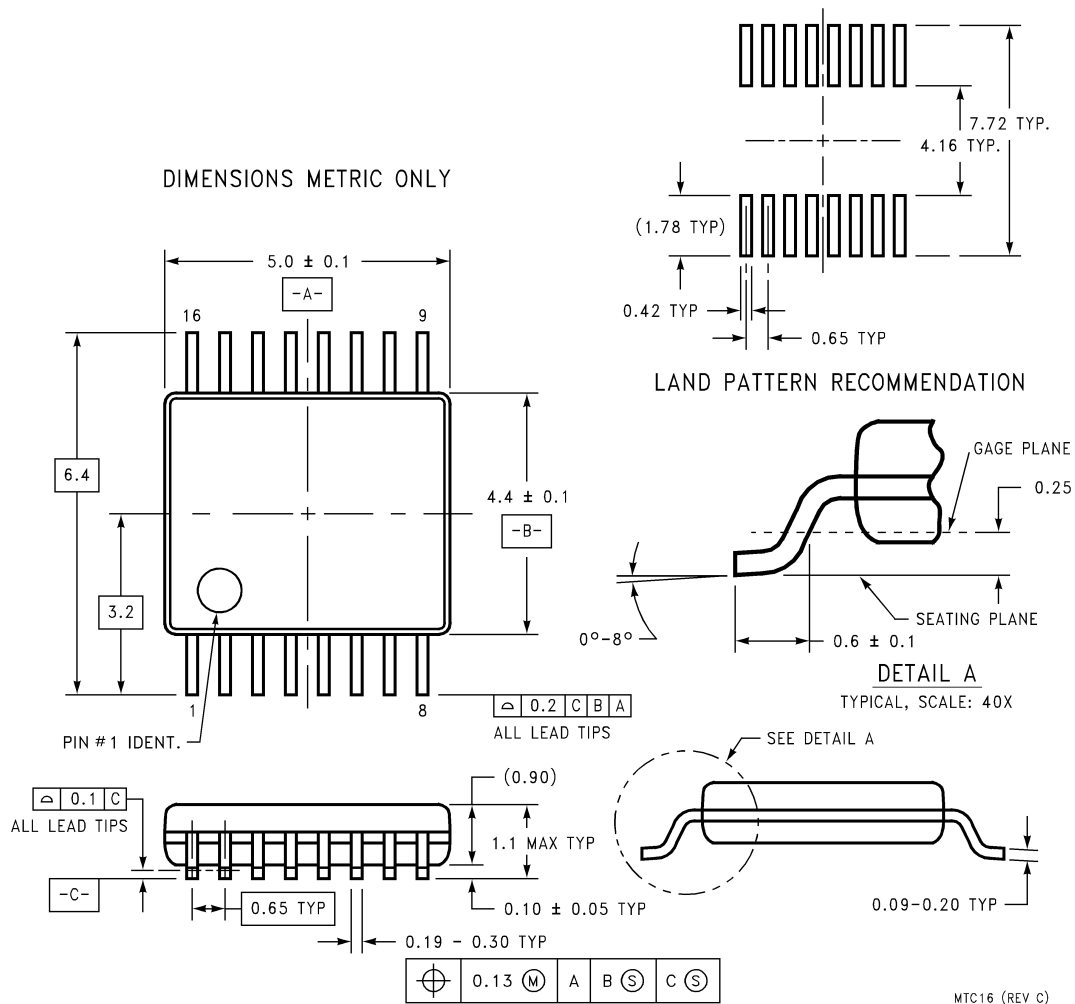
## NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WEED-Pending, DATED pending
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MLP16BrevB

**Pb-Free 16-Terminal Molded Leadless Package (MLP) Quad, JEDEC MO-220, 3mm Square  
Package Number MLP16B**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

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provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

Definition of terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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