

1 A POWER MINI MOLD TRIAC

DESCRIPTION

The AC01DJM is all diffused type TRIAC granted RMS On-state Current 1 Amps, with rated voltages up to 400 volts.

This is designed specifically to be driven by low-level logic in any gating mode.

FEATURES

- The AC01DJM offers sensitive gate specs of 5 and 10 mA, in all for quadrants.
- You can fill the gap between microprocessor controls and the power-output requirements.
- This is housed in the popular SOT-89 package.
- The package features excellent environmental stress and temperature cycling.

QUALITY GRADE

Standard

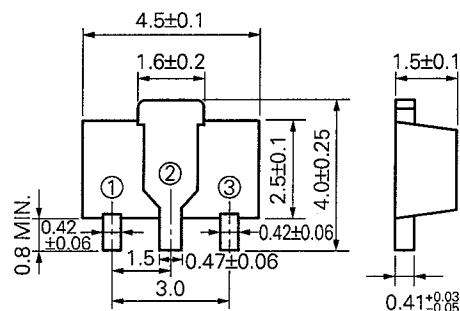
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

APPLICATIONS

Solid-state relays, microprocessor interfacing, TTL logic and various solid-state switch designs alone or with larger TRIAC.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MAXIMUM RATINGS	UNIT	NOTE
Repetitive Peak Off Voltage	V_{DRM}	400	V	
Non-repetitive Peak Off Voltage	V_{DSM}	500	V	
RMS On-State Current	$I_{T(RMS)}$	1 ($T_c = 113^\circ\text{C}$)	A	See Fig. 12
Peak Surge On-State Current	I_{TSM}	7 (50 Hz), 8 (60 Hz)	A	See Fig. 2
Fusing Current	$\int i^2 dt$	0.2 ($1\text{ ms} \leq t \leq 10\text{ ms}$)	A^2s	
Peak Gate Power Dissipation	P_{GM}	1 ($f \geq 50\text{ Hz}$, Duty $\leq 10\%$)	W	
Average Gate Power Dissipation	$P_{G(AV)}$	0.1	W	
Peak Gate Current	I_{GM}	± 0.5 ($f \geq 50\text{ Hz}$, Duty $\leq 10\%$)	A	
Junction Temperature	T_j	125	$^\circ\text{C}$	
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$	

PACKAGE DIMENSIONS
(in millimeters)

Pin Connections

1. T_1 Terminal
2. T_2 Terminal
3. Gate

* Measure point of Case Temperature

ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Peak Off-State Current		I_{DRM}	$V_{DM} = V_{DRM}$	$T_j = 25\text{ }^{\circ}\text{C}$	–	–	10	μA	
				$T_j = 125\text{ }^{\circ}\text{C}$	–	–	100		
On-State Voltage		V_{TM}	$I_{TM} = 1.2\text{ A}$		–	–	1.5	V	See Fig. 1
DC Gate Trigger Current	MODE I	I_{GT}	$V_{DM} = 12\text{ V}$ $R_L = 100\text{ }\Omega$	G; Positive, T_2 ; Positive	–	–	5	mA	See Fig. 5, 7
	II			G; Negative, T_2 ; Positive	–	–	10		
	III			G; Negative, T_2 ; Negative	–	–	5		
	IV			G; Positive, T_2 ; Negative	–	–	5		
DC Gate Trigger Voltage	MODE I	V_{GT}	$V_{DM} = 12\text{ V}$ $R_L = 100\text{ }\Omega$	G; Positive, T_2 ; Positive	–	–	1.0	V	See Fig. 6, 8
	II			G; Negative, T_2 ; Positive	–	–	1.5		
	III			G; Negative, T_2 ; Negative	–	–	1.0		
	IV			G; Positive, T_2 ; Negative	–	–	1.0		
Gate Non-Trigger Voltage		V_{GD}	$T_j = 125\text{ }^{\circ}\text{C}$, $V_{DM} = 1/2 V_{DRM}$		0.1	–	–	V	
DC Holding Current		I_H	$V_D = 24\text{ V}$, $I_{TM} = 1\text{ A}$		–	–	10	mA	
Critical Rate of Rise of Off-State Voltage		dv/dt	$T_j = 125\text{ }^{\circ}\text{C}$, $V_{DM} = 2/3 V_{DRM}$ Gate Open Circuited Exponential Waveform		–	10	–	V/ μs	
Critical Rate of Rise of Commutating Off-State Voltage		$(dv/dt)_c$	$T_j = 125\text{ }^{\circ}\text{C}$, $I_{TM} = 1.2\text{ A}$ $(di_T/dt)_c = -0.5\text{ A/ms}$ $V_{DM} = 400\text{ V}$		0.5	–	–	V/ μs	
Steady State		$R_{th(j-c)}$	Junction to Case		–	–	10	$^{\circ}\text{C/W}$	See Fig. 13
Thermal Resistance		$R_{th(j-a)}$	Junction to Ambient		–	–	120	$^{\circ}\text{C/W}$	

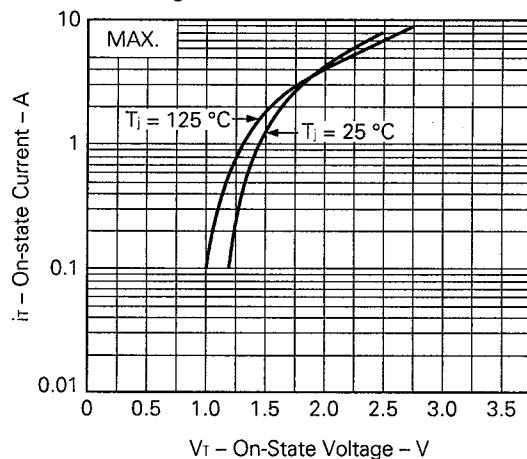
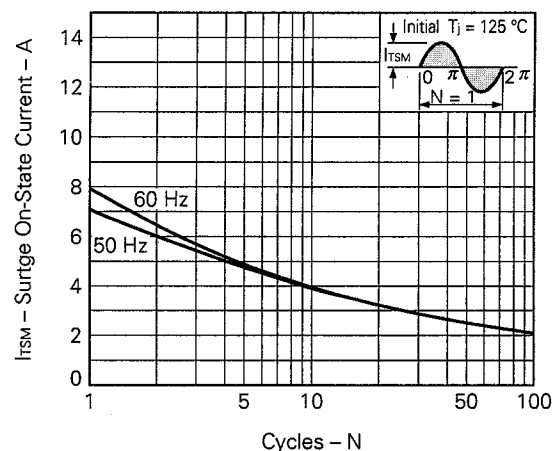
TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)Fig. 1 $i_T - V_T$ CHARACTERISTICFig. 2 I_{TSM} RATING

Fig. 3 $V_G - I_G$ RATING

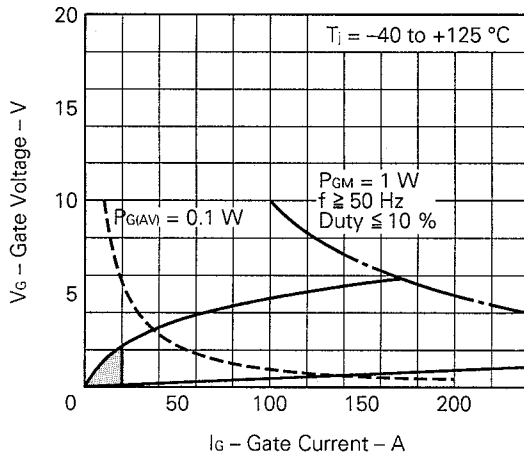


Fig. 4 GATE CHARACTERISTIC

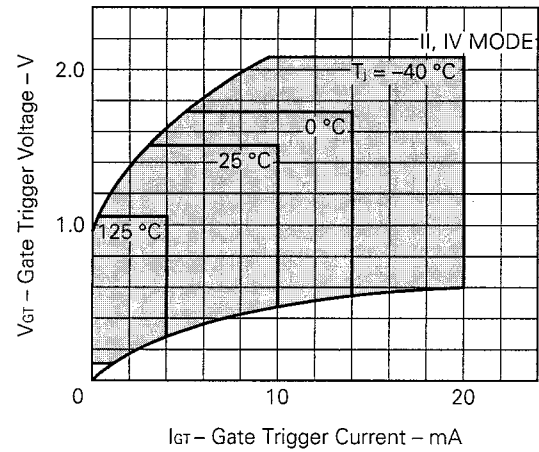


Fig. 5 GATE CHARACTERISTIC

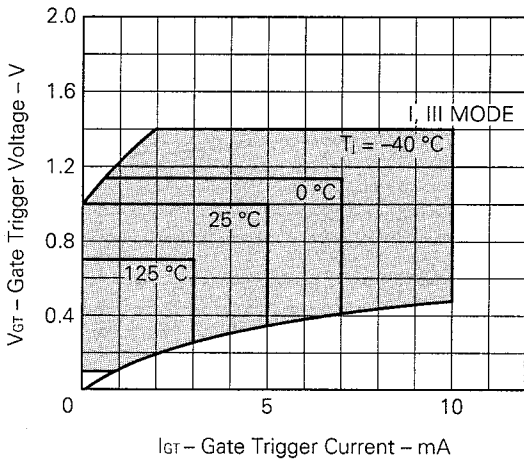


Fig. 6 $I_{GT} - T_a$ TYPICAL DISTRIBUTION

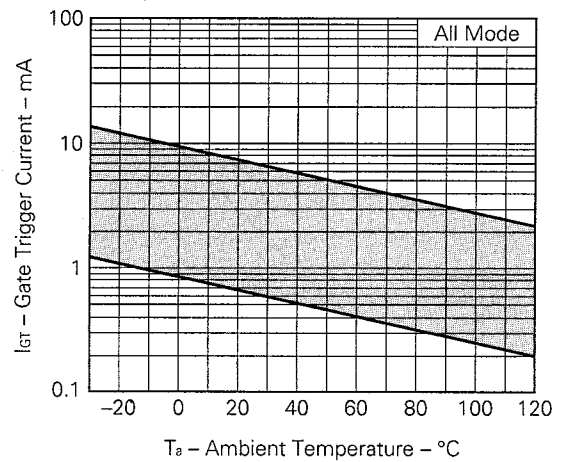


Fig. 7 $V_{GT} - T_a$ TYPICAL DISTRIBUTION

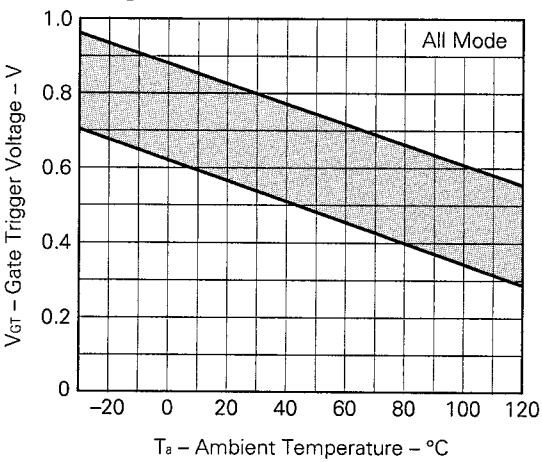


Fig. 8 $i_{GT} - \tau$ TYPICAL DISTRIBUTION

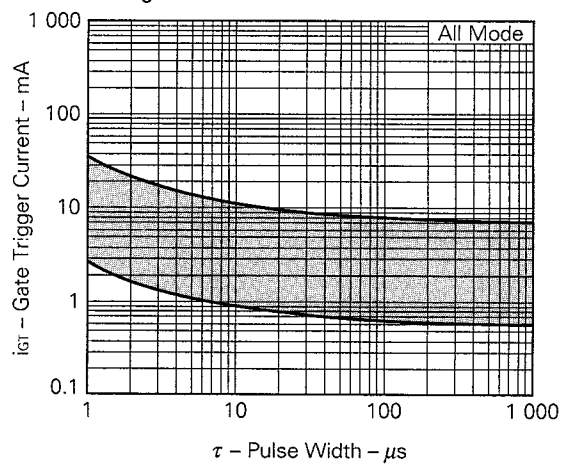


Fig. 9 $V_{GT} - \tau$ TYPICAL DISTRIBUTION

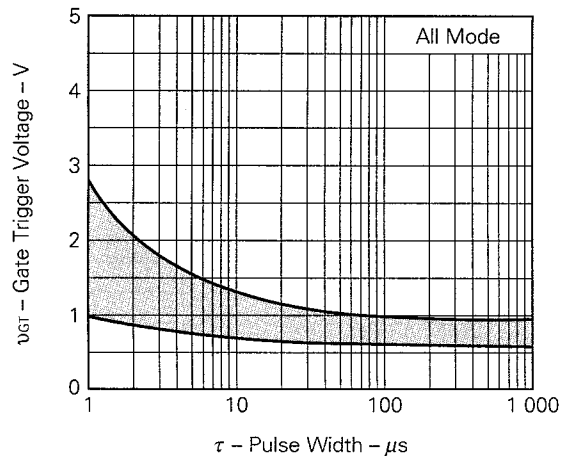


Fig. 10 $I_H - T_a$ TYPICAL DISTRIBUTION

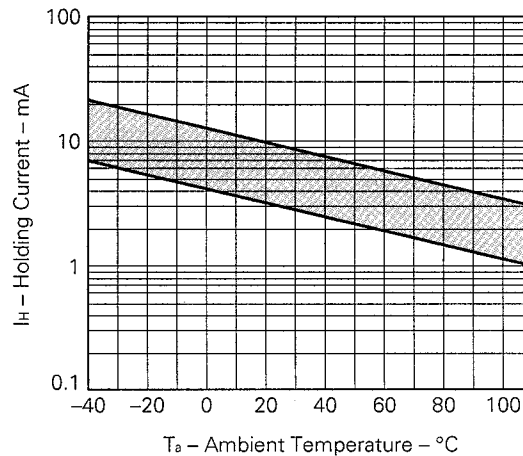


Fig. 11 $P_{T(AV)} - I_{T(RMS)}$ CHARACTERISTIC

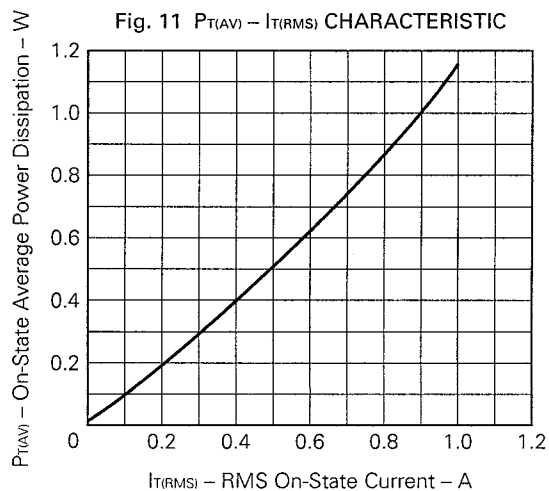


Fig. 12 $T_c - I_{T(RMS)}$ RATING

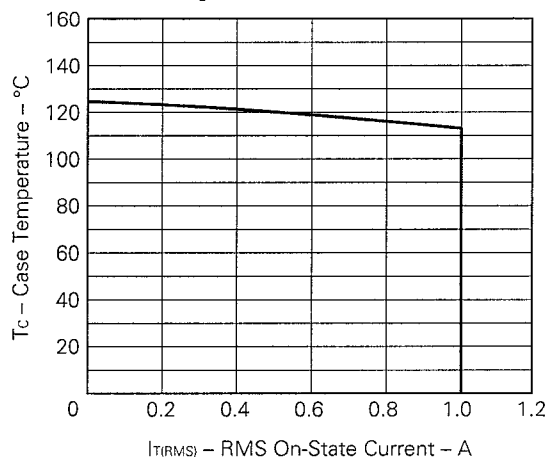


Fig. 13 $T_a - I_{T(RMS)}$ RATING

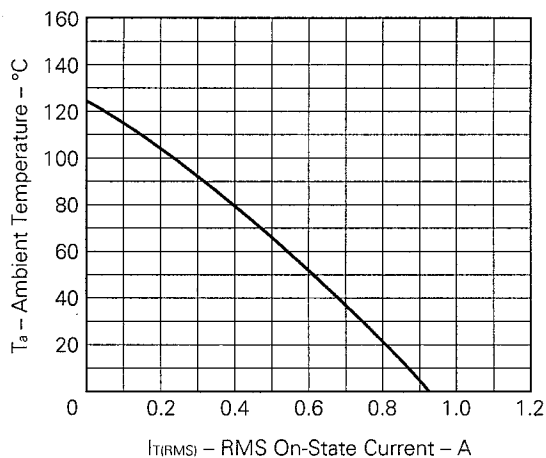
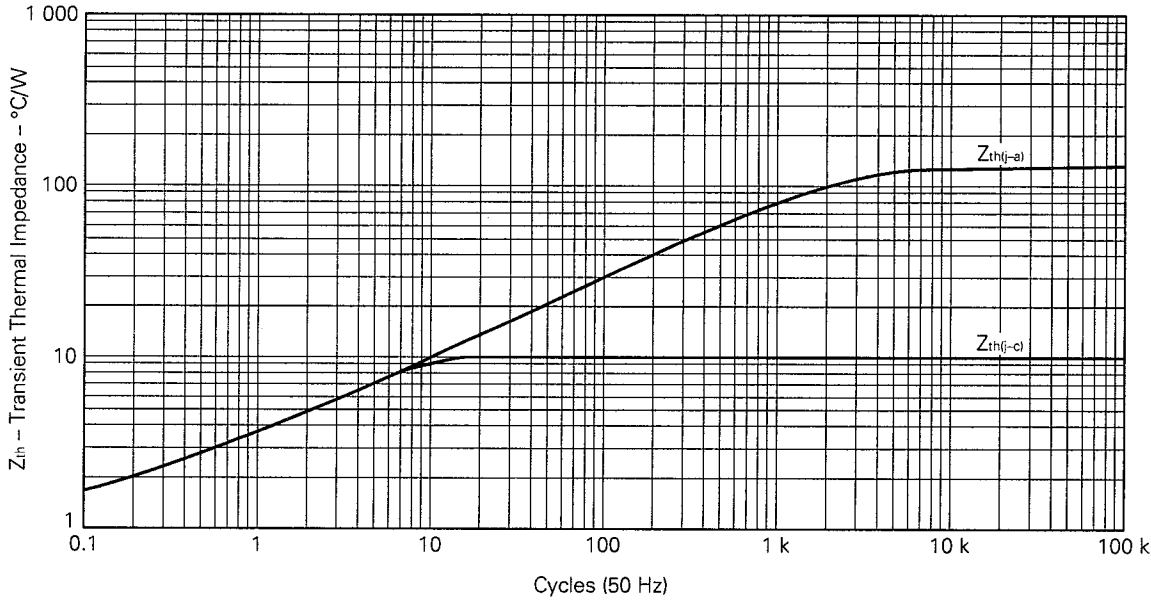


Fig. 14 Z_{th} CHARACTERISTIC



REFERENCE

Document name	Document No.
Quality control guide of semiconductor devices	MEI-1202
Assembly manual of semiconductor devices	IEI-1207

[MEMO]

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