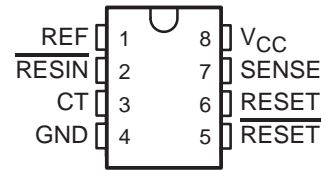


- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Wide Supply-Voltage Range
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- True and Complement Reset Outputs
- Externally Adjustable Pulse Duration

D OR P PACKAGE  
(TOP VIEW)



## description

The TL77xxA family of integrated-circuit supply-voltage supervisors is specifically designed for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the RESET output becomes active (low) when V<sub>CC</sub> attains a value approaching 3.6 V. At this point (assuming that SENSE is above V<sub>IT+</sub>), the delay timer function activates a time delay, after which outputs RESET and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, outputs RESET and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value. The time delay is determined by the value of the external capacitor C<sub>T</sub>:  $t_d = 1.3 \times 10^4 \times C_T$ , where C<sub>T</sub> is in farads (F) and t<sub>d</sub> is in seconds (s).

During power down (assuming that SENSE is below V<sub>IT-</sub>), the outputs remain active until the V<sub>CC</sub> falls below a maximum of 2 V. After this, the outputs are undefined.

An external capacitor (typically 0.1 μF for the TL77xxAC and TL77xxAI) must be connected to REF to reduce the influence of fast transients in the supply voltage.

The TL77xxAC series is characterized for operation from 0°C to 70°C. The TL77xxAI series is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	TL7702ACD	TL7702ACP	TL7702ACY
	TL7705ACD	TL7705ACP	TL7705ACY
	TL7709ACD	TL7709ACP	TL7709ACY
	TL7712ACD	TL7712ACP	TL7712ACY
	TL7715ACD	TL7715ACP	TL7715ACY
–40°C to 85°C	TL7702AID	TL7702AIP	—
	TL7705AID	TL7705AIP	—
	TL7709AID	TL7709AIP	—
	TL7712AID	TL7712AIP	—
	TL7715AID	TL7715AIP	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL7702ACDR). Chip forms are tested at 25°C.



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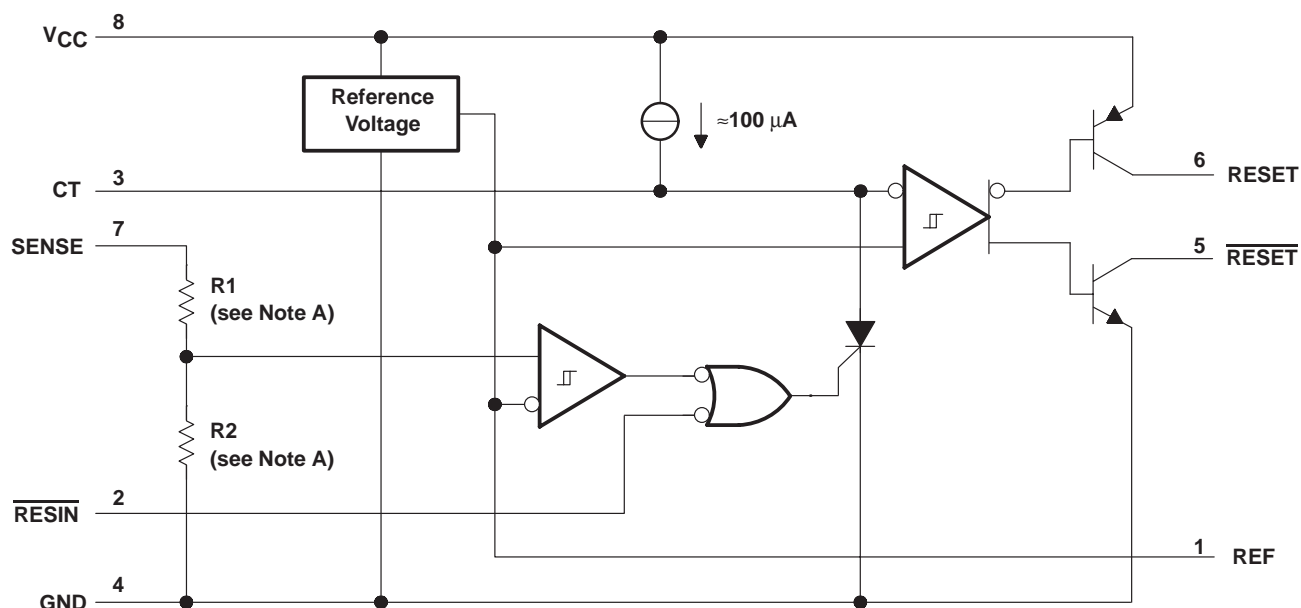
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## TL7702A, TL7705A, TL7709A, TL7712A, TL7715A SUPPLY-VOLTAGE SUPERVISORS

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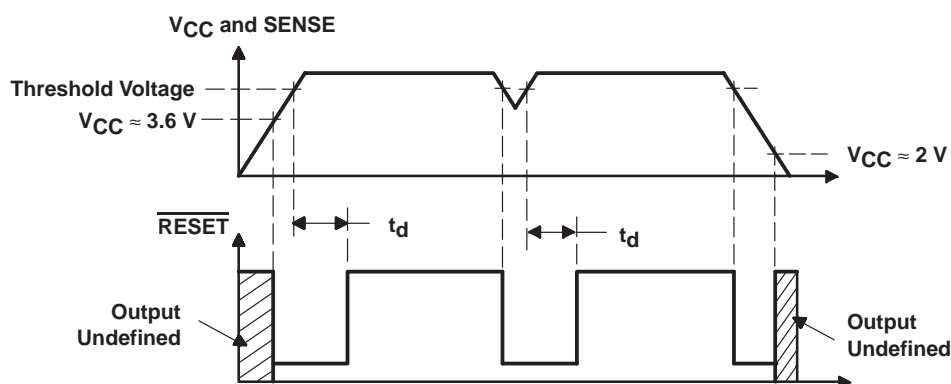
## functional block diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



NOTES: A. TL7702A:  $R_1 = 0\ \Omega$ ,  $R_2 = \text{open}$   
 TL7705A:  $R_1 = 7.8\ \text{k}\Omega$ ,  $R_2 = 10\ \text{k}\Omega$   
 TL7709A:  $R_1 = 19.7\ \text{k}\Omega$ ,  $R_2 = 10\ \text{k}\Omega$   
 TL7712A:  $R_1 = 32.7\ \text{k}\Omega$ ,  $R_2 = 10\ \text{k}\Omega$   
 TL7715A:  $R_1 = 43.4\ \text{k}\Omega$ ,  $R_2 = 10\ \text{k}\Omega$   
 B. Resistor values shown are nominal.

## timing diagram



# TL7702A, TL7705A, TL7709A, TL7712A, TL7715A SUPPLY-VOLTAGE SUPERVISORS

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1)	20 V
Input voltage range, $V_I$ , $\overline{RESIN}$	–0.3 V to 20 V
Input voltage range, $V_I$ , SENSE: TL7702A (see Note 2)	–0.3 V to 6 V
TL7705A	–0.3 V to 20 V
TL7709A	–0.3 V to 20 V
TL7712A, TL7715A	–0.3 V to 20 V
High-level output current, $I_{OH}$ , $\overline{RESET}$	–30 mA
Low-level output current, $I_{OL}$ , $\overline{RESET}$	30 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 3 and 4): D package	97°C/W
P package	127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to the network ground terminal.
  2. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed  $V_{CC} - 1$  V or 6 V, whichever is less.
  3. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
  4. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$		3.5	18	V
High-level input voltage at $\overline{RESIN}$ , $V_{IH}$		2		V
Low-level input voltage at $\overline{RESIN}$ , $V_{IL}$			0.6	V
Input voltage, SENSE, $V_I$	TL7702A	0	See Note 2	V
	TL7705A	0	10	
	TL7709A	0	15	
	TL7712A	0	20	
	TL7715A	0	20	
High-level output current, $\overline{RESET}$ , $I_{OH}$			–16	mA
Low-level output current, $\overline{RESET}$ , $I_{OL}$			16	mA
Timing capacitor, $C_T$			10	μF
Operating free-air temperature range, $T_A$	TL77xxAC	0	70	°C
	TL77xxAI	–40	85	

NOTE 2: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed  $V_{CC} - 1$  V or 6 V, whichever is less.



# TL7702A, TL7705A, TL7709A, TL7712A, TL7715A SUPPLY-VOLTAGE SUPERVISORS

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## electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
V <sub>OH</sub>	High-level output voltage, RESET		I <sub>OH</sub> = −16 mA	V <sub>CC</sub> −1.5			V
V <sub>OL</sub>	Low-level output voltage, RESET		I <sub>OL</sub> = 16 mA	0.4			V
V <sub>ref</sub>	Reference voltage		T <sub>A</sub> = 25°C	2.48	2.53	2.58	V
V <sub>IT−</sub>	Negative-going input threshold voltage, SENSE	TL7702A	T <sub>A</sub> = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11	
		TL7715A		13.2	13.5	13.8	
V <sub>hys</sub>	Hysteresis, SENSE (V <sub>IT+</sub> − V <sub>IT−</sub> )	TL7702A	T <sub>A</sub> = 25°C	10			mV
		TL7705A		15			
		TL7709A		20			
		TL7712A		35			
		TL7715A		45			
I <sub>I</sub>	Input current	RESIN	V <sub>I</sub> = 2.4 V to V <sub>CC</sub>	20			μA
			V <sub>I</sub> = 0.4 V	−100			
	SENSE	TL7702A	V <sub>ref</sub> < V <sub>I</sub> < V <sub>CC</sub> − 1.5 V	0.5    2			
I <sub>OH</sub>	High-level output current, RESET		V <sub>O</sub> = 18 V	50			μA
I <sub>OL</sub>	Low-level output current, RESET		V <sub>O</sub> = 0	−50			μA
I <sub>CC</sub>	Supply current		All inputs and outputs open	1.8    3			mA

† All electrical characteristics are measured with 0.1-μF capacitors connected at REF, CT, and V<sub>CC</sub> to GND.

## switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
Output pulse duration			C <sub>T</sub> = 0.1 μF	0.65	1.2	2.6	μs
Input pulse duration at <u>RESIN</u>				0.4			μs
t <sub>w(S)</sub>	Pulse duration at SENSE input to switch outputs		V <sub>IH</sub> = V <sub>IT–</sub> +200 mV,    V <sub>IL</sub> = V <sub>IT–</sub> –200 mV	2			μs
t <sub>pd</sub>	Propagation delay time, <u>RESIN</u> to <u>RESET</u>		V <sub>CC</sub> = 5 V			1	μs
t <sub>r</sub>	Rise time	<u>RESET</u>	V <sub>CC</sub> = 5 V,                      See Note 5			0.2	μs
		<u>RESET</u>				3.5	
t <sub>f</sub>	Fall time	<u>RESET</u>	V <sub>CC</sub> = 5 V,                      See Note 5			3.5	μs
		<u>RESET</u>				0.2	

‡ All switching characteristics are measured with 0.1-μF capacitors connected at REF and V<sub>CC</sub> to GND.

NOTE 5: The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and RESET.



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# TL7702A, TL7705A, TL7709A, TL7712A, TL7715A SUPPLY-VOLTAGE SUPERVISORS

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**electrical characteristics over recommended operating conditions,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	TL77xxAY			UNIT
			MIN	TYP	MAX	
$V_{\text{ref}}$	Reference voltage			2.53		V
$V_{\text{IT-}}$	Negative-going input threshold voltage, SENSE	TL7702A		2.53		V
		TL7705A		4.55		
		TL7709A		7.6		
		TL7712A		10.8		
		TL7715A		13.5		
$V_{\text{hys}}$	Hysteresis, SENSE ( $V_{\text{IT+}} - V_{\text{IT-}}$ )	TL7702A		10		mV
		TL7705A		15		
		TL7709A		20		
		TL7712A		35		
		TL7715A		45		
$I_{\text{I}}$	Input current, SENSE	TL7702A	$V_{\text{ref}} < V_{\text{I}} < V_{\text{CC}} - 1.5\text{ V}$			$\mu\text{A}$
$I_{\text{CC}}$	Supply current	All inputs and outputs open			1.8	mA

† All electrical characteristics are measured with 0.1- $\mu\text{F}$  capacitors connected at REF, CT, and  $V_{\text{CC}}$  to GND.

**switching characteristics over recommended operating conditions,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS‡	TL77xxAY			UNIT
			MIN	TYP	MAX	
$t_{\text{d}}$	Output pulse time delay	$C_{\text{T}} = 0.1\ \mu\text{F}$		1.2		$\mu\text{s}$

‡ All switching characteristics are measured with 0.1- $\mu\text{F}$  capacitors connected at REF and  $V_{\text{CC}}$  to GND.

# TL7702A, TL7705A, TL7709A, TL7712A, TL7715A SUPPLY-VOLTAGE SUPERVISORS

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## PARAMETER MEASUREMENT INFORMATION

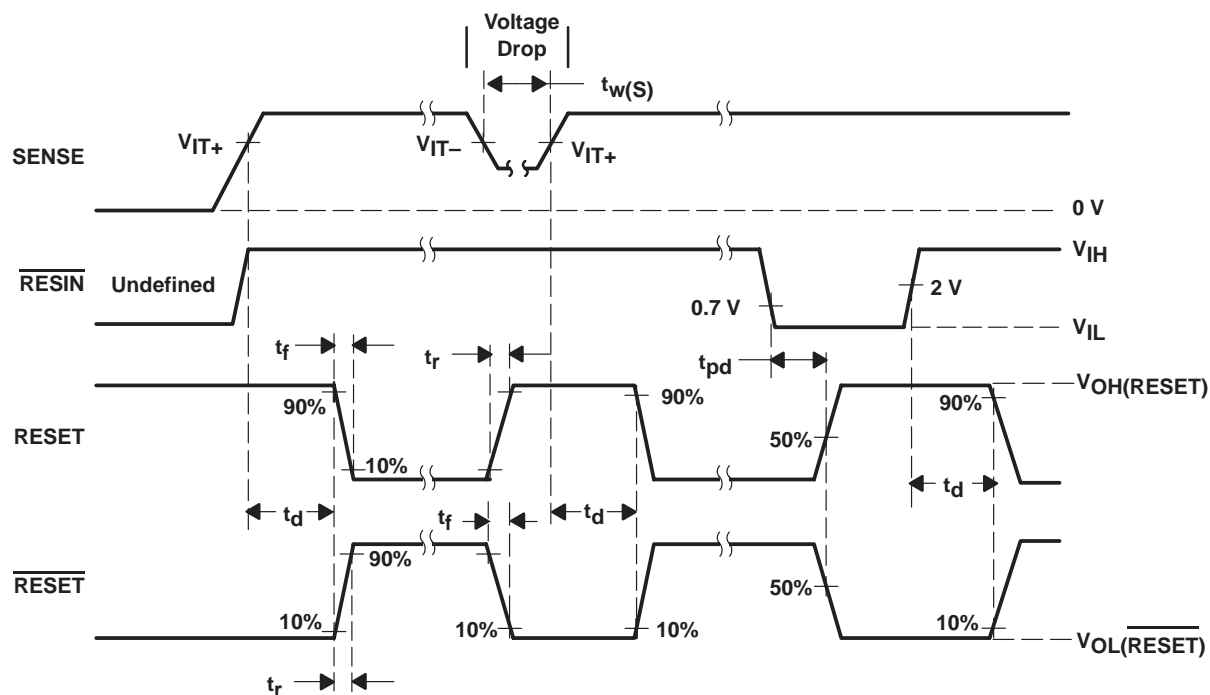


Figure 1. Voltage Waveforms

# TYPICAL CHARACTERISTICS†

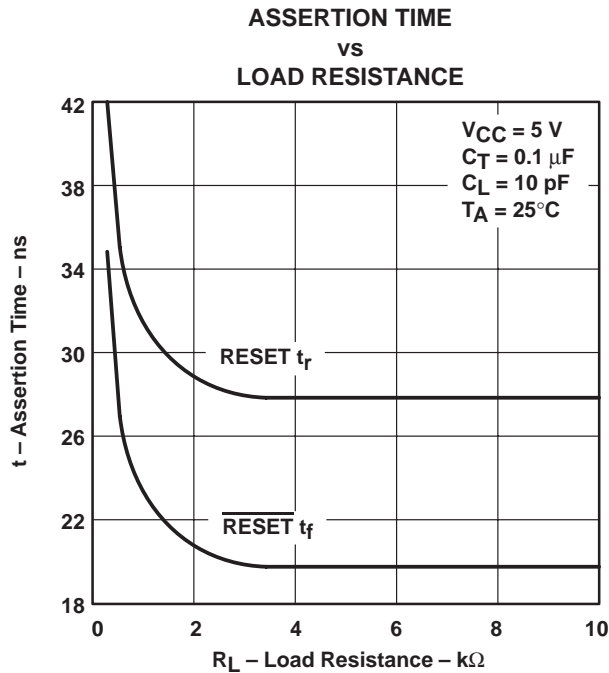


Figure 2

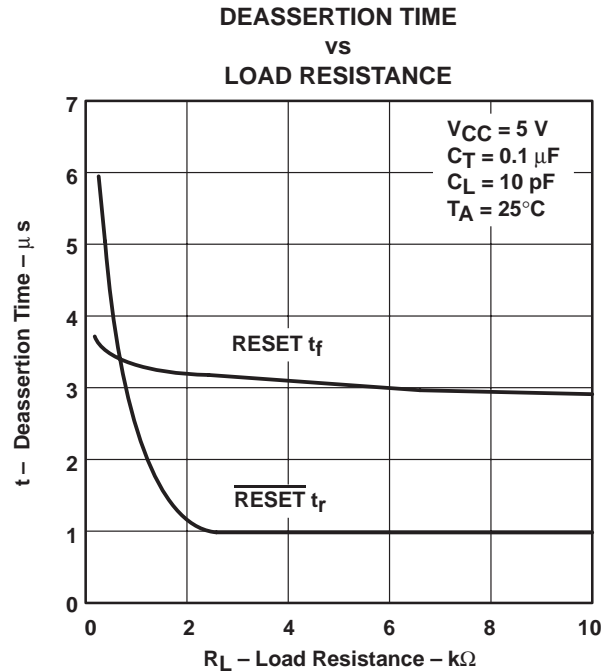


Figure 3

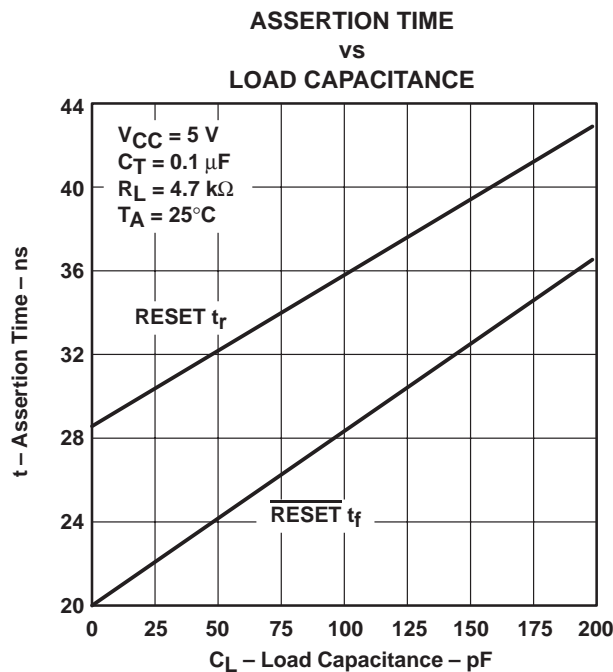


Figure 4

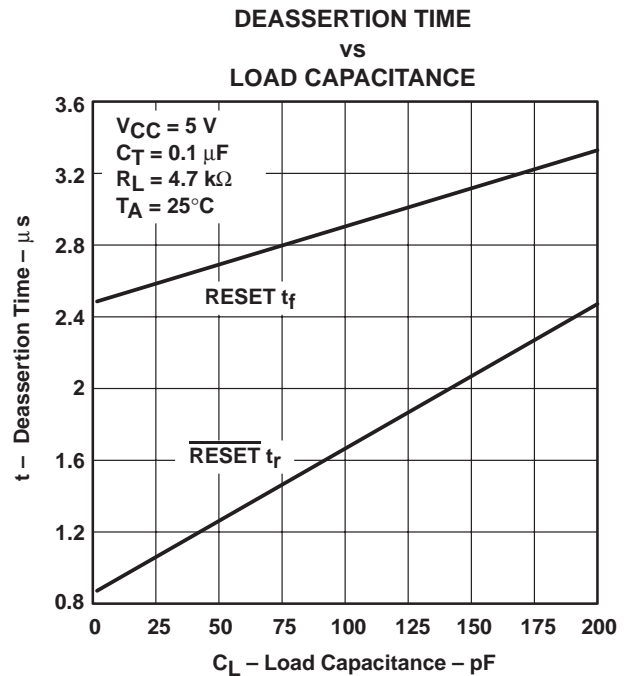


Figure 5

† For proper operation, both RESET and RESET should be terminated with resistors of similar value. Failure to do so may cause unwanted plateauing in either output waveform during switching.

# TL7702A, TL7705A, TL7709A, TL7712A, TL7715A SUPPLY-VOLTAGE SUPERVISORS

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## APPLICATION INFORMATION

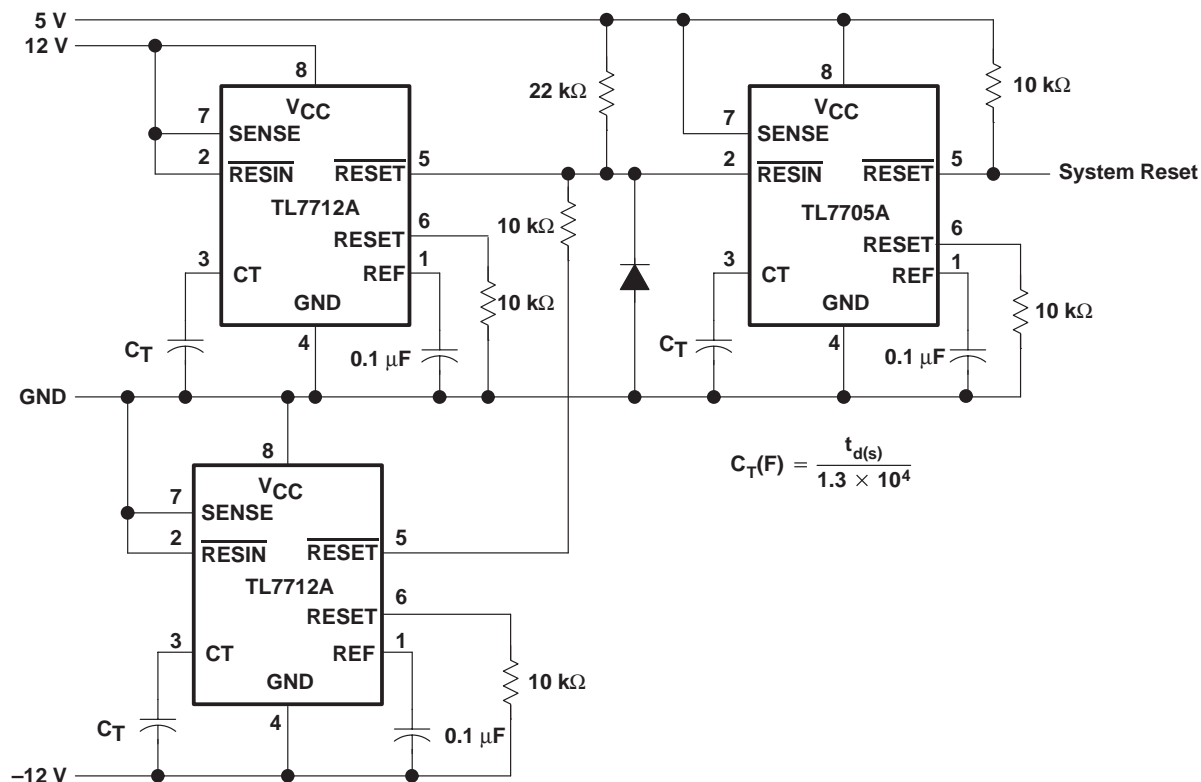


Figure 6. Multiple Power-Supply System Reset Generation

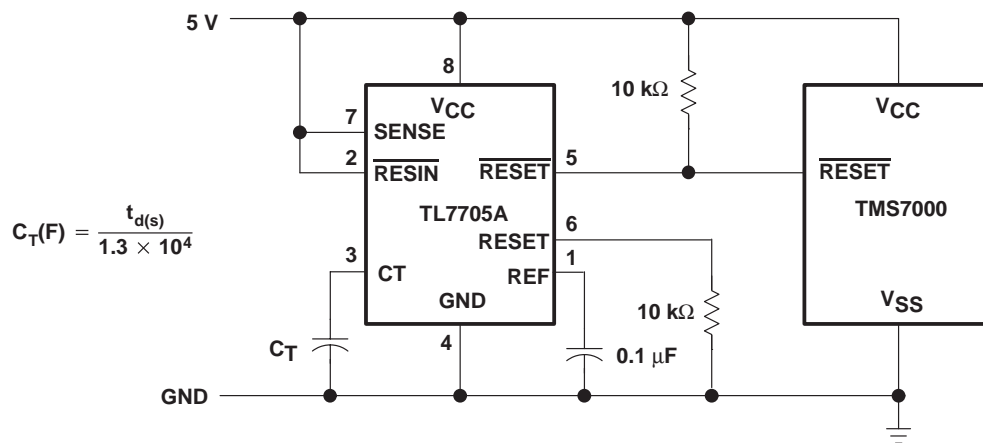


Figure 7. Reset Controller for TMS7000 System



## APPLICATION INFORMATION

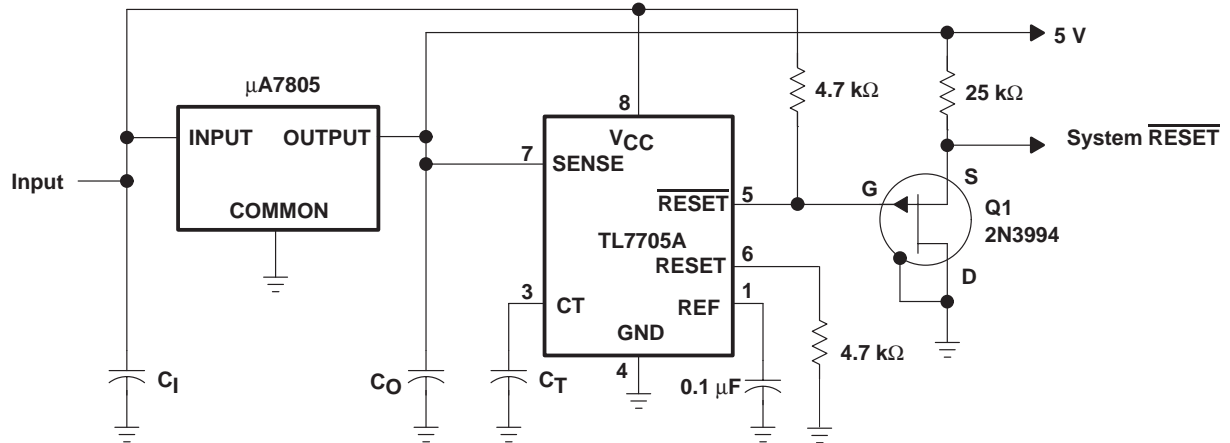


Figure 8. Eliminating Undefined States Using a P-Channel JFET

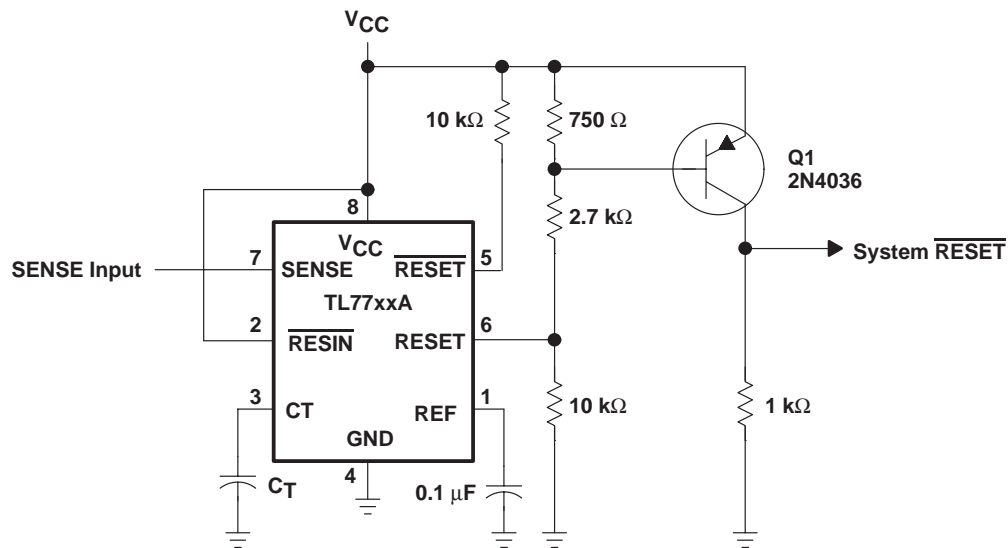


Figure 9. Eliminating Undefined States Using a pnp Transistor

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