



## 2 Megabit (256K x 8) Multi-Purpose Flash SST39SF020

### Preliminary Specifications

#### FEATURES:

- **Organized as 256 K X 8**
- **Single 5.0V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 20 mA (typical)
  - Standby Current: 10  $\mu$ A (typical)
- **Sector Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Time:**
  - 70 and 90 ns
- **Latched Address and Data**
- **Fast Sector Erase and Byte Program:**
  - Sector Erase Time: 7 ms (typical)
  - Chip Erase Time: 15 ms (typical)
  - Byte Program time: 20  $\mu$ s (typical)
  - Chip Rewrite Time: 5 seconds (typical)
- **Automatic Write Timing**
  - Internal  $V_{pp}$  Generation
- **End of Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - EEPROM Pinouts and command set
- **Packages Available**
  - 32-Pin PDIP
  - 32-Pin PLCC
  - 32-Pin TSOP (8mm x 14mm)

#### PRODUCT DESCRIPTION

The SST39SF020 is a 256K x 8 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF020 device writes (Program or Erase) with a 5.0V-only power supply. The SST39SF020 device conforms to JEDEC standard pinouts for x8 memories.

Featuring high performance byte program, the SST39SF020 device provides a maximum byte-program time of 30  $\mu$ sec. The entire memory can be erased and programmed byte by byte typically in 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, the SST39SF020 device has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST39SF020 device is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39SF020 device is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST39SF020 device significantly improves performance and reliability, while lowering power

consumption. The SST39SF020 inherently uses less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The SST39SF020 device also improves flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of endurance cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose erase and program times increase with accumulated endurance cycles.

To meet high density, surface mount requirements, the SST39SF020 device is offered in 32-pin TSOP and 32-pin PLCC packages. A 600 mil, 32-pin PDIP is also available. See Figures 1 and 2 for pinouts.

#### Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while





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keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

### Read

The Read operation of the SST39SF020 device is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 3).

### Byte Program Operation

The SST39SF020 device is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 30  $\mu$ s. See Figures 4 and 5 for WE# and CE# controlled Program operation timing diagrams and Figure 14 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

### Sector Erase Operation

The Sector Erase operation allows the system to erase the device on a sector by sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector Erase operation is initiated by executing a six-byte-command load sequence for software data protection with sector erase command (30H) and sector address (SA) in the last bus cycle. The address lines A12-A17 will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The end of Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 8 for timing waveforms. Any commands written during the Sector Erase operation will be ignored.

### Chip-Erase Operation

The SST39SF020 device provides a Chip-Erase operation, which allows the user to erase the entire memory array to the "1's" state. This is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six-byte software data protection command sequence with Chip Erase command (10H) with address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 9 for timing diagram, and Figure 17 for the flowchart. Any commands written during the Chip Erase operation will be ignored.

### Write Operation Status Detection

The SST39SF020 device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits : Data# Polling (DQ<sub>7</sub>) and Toggle Bit (DQ<sub>6</sub>). The end of write detection mode is enabled after the rising edge of WE# which initiates the internal program or erase cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ<sub>7</sub> or DQ<sub>6</sub>. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

### Data# Polling (DQ<sub>7</sub>)

When the SST39SF020 device is in the internal Program operation, any attempt to read DQ<sub>7</sub> will produce the complement of the true data. Once the Program operation is completed, DQ<sub>7</sub> will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ<sub>7</sub> will produce a '0'. Once the internal Erase operation is completed, DQ<sub>7</sub> will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For sector or chip erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Data# Polling timing diagram and Figure 15 for a flowchart.



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#### Toggle Bit (DQ<sub>6</sub>)

During the internal Program or Erase operation, any consecutive attempts to read DQ<sub>6</sub> will produce alternating 0's and 1's, i.e., toggling between 0 and 1. The Toggle Bit will begin with "1". When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Toggle Bit timing diagram and Figure 15 for a flowchart.

#### Data Protection

The SST39SF020 device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

#### Hardware Data Protection

**Noise/Glitch Protection:** A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

**V<sub>CC</sub> Power Up/Down Detection:** The write operation is inhibited when V<sub>CC</sub> is less than 2.5V.

**Write Inhibit Mode:** Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

#### Software Data Protection (SDP)

The SST39SF020 provides the JEDEC approved software data protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent write operations, e.g., during the system power-up

or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST39SF020 device is shipped with the software data protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within TRC.

#### Product Identification

The product identification mode identifies the device as the SST39SF020 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST39SF020 device. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 10 for the software ID entry and read timing diagram and Figure 16 for the ID entry command sequence flowchart.

**TABLE 1: PRODUCT IDENTIFICATION TABLE**

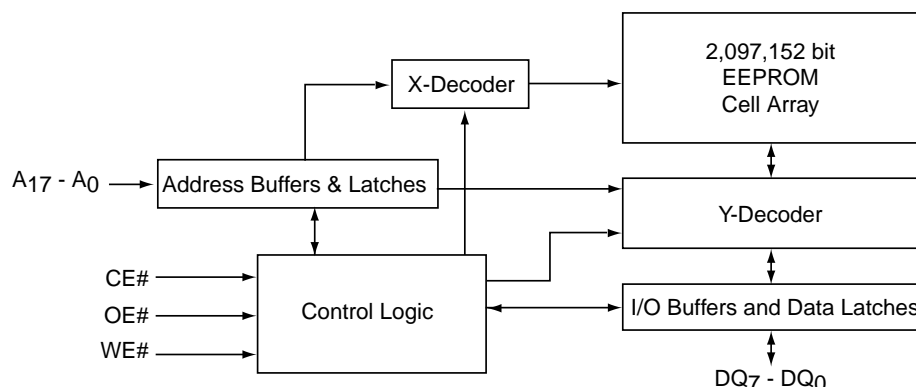
|                     | Address | Data |
|---------------------|---------|------|
| Manufacturer's Code | 0000H   | BF H |
| Device Code         | 0001H   | B6 H |

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#### Product Identification Mode Exit/Reset

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 11 for timing waveform and Figure 16 for a flowchart.

### FUNCTIONAL BLOCK DIAGRAM OF SST39SF020

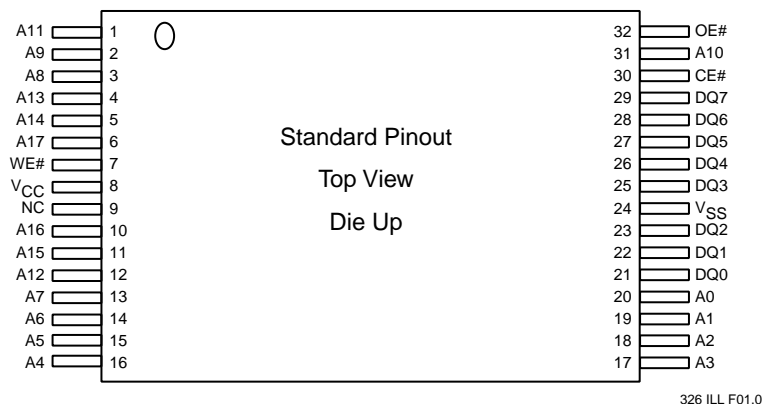


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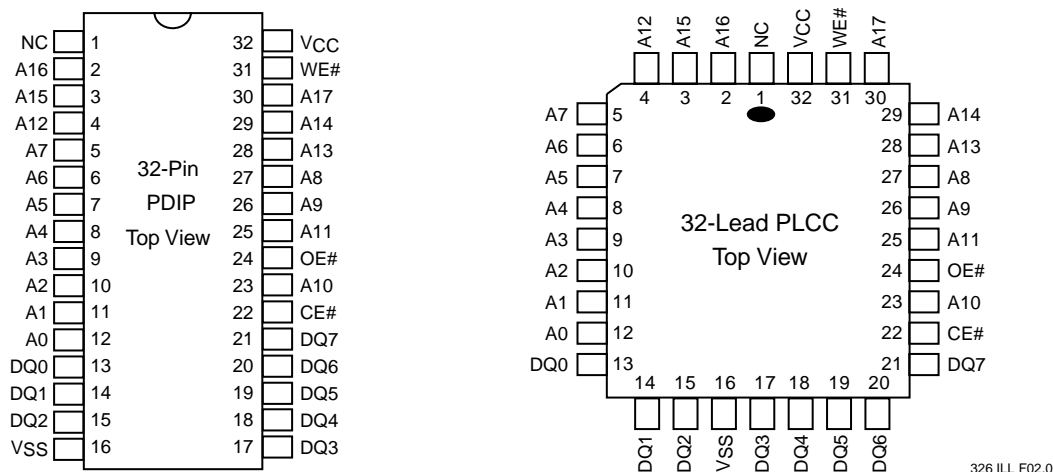


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**FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGES (8mm x 14mm)**



**FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PDIPs AND 32-LEAD PLCCs**



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**TABLE 2: PIN DESCRIPTION**

| Symbol                           | Pin Name          | Functions  |
|----------------------------------|-------------------|--|
| A <sub>17</sub> -A <sub>0</sub>  | Address Inputs    | To provide memory addresses. During sector erase A <sub>17</sub> -A <sub>12</sub> address lines will select the sector.  |
| DQ <sub>7</sub> -DQ <sub>0</sub> | Data Input/output | To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high. |
| CE#                              | Chip Enable       | To activate the device when CE# is low.  |
| OE#                              | Output Enable     | To gate the data output buffers.   |
| WE#                              | Write Enable      | To control the write operations.   |
| V <sub>cc</sub>                  | Power Supply      | To provide 5-volt supply ( $\pm 10\%$ )  |
| V <sub>ss</sub>                  | Ground            |  |
| NC                               | No Connection     | Unconnected pins.  |

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**TABLE 3: OPERATION MODES SELECTION**

| Mode                   | CE#             | OE#             | WE#             | A <sub>9</sub>  | DQ                      | Address   |
|------------------------|-----------------|-----------------|-----------------|-----------------|-------------------------|---|
| Read                   | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | A <sub>IN</sub> | D <sub>OUT</sub>        | A <sub>IN</sub>   |
| Program                | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | A <sub>IN</sub> | D <sub>IN</sub>         | A <sub>IN</sub>   |
| Erase                  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | X               | X                       | Sector address, XXh for chip erase  |
| Standby                | V <sub>IH</sub> | X               | X               | X               | High Z                  | X   |
| Write Inhibit          | X               | V <sub>IL</sub> | X               | X               | High Z/D <sub>OUT</sub> | X   |
|                        | X               | X               | V <sub>IH</sub> | X               | High Z/D <sub>OUT</sub> | X   |
| Product Identification |                 |                 |                 |                 |                         |   |
| Hardware Mode          | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>H</sub>  | Manufacturer Code (BF)  | A <sub>17</sub> - A <sub>1</sub> = V <sub>IL</sub> , A <sub>0</sub> = V <sub>IL</sub> |
|                        |                 |                 |                 |                 | Device Code (B6)        | A <sub>17</sub> - A <sub>1</sub> = V <sub>IL</sub> , A <sub>0</sub> = V <sub>IH</sub> |
| Software Mode          | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | A <sub>IN</sub> | ID Code                 | See Table 4   |

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**TABLE 4: SOFTWARE COMMAND SEQUENCE**

| Command Sequence  | 1st Bus Write Cycle |      | 2nd Bus Write Cycle |      | 3rd Bus Write Cycle |      | 4th Bus Write Cycle |      | 5th Bus Write Cycle |      | 6th Bus Write Cycle            |      |
|-------------------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|--------------------------------|------|
|                   | Addr <sup>(1)</sup> | Data | Addr <sup>(1)</sup> | Data | Addr <sup>(1)</sup> | Data | Addr <sup>(1)</sup> | Data | Addr <sup>(1)</sup> | Data | Addr <sup>(1)</sup>            | Data |
| Byte Program      | 5555H               | AAH  | 2AAAH               | 55H  | 5555H               | A0H  | BA <sup>(3)</sup>   | Data |                     |      |                                |      |
| Sector Erase      | 5555H               | AAH  | 2AAAH               | 55H  | 5555H               | 80H  | 5555H               | AAH  | 2AAAH               | 55H  | SA <sub>x</sub> <sup>(2)</sup> | 30H  |
| Chip Erase        | 5555H               | AAH  | 2AAAH               | 55H  | 5555H               | 80H  | 5555H               | AAH  | 2AAAH               | 55H  | 5555H                          | 10H  |
| Software ID Entry | 5555H               | AAH  | 2AAAH               | 55H  | 5555H               | 90H  |                     |      |                     |      |                                |      |
| Software ID Exit  | XXH                 | F0H  |                     |      |                     |      |                     |      |                     |      |                                |      |
| Software ID Exit  | 5555H               | AAH  | 2AAAH               | 55H  | 5555H               | F0H  |                     |      |                     |      |                                |      |

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**Notes:**

- (1) Address format A<sub>14</sub>-A<sub>0</sub> (Hex), Addresses A<sub>15</sub>, A<sub>16</sub> and A<sub>17</sub> are a "Don't Care" for the Command sequence.
- (2) SA<sub>x</sub> for sector erase; uses A<sub>17</sub>-A<sub>12</sub> address lines
- (3) BA = Program Byte address
- (4) Both Software ID Exit operations are equivalent

**Notes for Software ID Entry Command Sequence**

- 1. With A<sub>17</sub>-A<sub>1</sub>=0; SST Manufacturer Code = BFH, is read with A<sub>0</sub> = 0, SST39SF020 Device Code = B6H, is read with A<sub>0</sub> = 1.
- 2. The device does not remain in Software Product ID Mode if powered down.



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**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

|   |                          |
|---|--------------------------|
| Temperature Under Bias .....                                    | -55°C to +125°C          |
| Storage Temperature .....                                       | -65°C to +150°C          |
| D. C. Voltage on Any Pin to Ground Potential .....              | -0.5V to $V_{CC} + 0.5V$ |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... | -1.0V to $V_{CC} + 1.0V$ |
| Voltage on A <sub>9</sub> Pin to Ground Potential .....         | -0.5V to 14.0V           |
| Package Power Dissipation Capability (Ta = 25°C) .....          | 1.0W                     |
| Through Hole Lead Soldering Temperature (10 Seconds) .....      | 300°C                    |
| Surface Mount Lead Soldering Temperature (3 Seconds) .....      | 240°C                    |
| Output Short Circuit Current <sup>(1)</sup> .....               | 100 mA                   |

**Note:** <sup>(1)</sup> Outputs shorted for no more than one second. No more than one output shorted at a time.

### OPERATING RANGE

| Range      | Ambient Temp     | V <sub>CC</sub> |
|------------|------------------|-----------------|
| Commercial | 0 °C to +70 °C   | 5V±10%          |
| Industrial | -40 °C to +85 °C | 5V±10%          |

### AC CONDITIONS OF TEST

|                            |                                   |
|----------------------------|-----------------------------------|
| Input Rise/Fall Time ..... | 10 ns                             |
| Output Load .....          | C <sub>L</sub> = 100 pF for 90 ns |
| Output Load .....          | C <sub>L</sub> = 30 pF for 70 ns  |
| See Figures 12 and 13      |                                   |





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**TABLE 5: DC OPERATING CHARACTERISTICS  $V_{CC} = 5V \pm 10\%$**

| Symbol                          | Parameter                                    | Limits |      |       | Test Conditions   |
|---------------------------------|--|--------|------|-------|---|
|                                 |  | Min    | Max  | Units |   |
| I <sub>CC</sub>                 | Power Supply Current Read                    |        | 30   | mA    | CE#=OE#=V <sub>IL</sub> , WE#=V <sub>IH</sub> , all I/Os open, Address input = V <sub>IL</sub> /V <sub>IH</sub> , at f=1/T <sub>RC</sub> Min., V <sub>CC</sub> =V <sub>CC</sub> Max |
|                                 | Write  |        | 50   | mA    | CE#=WE#=V <sub>IL</sub> , OE#=V <sub>IH</sub> , V <sub>CC</sub> =V <sub>CC</sub> Max.   |
| I <sub>SB1</sub><br>(TTL input) | Standby V <sub>CC</sub> Current              |        | 3    | mA    | CE#=V <sub>IH</sub> , V <sub>CC</sub> =V <sub>CC</sub> Max.   |
| I <sub>SB2</sub>                | Standby V <sub>CC</sub> Current (CMOS input) |        | 50   | μA    | CE#=V <sub>CC</sub> -0.3V. V <sub>CC</sub> = V <sub>CC</sub> Max.   |
| I <sub>LI</sub>                 | Input Leakage Current                        |        | 1    | μA    | V <sub>IN</sub> =GND to V <sub>CC</sub> , V <sub>CC</sub> = V <sub>CC</sub> Max.  |
| I <sub>LO</sub>                 | Output Leakage Current                       |        | 1    | μA    | V <sub>OUT</sub> =GND to V <sub>CC</sub> , V <sub>CC</sub> = V <sub>CC</sub> Max.   |
| V <sub>IL</sub>                 | Input Low Voltage                            | 2.0    | 0.8  | V     | V <sub>CC</sub> = V <sub>CC</sub> Max.  |
| V <sub>IH</sub>                 | Input High Voltage                           |        |      | V     | V <sub>CC</sub> = V <sub>CC</sub> Max.  |
| V <sub>OL</sub>                 | Output Low Voltage                           |        | 0.4  | V     | I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = V <sub>CC</sub> Min.  |
| V <sub>OH</sub>                 | Output High Voltage                          | 2.4    |      | V     | I <sub>OH</sub> = -400μA, V <sub>CC</sub> = V <sub>CC</sub> Min.  |
| V <sub>H</sub>                  | Supervoltage for A <sub>9</sub> pin          | 11.4   | 12.6 | V     | CE# = OE# =V <sub>IL</sub> , WE# = V <sub>IH</sub>  |
| I <sub>H</sub>                  | Supervoltage Current for A <sub>9</sub> pin  |        | 200  | μA    | CE# = OE# = V <sub>IL</sub> , WE# = V <sub>IH</sub> , A <sub>9</sub> = V <sub>H</sub> Max.  |

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**TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS**

| Symbol                               | Parameter                   | Minimum | Units |
|--------------------------------------|-----------------------------|---------|-------|
| T <sub>PU-READ</sub> <sup>(1)</sup>  | Power-up to Read Operation  | 100     | μs    |
| T <sub>PU-WRITE</sub> <sup>(1)</sup> | Power-up to Write Operation | 100     | μs    |

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**TABLE 7: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)**

| Parameter                       | Description         | Test Condition        | Maximum |
|---------------------------------|---------------------|-----------------------|---------|
| C <sub>I/O</sub> <sup>(1)</sup> | I/O Pin Capacitance | V <sub>I/O</sub> = 0V | 12 pF   |
| C <sub>IN</sub> <sup>(1)</sup>  | Input Capacitance   | V <sub>IN</sub> = 0V  | 6 pF    |

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**Note:** <sup>(1)</sup>This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 8: RELIABILITY CHARACTERISTICS**

| Symbol                              | Parameter                           | Minimum Specification | Units  | Test Method              |
|-------------------------------------|-------------------------------------|-----------------------|--------|--------------------------|
| N <sub>END</sub> <sup>(1)</sup>     | Endurance                           | 10,000                | Cycles | MIL-STD-883, Method 1033 |
| T <sub>DR</sub> <sup>(1)</sup>      | Data Retention                      | 100                   | Years  | JEDEC Standard A103      |
| V <sub>ZAP_HBM</sub> <sup>(1)</sup> | ESD Susceptibility Human Body Model | 1000                  | Volts  | JEDEC Standard A114      |
| V <sub>ZAP_MM</sub> <sup>(1)</sup>  | ESD Susceptibility Machine Model    | 200                   | Volts  | JEDEC Standard A115      |
| I <sub>LTH</sub> <sup>(1)</sup>     | Latch Up                            | 100 + I <sub>CC</sub> | mA     | JEDEC Standard 78        |

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**Note:** <sup>(1)</sup>This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.





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### AC CHARACTERISTICS

**TABLE 9: READ CYCLE TIMING PARAMETERS  $V_{CC} = 4.5-5.5V$**

| Symbol          | Parameter                       | SST39SF020-70 |     | SST39SF020-90 |     | Units |
|-----------------|---------------------------------|---------------|-----|---------------|-----|-------|
|                 |                                 | Min           | Max | Min           | Max |       |
| $T_{RC}$        | Read Cycle time                 | 70            |     | 90            |     | ns    |
| $T_{CE}$        | Chip Enable Access Time         |               | 70  |               | 90  | ns    |
| $T_{AA}$        | Address Access Time             |               | 70  |               | 90  | ns    |
| $T_{OE}$        | Output Enable Access Time       |               | 35  |               | 45  | ns    |
| $T_{CLZ}^{(1)}$ | CE# Low to Active Output        | 0             |     | 0             |     | ns    |
| $T_{OLZ}^{(1)}$ | OE# Low to Active Output        | 0             |     | 0             |     | ns    |
| $T_{CHZ}^{(1)}$ | CE# High to High-Z Output       |               | 15  |               | 20  | ns    |
| $T_{OHZ}^{(1)}$ | OE# High to High-Z Output       |               | 15  |               | 20  | ns    |
| $T_{OH}^{(1)}$  | Output Hold from Address Change | 0             |     | 0             |     | ns    |

Note:  $C_L = 100$  pF for 90 ns,  $C_L = 30$  pF for 70 ns

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**TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS**

| Symbol          | Parameter                        | Min | Max | Units   |
|-----------------|----------------------------------|-----|-----|---------|
| $T_{BP}$        | Byte Program time                |     | 30  | $\mu s$ |
| $T_{AS}$        | Address Setup Time               | 0   |     | ns      |
| $T_{AH}$        | Address Hold Time                | 30  |     | ns      |
| $T_{CS}$        | WE# and CE# Setup Time           | 0   |     | ns      |
| $T_{CH}$        | WE# and CE# Hold Time            | 0   |     | ns      |
| $T_{OES}$       | OE# High Setup Time              | 0   |     | ns      |
| $T_{OEH}$       | OE# High Hold Time               | 0   |     | ns      |
| $T_{CP}$        | CE# Pulse Width                  | 40  |     | ns      |
| $T_{WP}$        | WE# Pulse Width                  | 40  |     | ns      |
| $T_{WPH}^{(1)}$ | WE# Pulse Width High             | 30  |     | ns      |
| $T_{CPH}^{(1)}$ | CE# Pulse Width High             | 30  |     | ns      |
| $T_{DS}$        | Data Setup Time                  | 30  |     | ns      |
| $T_{DH}^{(1)}$  | Data Hold Time                   | 0   |     | ns      |
| $T_{IDA}^{(1)}$ | Software ID Access and Exit Time |     | 150 | ns      |
| $T_{SE}$        | Sector Erase                     |     | 10  | ms      |
| $T_{SCE}$       | Chip Erase                       |     | 20  | ms      |

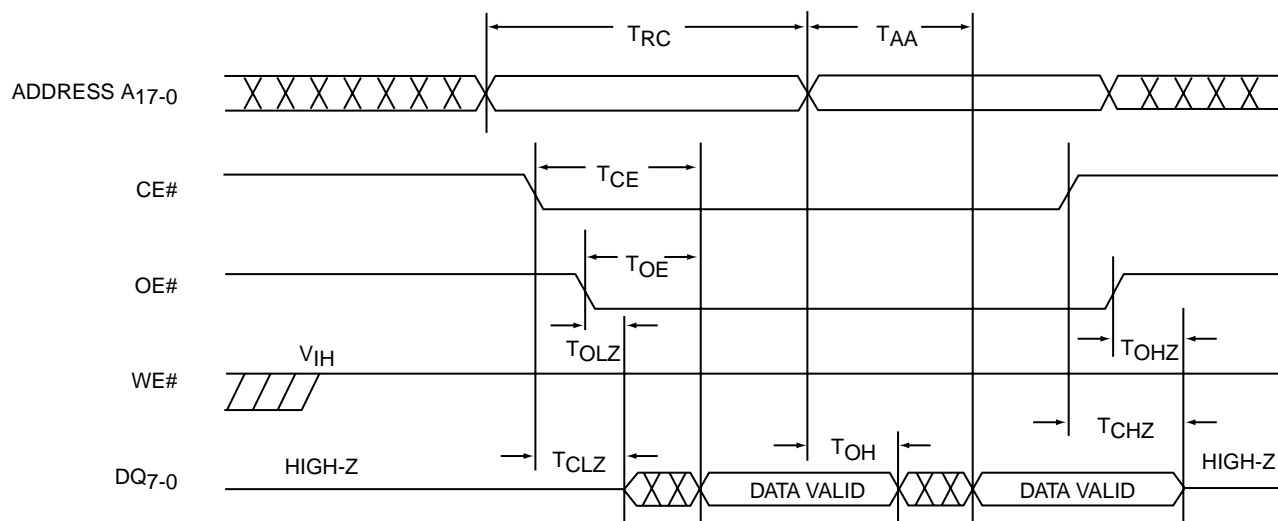
326 PGM T10.4

**Note:** <sup>(1)</sup>This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.



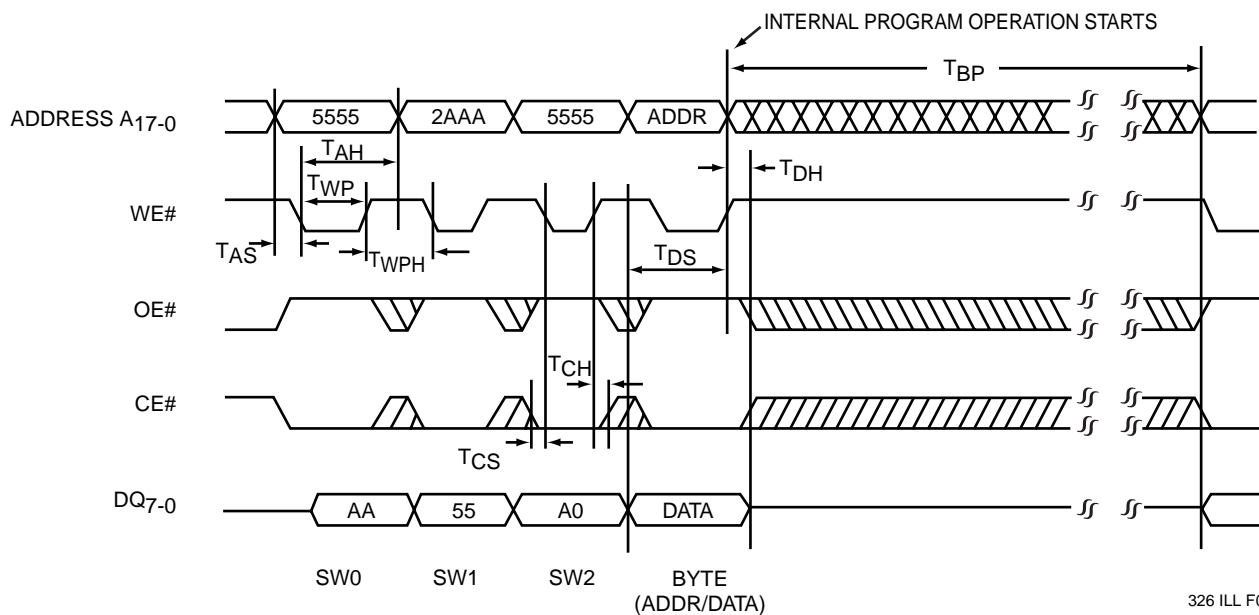
## 2 Megabit Multi-Purpose Flash SST39SF020

Preliminary Specifications



326 ILL F03.0

FIGURE 3: READ CYCLE TIMING DIAGRAM



326 ILL F04.3

FIGURE 4: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

## 2 Megabit Multi-Purpose Flash SST39SF020



Preliminary Specifications

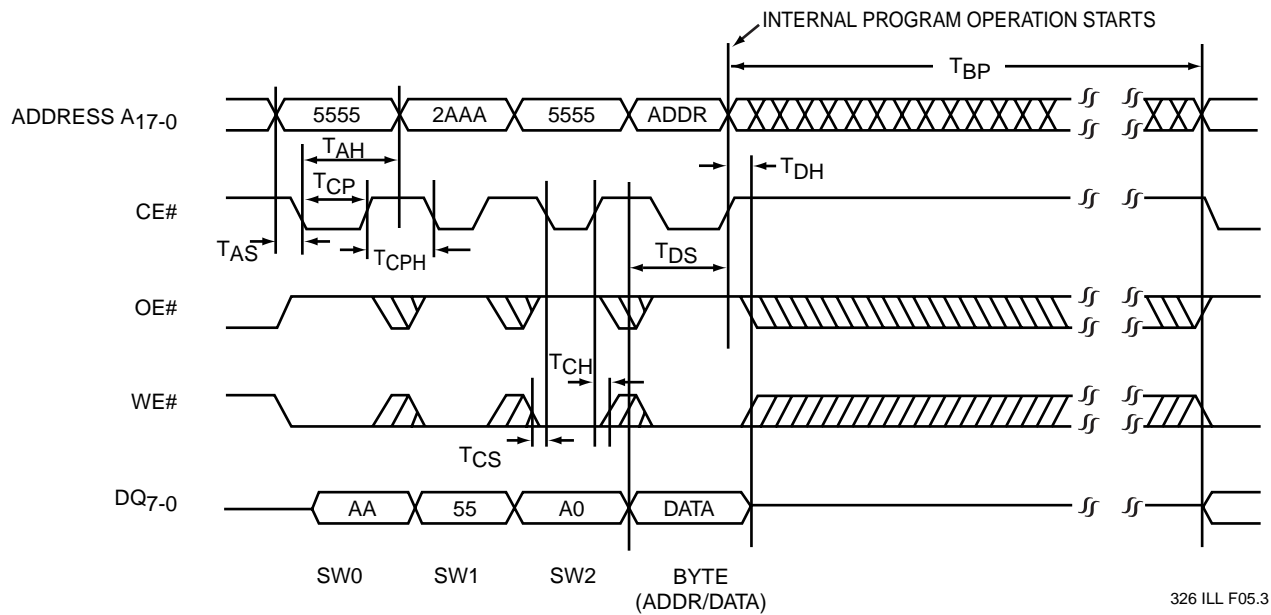


FIGURE 5: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

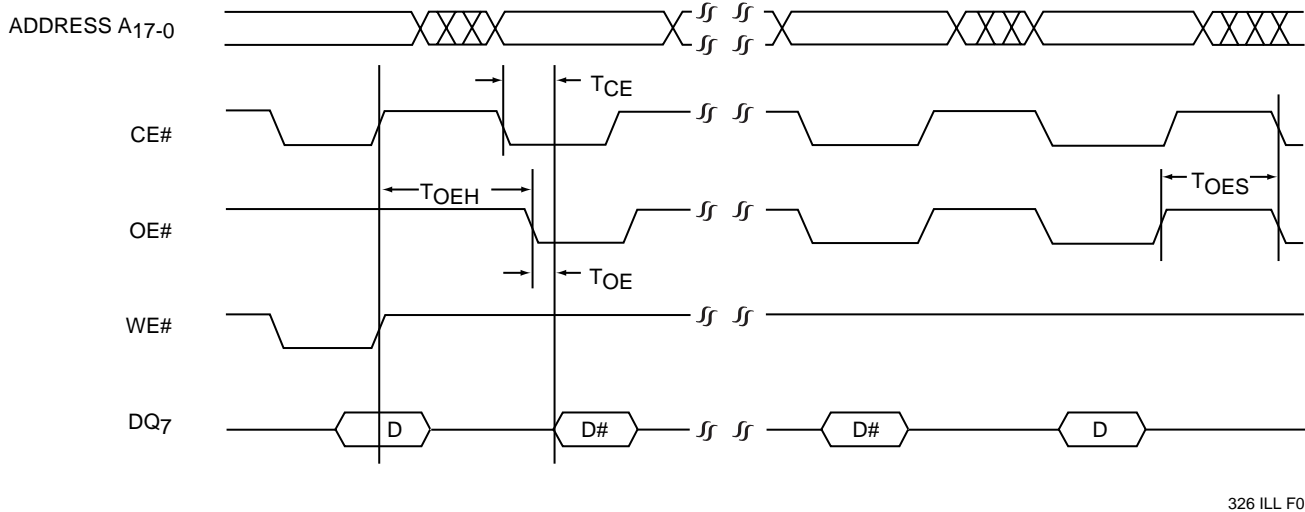


FIGURE 6: DATA# POLLING TIMING DIAGRAM



## 2 Megabit Multi-Purpose Flash SST39SF020

Preliminary Specifications

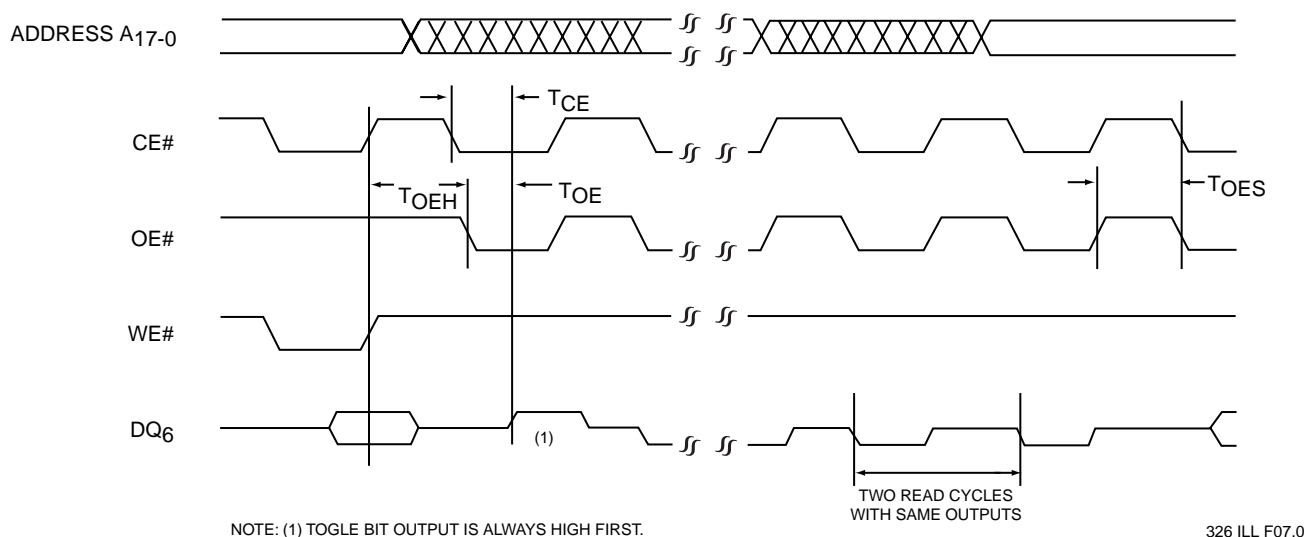
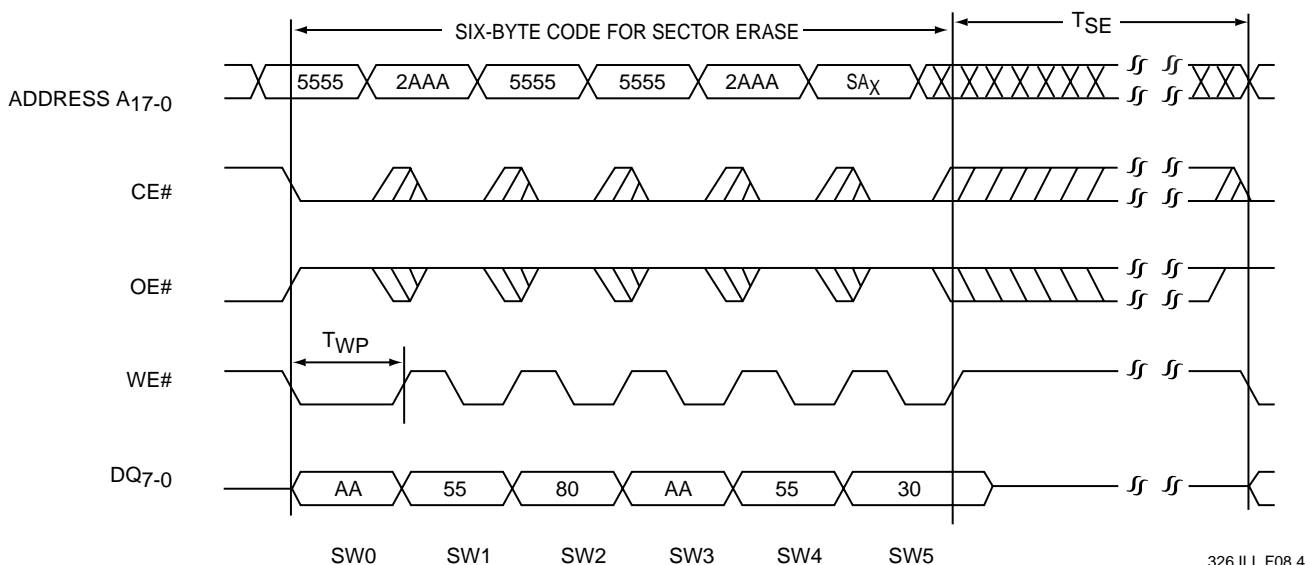


FIGURE 7: TOGGLE BIT TIMING DIAGRAM



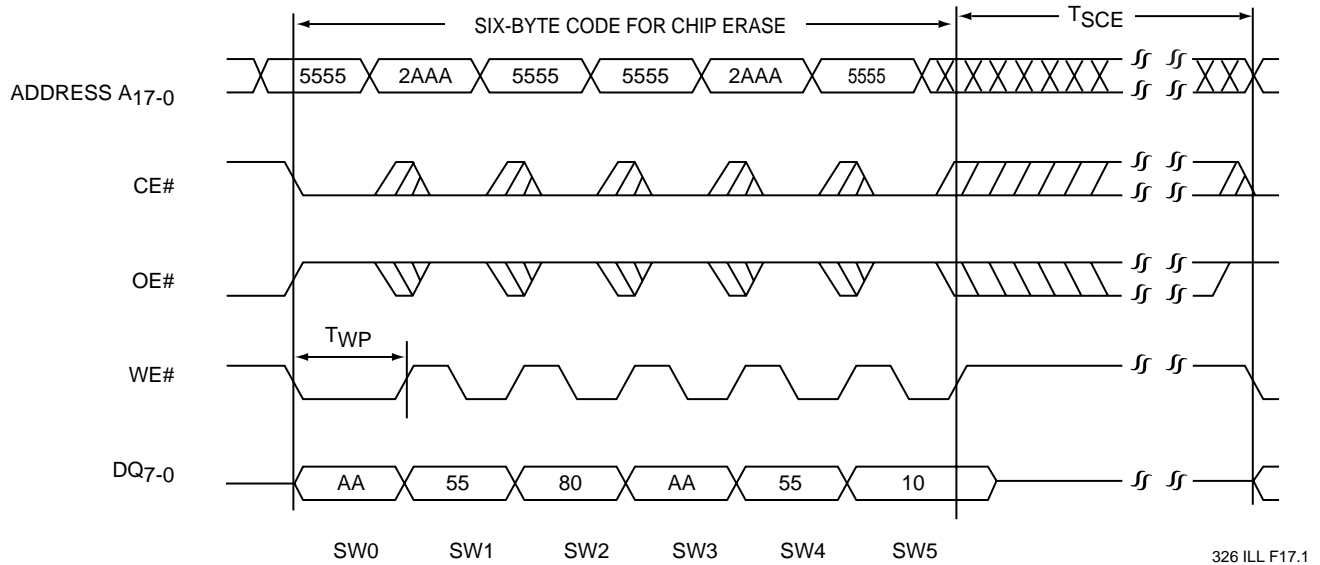
Note: The device also supports CE# controlled sector erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)  
SA<sub>x</sub> = Sector Address

FIGURE 8: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM

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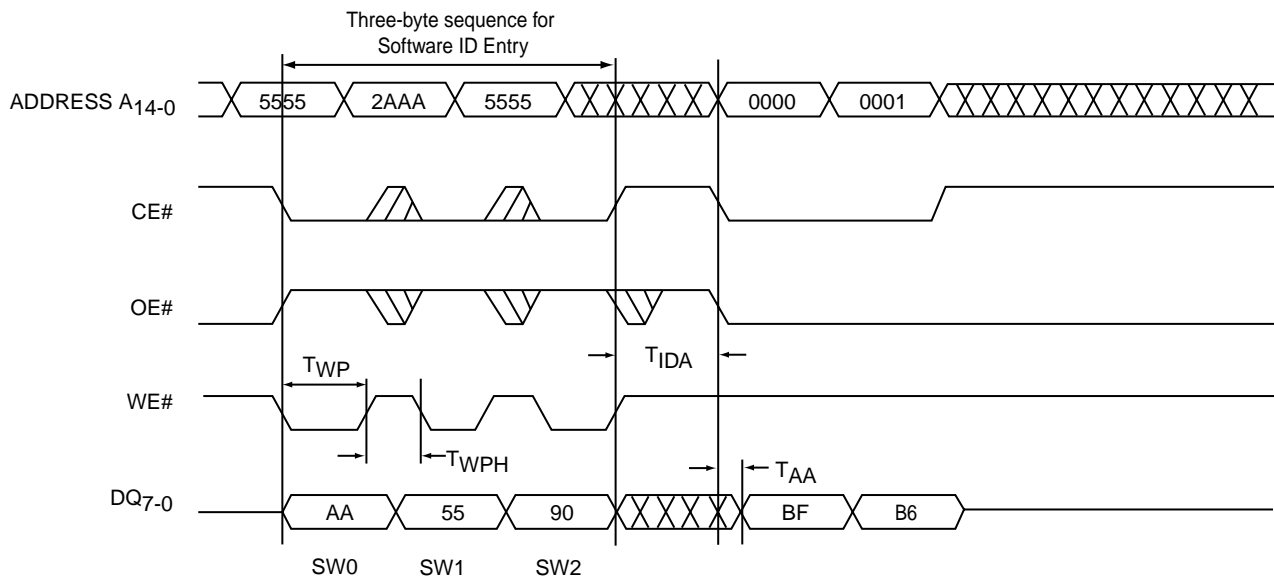


Preliminary Specifications



Note: The device also supports CE# controlled chip erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)

**FIGURE 9: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM**

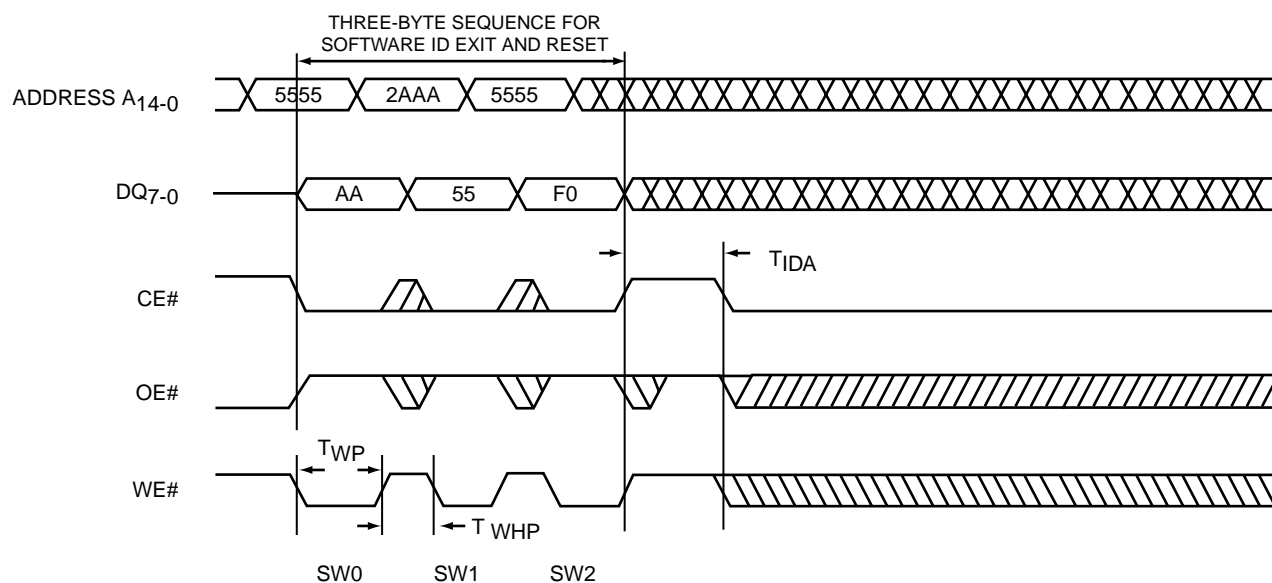


**FIGURE 10: SOFTWARE ID ENTRY AND READ**



## 2 Megabit Multi-Purpose Flash SST39SF020

Preliminary Specifications



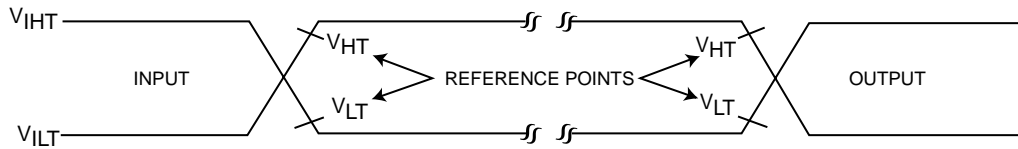
326 ILL F10.0

**FIGURE 11: SOFTWARE ID EXIT AND RESET**

## 2 Megabit Multi-Purpose Flash SST39SF020



Preliminary Specifications



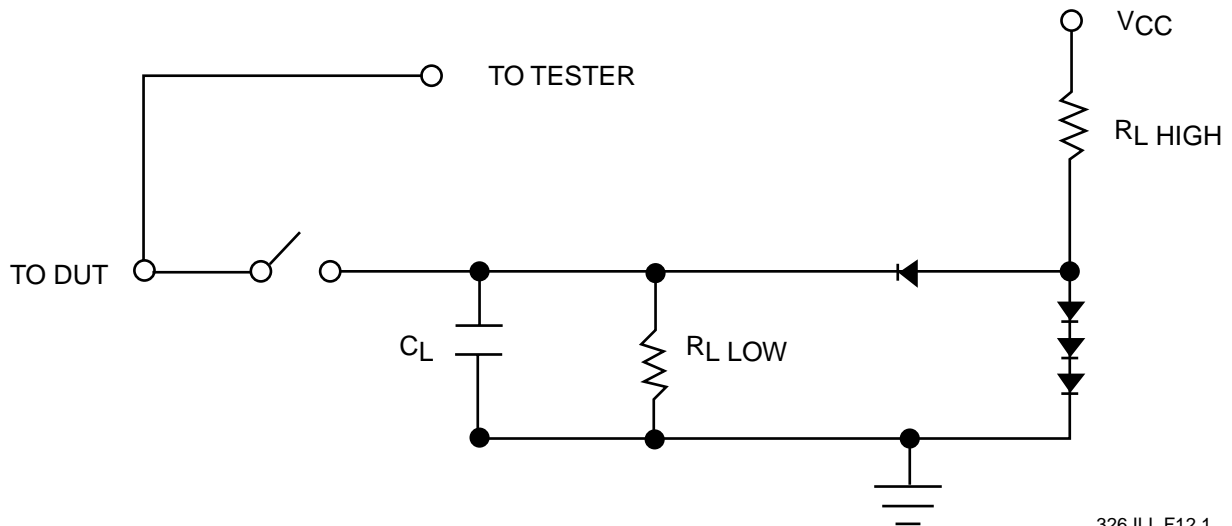
326 ILL F11.1

AC test inputs are driven at  $V_{IHT}$  (2.4 V) for a logic "1" and  $V_{ILT}$  (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are  $V_{HT}$  (2.0 V) and  $V_{LT}$  (0.8 V). Inputs rise and fall times (10%  $\leftrightarrow$  90%) are <10 ns.

Note:  $V_{HT}$ — $V_{HIGH}$  Test  
 $V_{LT}$ — $V_{LOW}$  Test  
 $V_{IHT}$ — $V_{INPUT}$  HIGH Test  
 $V_{ILT}$ — $V_{INPUT}$  LOW Test

FIGURE 12: AC INPUT/OUTPUT REFERENCE WAVEFORMS

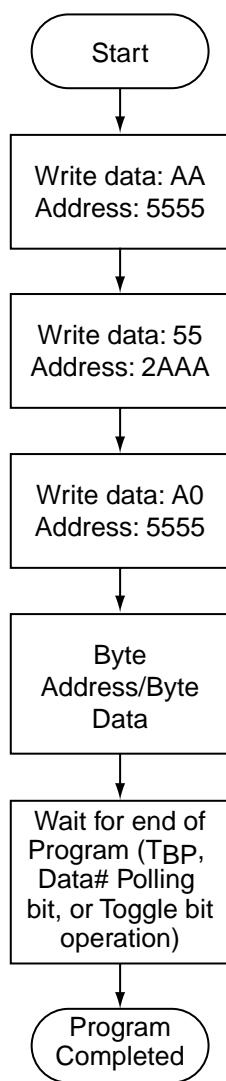
### TEST LOAD EXAMPLE



326 ILL F12.1

FIGURE 13: A TEST LOAD EXAMPLE





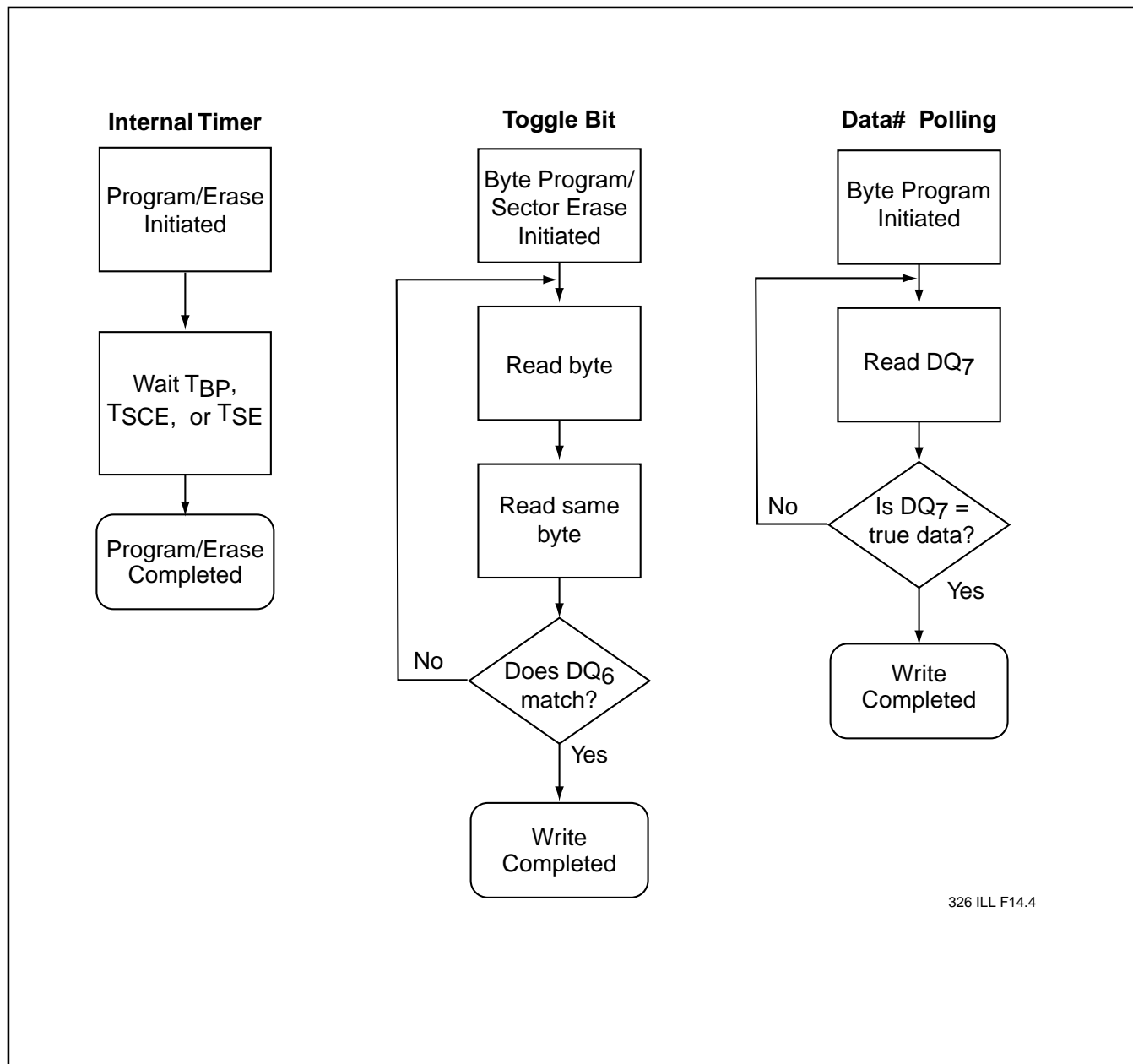
326 ILL F13.3

FIGURE 14: BYTE PROGRAM ALGORITHM



## 2 Megabit Multi-Purpose Flash SST39SF020

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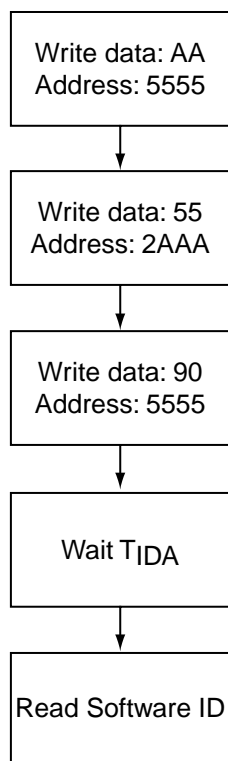


326 ILL F14.4

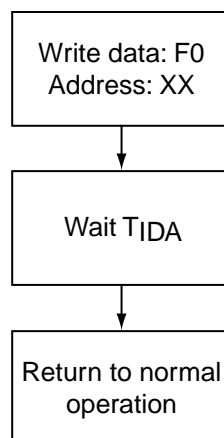
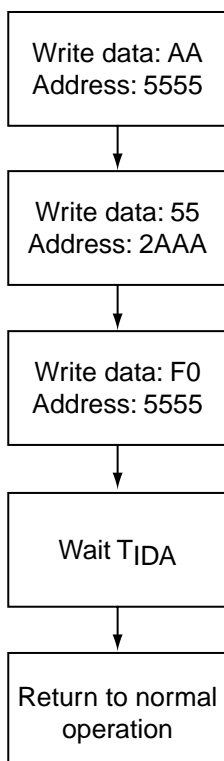
FIGURE 15: WAIT OPTIONS



**Software Product ID Entry  
Command Sequence**



**Software Product ID Exit &  
Reset Command Sequence**



326 ILL F15.1

**FIGURE 16: SOFTWARE PRODUCT COMMAND FLOWCHARTS**



## 2 Megabit Multi-Purpose Flash SST39SF020

Preliminary Specifications

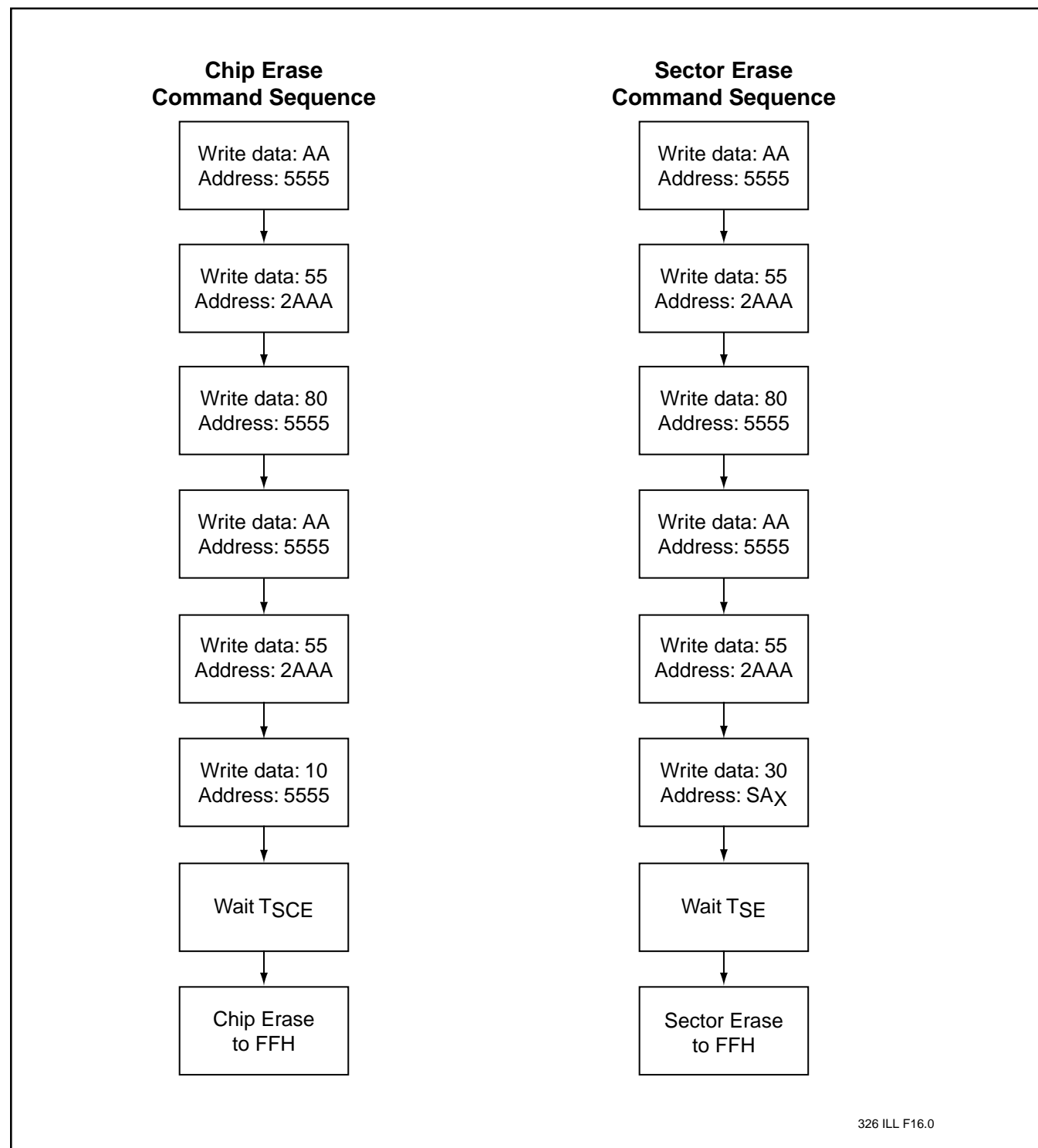


FIGURE 17: ERASE COMMAND SEQUENCE



## 2 Megabit Multi-Purpose Flash SST39SF020

Preliminary Specifications

| Device     | Speed | Suffix1 | Suffix2 |   |
|------------|-------|---------|---------|---|
| SST39SF020 | - XXX | - XX    | - XX    |   |
|            |       |         |         | <b>Package Modifier</b><br>H = 32 leads<br>Numeric = Die modifier                                       |
|            |       |         |         | <b>Package Type</b><br>P = PDIP<br>N = PLCC<br>W = TSOP (die up) (8mm x 14mm)<br>U = Unencapsulated die |
|            |       |         |         | <b>Temperature Range</b><br>C = Commercial = 0° to 70°C<br>I = Industrial = -40° to 85°C                |
|            |       |         |         | <b>Minimum Endurance</b><br>4 = 10,000 cycles   |
|            |       |         |         | <b>Read Access Speed</b><br>70 = 70 ns, 90 = 90 ns  |

### SST39SF020 Valid combinations

|                     |                     |                     |
|---------------------|---------------------|---------------------|
| SST39SF020-70-4C-WH | SST39SF020-70-4C-NH | SST39SF020-70-4C-PH |
| SST39SF020-90-4C-WH | SST39SF020-90-4C-NH | SST39SF020-90-4C-PH |
| SST39SF020-90-4C-U1 |                     |                     |

|                     |                     |
|---------------------|---------------------|
| SST39SF020-70-4I-WH | SST39SF020-70-4I-NH |
| SST39SF020-90-4I-WH | SST39SF020-90-4I-NH |

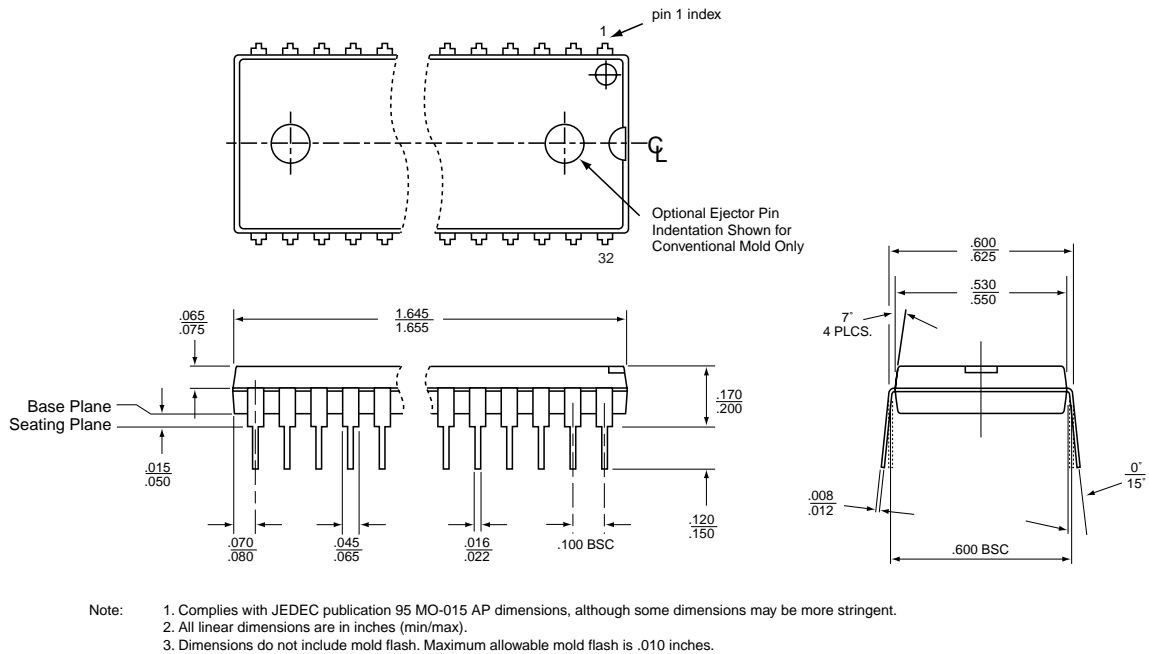
**Example :** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



## 2 Megabit Multi-Purpose Flash SST39SF020

Preliminary Specifications

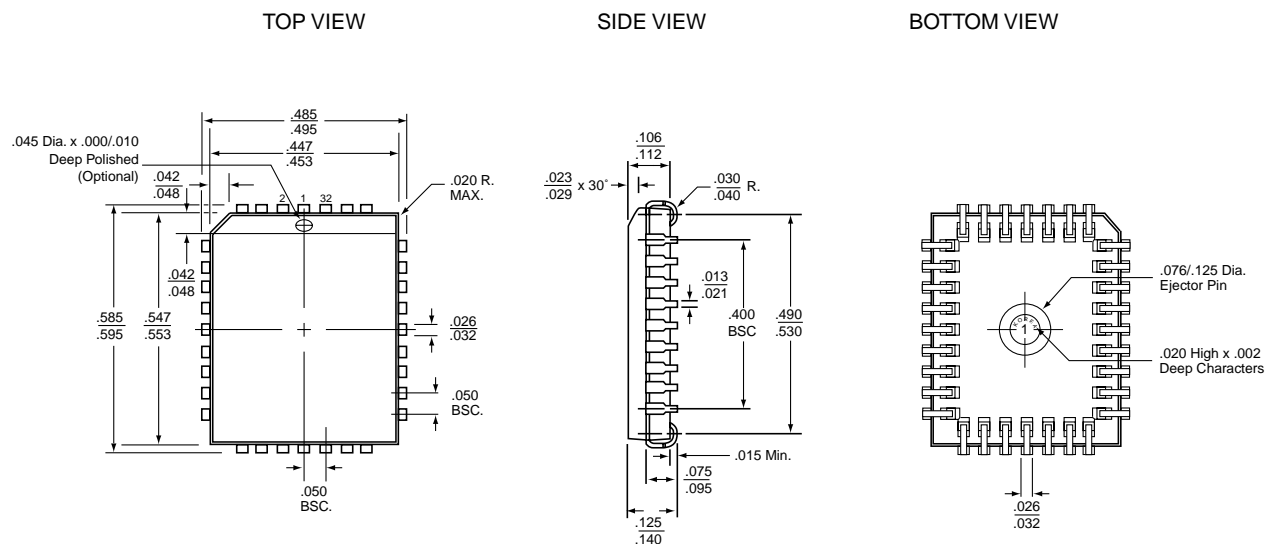
### PACKAGING DIAGRAMS



32.pdipPH-ILL.0

### 32-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)

SST PACKAGE CODE: PH



32.PLCC-NH-ILL.0

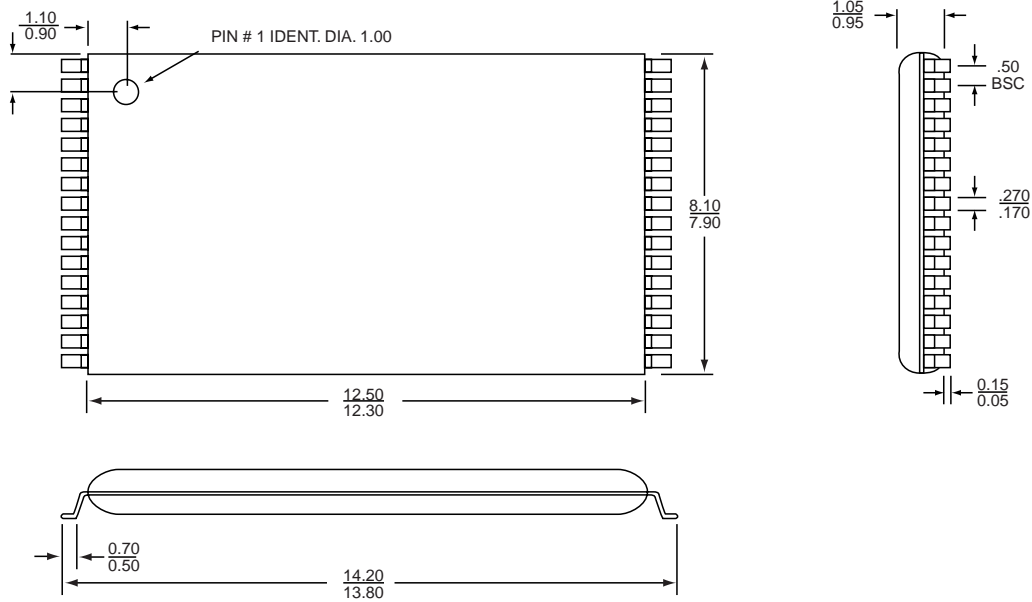
### 32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)

SST PACKAGE CODE: NH



## 2 Megabit Multi-Purpose Flash SST39SF020

Preliminary Specifications



Note:

1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 ( $\pm 0.05$ ) mm.

32.TSOP-WH-ILL.0

**32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)**

**SST PACKAGE CODE: WH**





## **2 Megabit Multi-Purpose Flash SST39SF020**

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Preliminary Specifications

**NOTES:**