1. General Descriptions

TRA1309B is a speaker amplifier that can accept PWM and analog signal and doesn't need any external device for these input signals. PWM input supports mainly for TRITAN's PWM output. The TRA1309B contains advanced de-pop circuitry which eliminates pops during power on/off, chip enable and disable. The gain can be adjusted by connecting a resistor between RGAIN and SPKN to determine gain . (Maximum gain = 7, if RGAIN floating) Internal sound processing is added for better sound quality.

2. Features

- Accept PWM and analog signal and doesn't need any external devices for these input signals.
- Mute function
- Wide operation voltage : 2.4V~5.5V
- sound processing for better sound quality
- Auto power ON/OFF
- Low standby current : 2u A, typ.
- High output power Pout = 0.65W (VDD=5.5V, THD=1%), Pout(PB) = 0.8W (VDD=5.5V, THD=1%, PB mode)

3. Packaging and Pads Information

Signal Name	Pin Type	Signal Description
SVDD	I	Speaker driver power input
SVSS	I	Speaker driver ground input
VDD	I	Internal circuit power input
VSS	I	Internal circuit ground input
PWMP_ANA	I	PWMP signal input at PWM mode, analog signal input at analog mode.
PWMN_CE	I	PWMN signal input at PWM mode, Chip enable signal at analog mode.
PASEN	I	When PASEN = VDD, chip operates in analog mode, connect to VSS for PWM mode
RGAIN	I	Gain adjust pad,
SPKP	O	Positive speaker output
SPKN	O	Negative speaker output
PB	I	Power boost, connect this pin to SVSS when high power is needed, can be left no connection if power < 0.6W

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to 5.5	V
Input Voltage	Vi	-0.5 to Vdd+0.5	V
Operating Temperature Range	Ta	-20 to 75	℃
Storage Temperature Range	Tstg	-40 to 150	℃

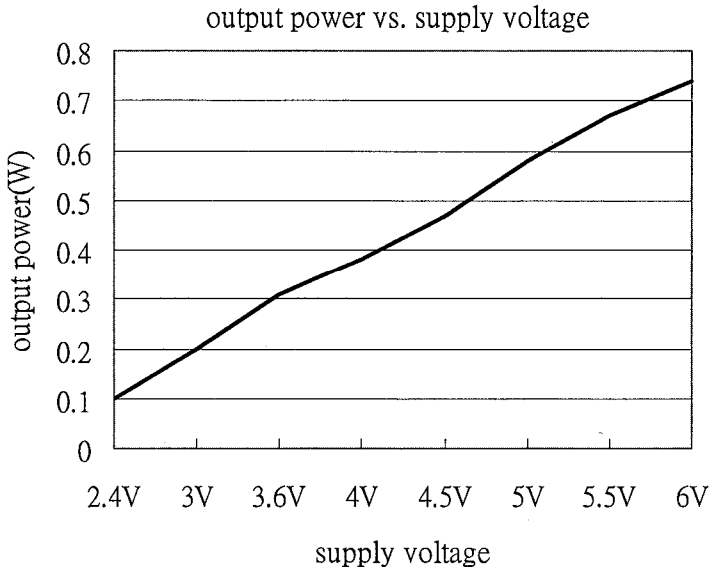
4.2 DC/AC Characteristics

Ta=25℃ unless otherwise noted

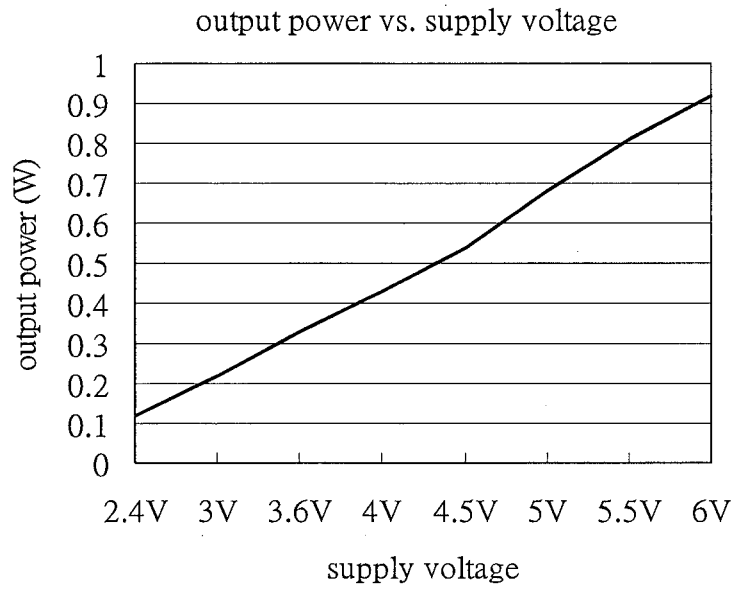
Parameters	Symbol	Minimum	Typical	Maximum	
Power supply range	VDD	2.4 V	-	5.5 V	
Operating current	Iop		6mA		VDD=5.5V
Standby current	Imute		2uA		1.When PASEN=VDD, PWMP_ANA=VSS or PWMN_CE=VSS 2.When PASEN=VSS PWMP_ANA=floating PWMN_CE=floating
Input high voltage	Vih	1V			VDD=2.4V~5.5V
Input low voltage	Vil			0.5V	VDD=2.4V~5.5V
Input current	Ic			0.1 uA 5 uA	1.PASEN=VDD (analog input mode) 2.PASEN=VSS (PWM input mode) When PWMP_ANA or PWMN_CE connect to VSS will sink this current
Pull up resistor	Rpull-h		2Meg ohm		VDD=3.3V PWMP_ANA & PWMN_CE
Output power	Pout		0.65W		VDD=5.5V,THD=1%
Output power(PB mode)	Pout(PB)		0.8W		VDD=5.5V,THD=1%, power boost mode
Mute time	Mt		30mS 200mS		Mute-on Mute-off
THD+Noise	THD+N		1%		VDD=5V,Pout=0.5W,R_L=8Ω,Gain=7
THD+Noise (PB mode)	THD+N(PB)		1%		VDD=5V,Pout=0.6W,R_L=8Ω,Gain=7

4.3 Output power perfomance

1. Output power vs. supply voltage (Fin = 1Khz, R_L = 8Ω, THD=1%, normal mode)



2. Output power vs. supply voltage (Fin = 1Khz, R_L = 8Ω, THD=1%, PB mode)



5. FUNCTIONAL DESCRIPTION

5.1 PWM signal transfer to Analog signal

If input signal is PWM, please set PASEN =VSS. This mode is mainly for TRITAN's PWM output. The PWMP direct connect to TRA1309B's PWMP_ANA and the PWMN direct connect to TRA1309B's PWMN_CE(Fig5-1). When PWM input is disabled, TRA1309B will enter power OFF mode automatically with mute-off sequence. When PWM enabled, TRA1309 will be turned ON automatically and mute-on sequence is executed(Fig 5-2).

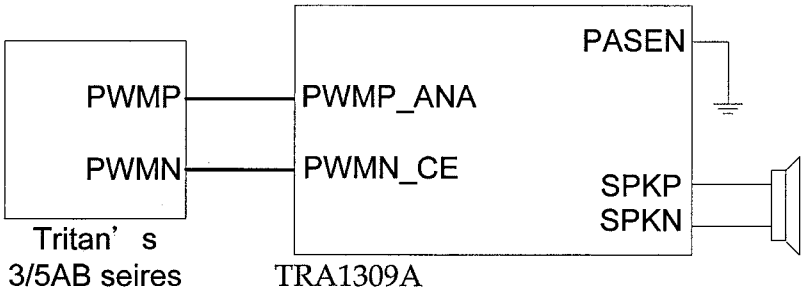


Fig 5-1 PWM input application circuit

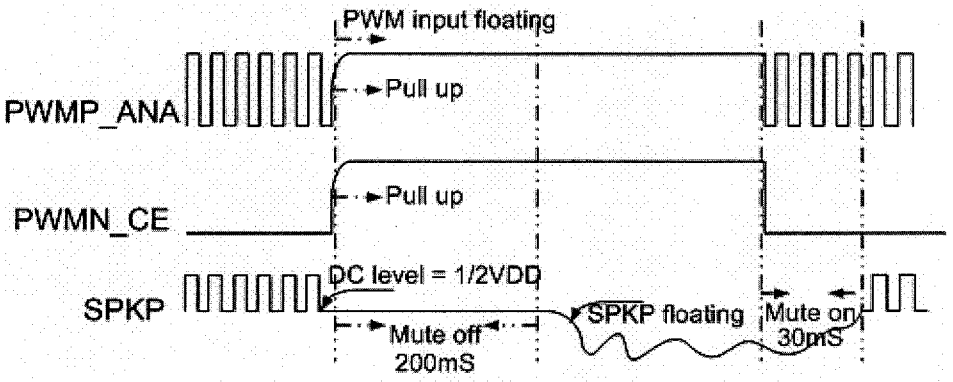


Fig 5-2 Mute sequence at PWM input

5.2 Analog signal input

If input signal is analog signal, please set PASEN=VDD. Capacitor is not needed for decoupling. Simply connect input analog signal to PWMP_ANA(input range = -0.3V~VDD+0.3V) Fig 5-3. Please set PWMN_CE=VDD to enter this mode, if analog input signal is Tritan's 7A series or similar current DAC type analog signal. Chip will enter and leave standby mode automatically(Fig 5-4). For other analog signal, please use PWMN_CE pin to control power ON/OFF and mute control. PWMN_CE=VSS for mute-off function and PWMN_CE=VDD for mute-on function(Fig 5-5).

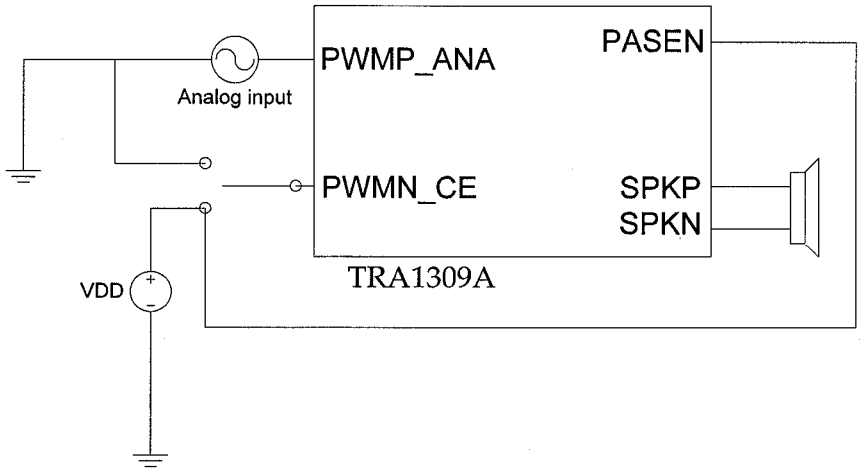


Fig 5-3 analog input application circuit

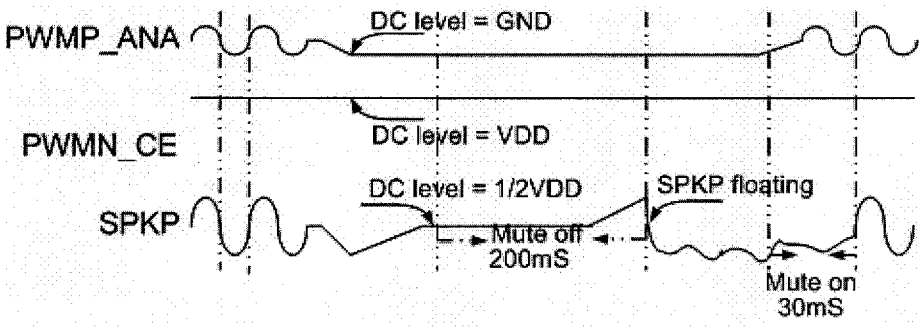


Fig 5-4 Mute sequence at Tritan's 7A series or similar current DAC input

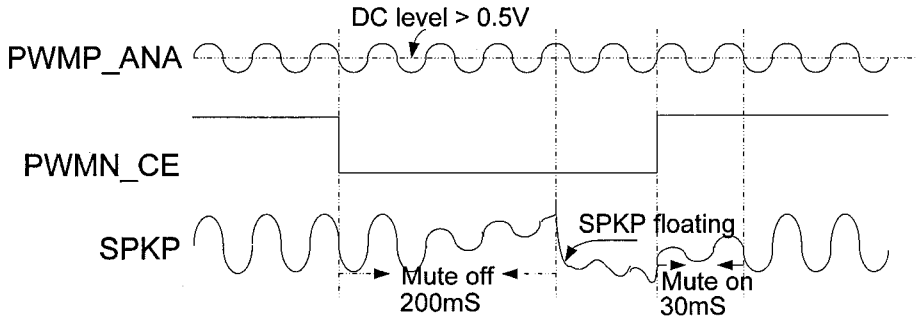
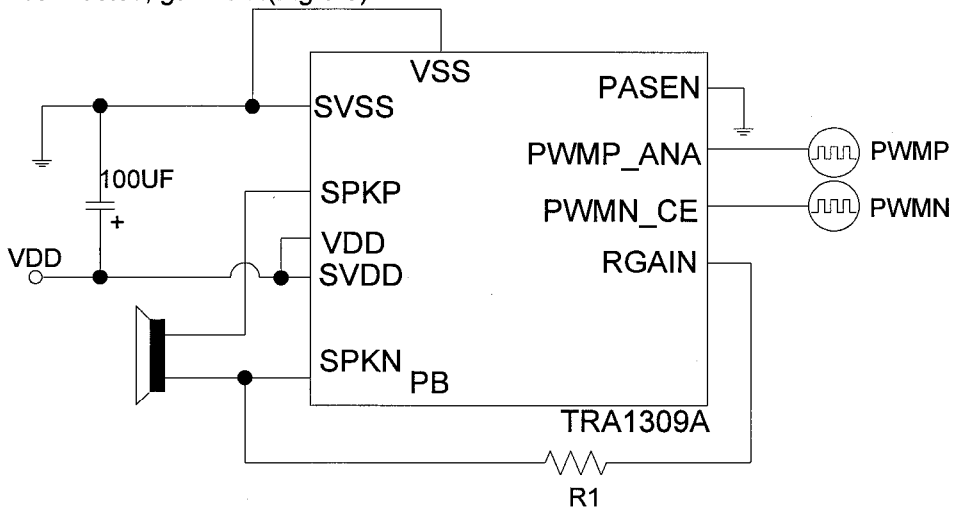


Fig 5-5 Mute sequence at general analog input

5.3 Gain adjust

TRA1309B could connect a resistor(R1) between RGAIN and SPKN to determine gain. If R1 is not connected, gain is 7.(Fig 5-6)

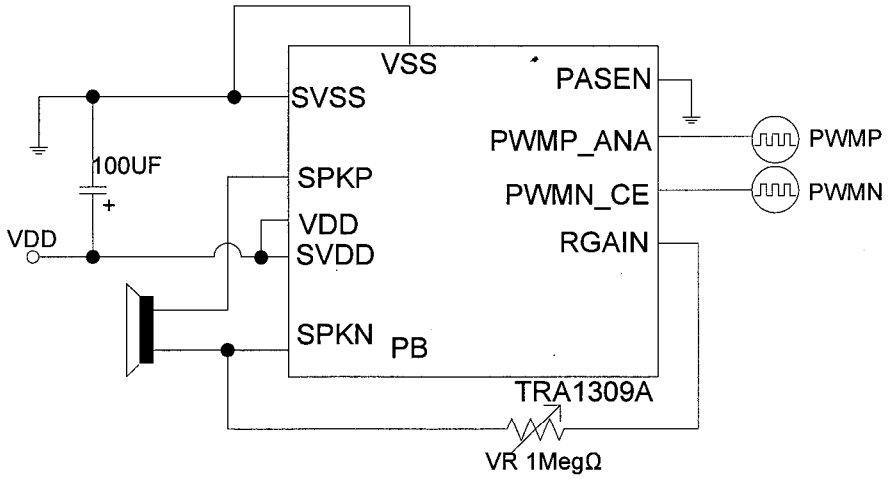


Gain = 2 * R1 / (120K + R1)

Fig 5-6 Use external resistor to determine gain

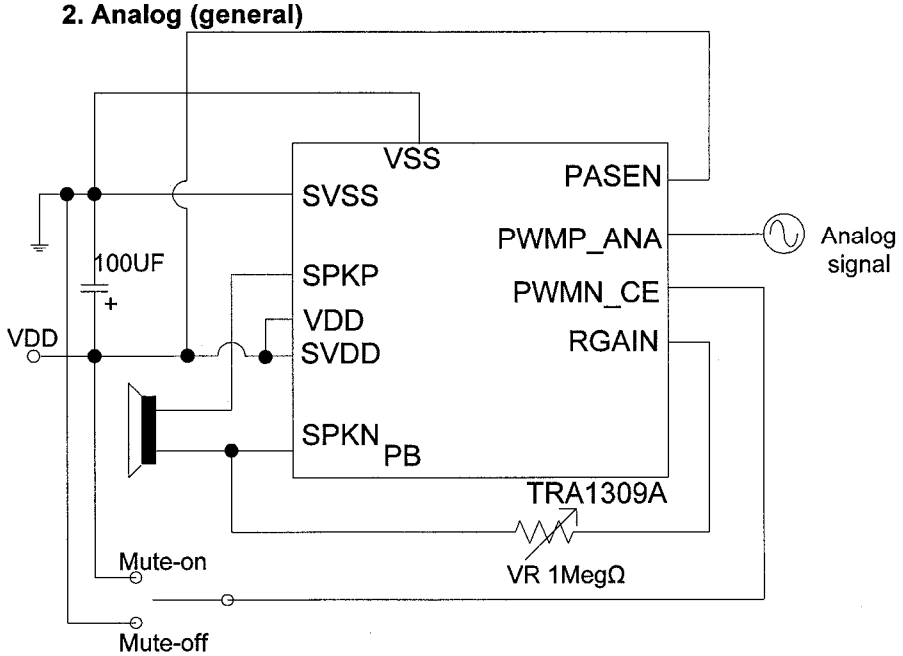
6. Application circuit

1. PWM



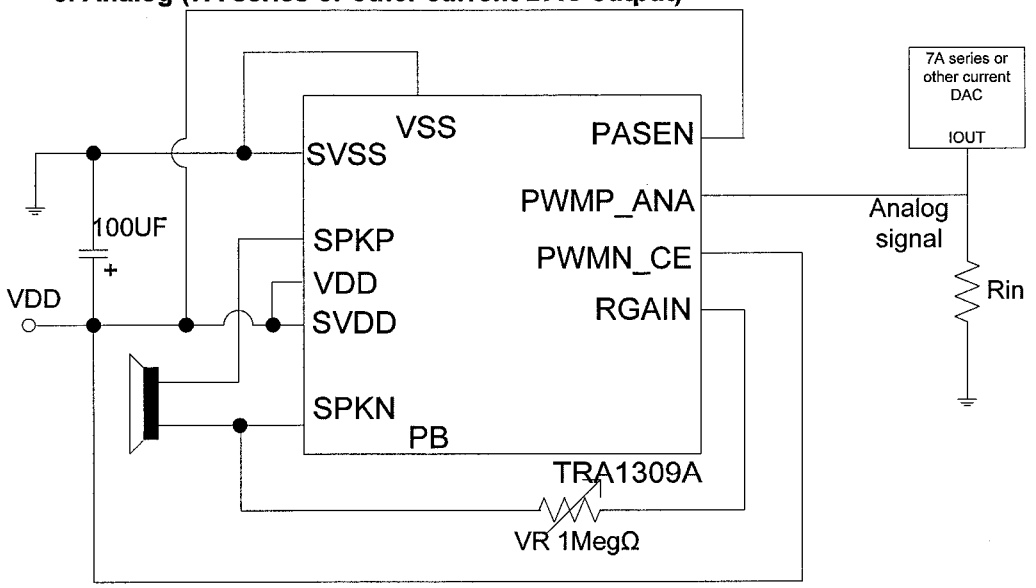
- If R1 = VR, 1MegΩ is suggested
- Wire of RGAIN must be kept as short as possible
- PB could connect to SVSS for power boost

2. Analog (general)



- If R1 = VR, 1MegΩ is suggested
- Wire of RGAIN must be kept as short as possible
- PB could connect to SVSS for power boost
- DC level of analog signal suggest ≧ 0.5V

3. Analog (7A series or other current DAC output)



- If R1 = VR, 1MegΩ is suggested
- Wire of RGAIN must be kept as short as possible
- PB could connect to SVSS for power boost
- Rin define for suitable Vin range.

When IOUT= 0~3mA, TRA1309B Gain=7

Vdd range	2-cell battery	3-cell battery	4-cell battery
Rin	360Ω	510Ω	620Ω

When IOUT=0~5mA, TRA1309B Gain=7

Vdd range	2-cell battery	3-cell battery	4-cell battery
Rin	220Ω	300Ω	510Ω

- Higher Rin value will increase overall gain, lower Rin value will reduce gain.

Note : Load capacitance on SPKP/SPKN must be take care of as followed :

Reisitor load between SPKP and SPKN	Maximum load capacitance
Open	100pF
8ohm	300pF

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
V1.0	New		2007.10.29