IRVINE SENSORS
CORPORATION

MS3110BDPC

Evaluation/Programming Board and Support Software

Operating Specifications and Users Manual

Irvine Sensors Corporation., 3001 Redhill Avenue, Costa Mesa, California 92626

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1.0 Scope

This document serves as the technical specifications and instructions for the IBM®-compatible PC-based Evaluation Board (MS3110BDPC) for Irvine Sensors Corporation. Universal Capacitive Readout™ IC, Part Number MS3110P (16-pin SOIC.) A functional description of the MS3110 is also included.

2.0 Introduction

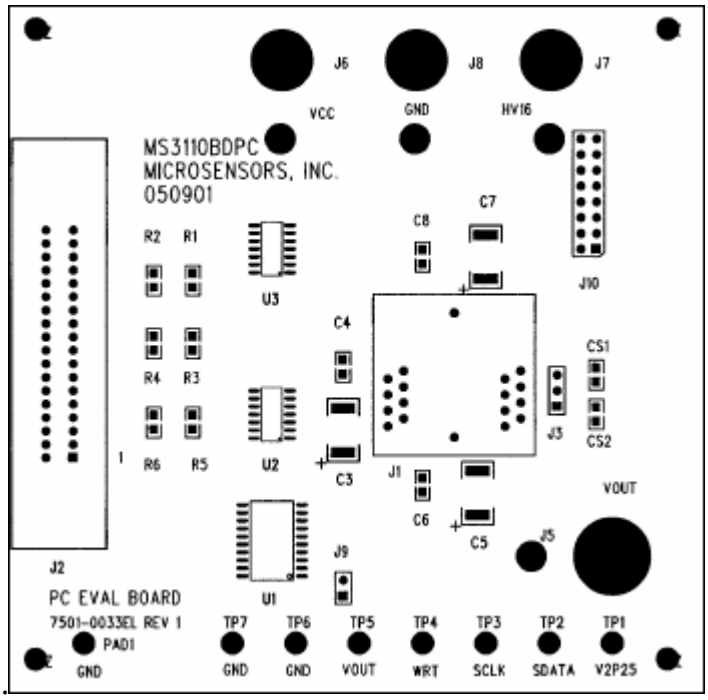
2.1. Overview of the MS3110BDPC Evaluation Board

The primary function of the MS3110BDPC Evaluation Board is to help the end user evaluate the operation of the MS3110 Universal Capacitive Readout IC. There are two major components of the Evaluation Board system. One is the board itself, a 4.5" X 4.5" PCB which includes test points, buffer devices, and a few other features. The second element is a Windows®-based program that provides the programming signals to the
MS3110 device.

The MS3110BDPC allows for full programming of the MS3110. There are two programming modes;
(1) a direct-write to the volatile internal registers, and (2) an EEPROM programming mode. The direct write mode allows the user to quickly examine the effect of bias, gain, and offset settings. Once a group of parameters have been determined, the user can program the internal EEPROM to store the values.

To aid in development, the MS3110BDPC includes many test points to measure several of the operating parameters, such as the reference voltage (V2P25) and the output signal (VOUT). Additional test points have been provided for monitoring of the programming signals to the MS3110. The MS3110BDPC has a ZIF socket that accommodates the 16-pin SOIC package. The Evaluation Board software includes volatile register read-back, the ability to store programming settings, and hard-copy generation (printing). The board operates from a single +5Vdc supply. A second source (+16Vdc) is necessary for programming the MS3110 EEPROM.

MS3110BDPC Evaluation Board Hardware

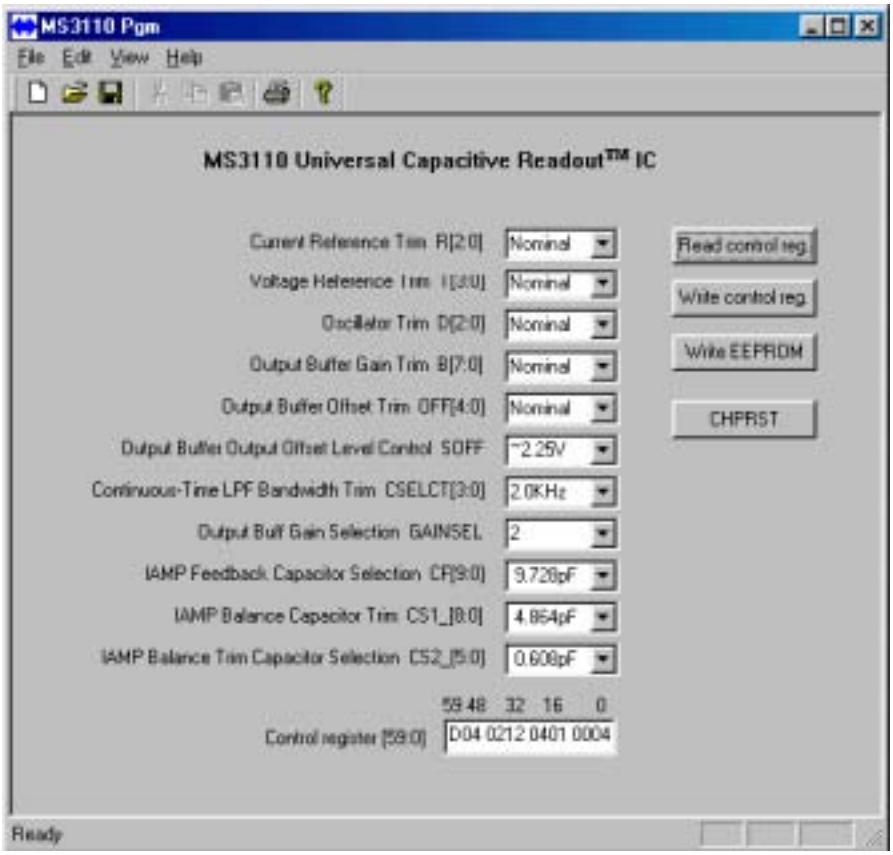


2.2. Overview of the MS3110 Software Program

The function of the software is to provide the programming settings and serial data stream for the MS3110. The program runs under Microsoft Windows Operating Systems. Interface to the Evaluation Board is via the parallel port, using a standard Centronics-type cable.

There are two components to the program; an executable file and an initialization file. *The initialization file must be located in the same directory as from where the executable file is launched.*
Both of these files will be explained in greater detail later in this document.

MS3110 Software Program



2.3. MS3110 Universal Capacitance Readout IC Overview

The MS3110 is a general purpose, ultra-low noise CMOS IC that transforms a changing input capacitance into an analog output voltage. The MS3110 can be interfaced to either differential or single capacitor elements. Sensitivity to 4.0aF/rtHz is typical for the IC. The MS3110 is extremely flexible, with many adjustable parameters including gain, bandwidth, and offset. An on-chip EEPROM is used to store desired settings. Only a single +5Vdc supply and a few decoupling components are required for operation. Please refer to the *MS3110 Universal Capacitance Readout™ IC Data sheet* for further details.

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3.0 Specifications for Operating Condition

Unless otherwise specified, the MS3110BDPC Evaluation Board shall operate under the conditions given below.

RECOMMENDED OPERATING CONDITIONS

Parameter	Specifications	Units
Power Supply Voltage VCC,VDD	4.8-5.2	Volts
Power Supply Voltage HV16	16-16.5	Volts
Operating Temperature	0-60	ºC
Analog Power Supply Noise, VCC	50	µVrms

ABSOLUTE MAXIMUM RATINGS

Parameter	Specification	Units
Power Supply Voltage VCC, VDD	5.5	Volts
Power Supply Voltage HV16	18	Volts
Storage Temperature Range	-65 to +125	ºC
All Inputs	-0.5 to 5.5	Volts

4.0 Software Installation & Operation

The software included with the Evaluation Board is located on the 3.5" MSDOS floppy disk. The MS3110BDPC connects to the PC via the parallel port using a standard Centronics-type printer cable. Plug the cable into the parallel port on the PC and connect the male Centronic end into the female connector on the MS3110BDPC.

4.1. Software Installation

There are two components of the MS3110 Evaluation Board software program. One part is the file marked *MS3110 Pgm*. This is the executable file. The other component is the initialization file, called *MS3110 pgm*. The initialization file provides the executable code with the necessary start-up parameters.

Installation is performed by copying both of the files from the floppy disk to the local fixed drive. One suggestion is to create a folder on the local fixed drive to place both the executable and initialization files. *The initialization file must reside in the same directory from where the executable is launched.* Using Windows Explorer, create a new folder in the desired location by selecting **New** under the **File** menu. A sub-menu will appear. Select **Folder**, and click the left mouse button. A new folder will appear in within the current directory, ready for naming. Name the folder *MS3110 Program*. Next, place the MS3110BDPC Software floppy disk into the A: drive, and click on the A: drive icon in the left window of the Explorer program. The two MS3110 files will appear in the right window. Select both files on the floppy and copy them to the newly created folder on the fixed drive

4.2. Software Operation

Double clicking on the MS3110 Pgm icon launches the program. The program uses the settings in the initialization file to determine certain operating parameters, such as the parallel port address and pin-out, initial values for each line, and the polarity.

The user-interface, shown on page 4 (MS3110 Software Program), will display once the program has successfully launched. All possible MS3110 programming configurations are available to the user through the software. The drop-down menu boxes to the right of the control register descriptors contain all the selectable settings. Each register in the MS3110 is shown in the software interface.

To select a particular value, place the mouse over the drop-down menu arrow and click the left button. Using the mouse, scroll through the available values and select the desired value by clicking the left mouse button. Some of the registers have a large number of values from which to choose. Use the slide boxes on the right to move throughout the selection range.

Once a particular setting is chosen, the **Control Register [59:0]** box will update to show the serial data stream that is to be loaded into the MS3110. The **Control Register** displays the data stream in hexadecimal format. The stream is loaded into the MS3110 beginning with bit 0, reading from right to left.

To load the parameters into the MS3110 volatile registers, place the mouse arrow over the **Write control reg.** button and click the left mouse button. The program will then send the data out the parallel port to the MS3110, via the Evaluation Board. Once loaded, the MS3110 will configure itself to the new settings. This programming mode is particularly useful for development since the effects of the setting changes can be seen immediately. However, the volatile register contents will be lost if power is removed from the MS3110, or a chip reset is issued (**CHPRST**).

When a particular set of parameters have been selected, the MS3110BDPC can be used to program the MS3110 EEPROM for long-term storage. To program the EEPROM, click on the **Write EEPROM** button. A pop-up box will appear prompting the user to turn on the +16Vdc supply. This step is necessary for storing the data to the EEPROM. After the supply is on, click the **OK** button. An hourglass will appear as the software loads the codes into the MS3110. Another pop-up box will prompt the user that the program load is complete and to turn off the +16Vdc supply. The selected register setting will now be stored in the MS3110 EEPROM.

In order to see that the EEPROM has been correctly written, a chip reset must be issued. To reset the MS3110, place the mouse pointer over the **CHPRST** button and click. This will cause the MS3110 to load the volatile registers from the EEPROM. Using the read-back feature verifies the contents of the volatile register.

Read-back is performed by placing the mouse pointer over the **Read control reg.** button and clicking. The software will extract the contents of the volatile registers from the EEPROM and display the settings in the **Control Register**. Also, the selection boxes for each register will jump to the assigned value. Important note: if the user would like to determine the contents of the EEPROM using the read-back feature, a chip-reset must be issued to the MS3110!

Along with interfacing to the MS3110, the PC-based software allows for printing, saving, and loading of the register settings. To print a set of register parameters, place the mouse over the **File** menu, and click the left button. A menu will appear with the **Print** option. Select it, and a printer dialog box will prompt the user for additional information. Click on **OK** to begin the print process.

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The user can also save MS3110 parameters to the computer. Select **Save As** under the **File** menu, and a dialog box will appear prompting the user for a file name. Note the required file extension is **.bin**. Enter the file name and click **Save**. To load a file, select **Open** under the **File** menu, located the desired file, select it, and click on the **Open** button.

4.3. Initialization File

The initialization file (MS3110 pgm.ini) contains the configuration settings for the executable code. The file type for the initialization file is listed as "Configuration Settings." It is important that this file be located in the same directory as the executable code. When the executable code is started the first thing it does is to search for the initialization file to determine important run settings.

The initialization file contains several lines of text. The file contents can be examined and modified. To open the file, simply double click on the file icon. Windows will open the file using the Notepad application. Be sure that the initialization file is saved before the executable is launched. Changes that are made in the Notepad application must be saved BEFORE the executable is opened. Only when the executable is launched does it read the initialization file.

The user can modify the initialization file. The important items are the Port Address, the Input, and the Output signals.

The text lines marked with *reg* (e.g. WRT_BACK *reg*, TESTSEL *reg*, WRT *reg*) determine the type of port register. The choices are:

- 0 = Data
- 1 = Status
- 2 = Control

On a parallel port, pins #2-#9 are all Data lines (output signals) and thus have the *reg* line set to 0. The MS3110BDPC uses pin #12 as the input (WRT_BACK), which is a Status line, and has the *reg* set to 1.

The *invert* lines determine which type of logic is to be used. A 0 indicated positive logic (low = ground, high = +5V), and a 1 indicates negative logic. It is also possible to set the initial state of the lines, using either a 1 or a 0 in the line marked *initial*.

Finally, there are two delay lines. The line marked TESTSEL *delay* determines the length of time, in milliseconds, that the TESTSEL line is pulled to a high logic before the EEPROM is programmed. TESTSEL remains high throughout the EEPROM program step. The CHPRST *delay* line determines the number of milliseconds that the CHPRST line is pulled to ground to reset the part.

5.0 Evaluation Board Hardware Guide

The MS3110BDPC interface board has many features, such as test points, access to programming signals, and a parallel-port interface for the PC. The following sections will describe the operation and features on the Interface board.

5.1. Connections

The MS3110BDPC requires only one +5Vdc supply for operation. The supply is connected to the banana jacks located on the upper edge of the board, with V+ to J6 (VCC) and ground to J8 (GND). In order to program the MS3110, a second power source is required. The supply voltage is +16Vdc and should be connected from J7 (HV16), to ground J8 (GND). Be careful not to cross the power supply connections as this could damage the interface board and the personal computer.

The PC parallel port connector is located on the left edge of the board. It is a standard Centronics-type connector. Using a printer cable, plug the female Centronics connector in to the MS3110BDPC. Then connect the other end to the parallel port of the PC.

5.2. Signal and Test Points

Many signal and test points are provided on the MS3110BDPC. These allow the user to monitor programming signals such as WRT, SDATA, and SCLK, and to examine the "status" of the MS3110. There is a BNC connector for VOUT, a test point to monitor the reference voltage, and a jumper for measuring the reference current.

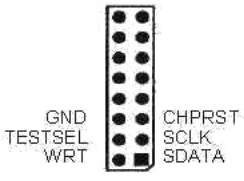
The programming signals are activated when the software sends information to the MS3110 or the MS3110 is reading back settings to the software. Using a storage oscilloscope or a logic analyzer, the user can capture the SDATA (TP2), SCLK (TP3) and WRT (TP4) signals for examination.

An additional test feature is provided by the MS3110BDPC; monitoring the reference bias current. This is done using the jumper J9. To measure the bias current, pull the shunt block off of the jumper, then connect an ammeter between the upper pin and ground. The current should be ~10μA. See Section 6.2.1 for more information on the reference current.

5.3. Jumper J10

The MS3110BDPC also includes a 16-pin jumper block for access to the programming signals.

The diagram below shows the pin-out for J10.



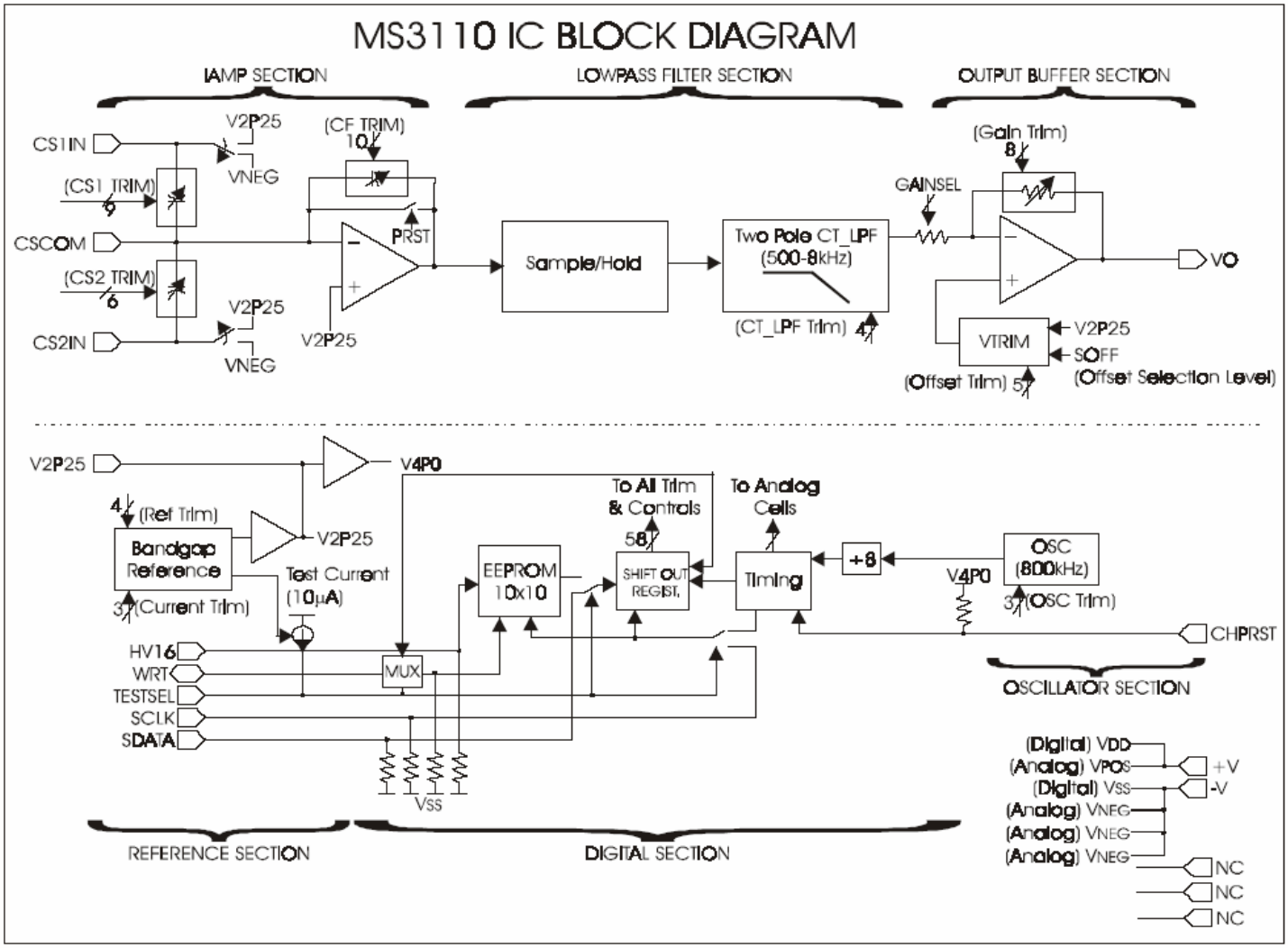
J10

6.0 MS 3110 Programming Specifications

6.1 Programming Map and Modes

6.1.1 EEPROM Nomenclature and Description

The following programming bit description and their programming map are presented below. The truth tables are presented in section 6.2. The MS3110 Diagram below illustrates the locations of the trims and features. The block diagram also shows a simplified view of the internal components of the MS3110. There are three basic sections: a charge amplifier, a low-pass filter, and an output buffer. These three blocks are part of the forward signal path that performs the capacitance-to-voltage transform. The MS3110 also contains digital contains logic to support the operation of the analog signal path.



Nomenclature and Descriptions

Name	No. bits	Description
R[2:0]	3	Current Reference Trim Bits
T[3:0]	4	Voltage Reference Trim Bits
D[2:0]	3	Oscillator Trim Bits
B[7:0]	8	Output Buffer Gain Trim
OFF[4:0]	5	Output Buffer Offset Trim
SOFF	1	Output Buffer Output Offset Level Control
CSELCT[3:0]	4	Continuous-Time LPF Bandwidth Trim
GAINSEL	1	
CF[9:0]	10	IAMP Feedback Capacitor Selection
CS1_[8:0]	9	IAMP Balance Capacitor Trim
CS2_[5:0]	6	IAMP Balance Trim Capacitor Selection

EEPROM Location Mapping

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADDR 9	R2	R1	R0	T3	T2	T1	T0	D0	D1	D2
ADDR 8		B0	B1	B2	B3	B4	B5	B6	B7	OFF0
ADDR 7	OFF1	OFF2	OFF3	OFF4	SOFF	CSELCT 3	CSELCT 2	CSELCT 1	CSELCT 0	
ADDR 6		GAINSEL		CF9	CF8	CF7	CF6	CF5	CF4	CF3
ADDR 5	CF2	CF1	CF0	CS1_8	CS1_7	CS1_6	CS1_5	CS1_4	CS1_3	CS1_2
ADDR 4	CS1_1	CS1_0	CS2_0	CS2_1	CS2_2	CS2_3	CS2_4	CS2_5		
ADDR 3										
ADDR 2										
ADDR 1										
ADDR 0										

All other locations are unused.

6.2. Programming Truth Tables

6.2.1. Bias Control Registers

Two trims are included in the master bias circuitry. The bandgap reference voltage can be trimmed to an optimum voltage with a trim range of +/-5.1%. Since the 2.25V DC reference tracks the bandgap reference voltage, the user can monitor the variation through pin V2P25. The reference level can be trimmed in 19 mV steps. This allows variations of the 2.25V Reference to be trimmed over process. An abridged version of the truth table is included below.

V2P25 Reference Voltage Trim (~19mV /step)

T3	T2	T1	T0	Voltage Trim
0	0	0	0	+5.1%
1	0	0	0	Nominal
1	1	1	1	-5.1%

FOR ALL APPLICATIONS, the V2P25 voltage reference should be trimmed to 2.25V +\-10mV.

In addition, the current reference can also be monitored and trimmed. The current monitor point is brought out to the TESTSEL pin that normally selects the mode of operation for the MS3110. But it also serves to monitor the internal bias current of 10µA typical when the pin is tied to logic low. The current reference can be monitored on the MS3110BDPC at jumper J9. Pull the shunt block off of the jumper, then connect an ammeter between the upper pin and ground to measure the bias current. Using the trim controls R[2:0], adjust the current to within the specification. Be sure to replace the shunt after completing trimming the reference current. The Current reference can be trimmed in 0.4 µA steps. An abridged version of the truth table is included below.

Current Reference Trim (~0.4µA/step)

R2	R1	R0	Current Trim
0	0	0	-32%
1	1	0	Nominal
1	1	1	+32%

FOR ALL APPLICATIONS, the current reference should be trimmed to *10µA+\-2µA.*

6.2.2. Oscillator Control Registers

Included in the MS3110 is the ability to trim the oscillator frequency over process. The truth table for trim is presented on the next page.

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Oscillator Trim

D2	D1	D0	Frequency Trim
0	0	0	Nominal
0	0	1	+15%
0	1	0	+24%
0	1	1	+33%
1	0	0	Nominal
1	0	1	-35%
1	1	0	-47%
1	1	1	-81%

FOR ALL APPLICATIONS, the Oscillator frequency reference should be trimmed to 100KHz +\- 5KHz. Monitoring can be done via CS2IN (J3 pin #1) or CS1IN (J3 pin #3).

6.2.3. Input Amplifier Control Registers

The analog front-end includes a capacitance transimpedance amplifier (IAMP) with a programmable feedback capacitor. The capacitor includes 10 bits of programmability in 19fF +/- 20% steps. The programmability allows the user to optimize the feedback capacitor for range and performance. An abridged version of the programming truth table is included below. The block diagram in Section 6.1 shows the location of the feedback capacitor in the signal path.

Feedback Capacitor Array CF (9:0) Binary Weighted (in 19fF steps)

CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0	Capacitor (pF)
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0.019
0	0	0	0	0	0	0	0	1	0	0.038
:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	9.728
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	19.437

The MS3110 ASIC is designed to receive pseudo-differential input-sense capacitors. The intention of designing in the CS1 capacitor array is to give the user the option to operate the ASIC single-ended over the entire 0.2pF-10pF operating input. The capacitor includes 9 bits of programmability in 19fF +/- 20% steps. The resolution of 19fF allows the user to balance the CS1 capacitance with the CS2 external capacitance to minimize offset. An abridged version of the programming truth table is included below. The block diagram in Section 6.1 shows the location of the feedback capacitor in the signal path.

Balance Capacitor Array CS1 (8:0) Binary Weighted (in 19fF steps)

CS1_8	CS1_7	CS1_6	CS1_5	CS1_4	CS1_3	CS1_2	CS1_1	CS1_0	Cap (pF)
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0.019
0	0	0	0	0	0	0	1	0	0.038
:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	4.864
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	9.709

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When the MS3110 is operated differentially, with the external sensing capacitors connected to the CS1IN and CS2IN, there is usually a capacitance imbalance that leads to a DC offset at the MS3110 signal path output. The CS1 Capacitor array, along with the CS2 Capacitor array, assists in reducing the DC offset by balancing the common-mode capacitance to within 19fF+/- 20% resolution. An abridged version of the programming truth table for CS2 array is included below.

Trim Capacitor Array CS2(5:0) Binary Weighted (in 19fF steps)

CS2_5	CS2_4	CS2_3	CS2_2	CS2_1	CS2_0	Cap (pF)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.019
0	0	0	0	1	0	0.038
:	:	:	:	:	:	:
1	0	0	0	0	0	0.608
:	:	:	:	:	:	:
1	1	1	1	1	1	1.197

6.2.4. Lowpass Filter Control Registers

The two-pole lowpass filter section is designed with a programmable bandwidth ranging from 500Hz to 8KHz. The bandwidth selection error falls within +/-21% for any desired filter frequency within this filter range.

The truth table and the respective nominal 3dB bandwidths are included below. The block diagram in Section 6.1 shows the trim location in the signal path.

Continuous-Time LPF Controls

CSELCT3	CSELCT2	CSELCT1	CSELCT0	Bandwidth (KHz)
0	0	0	0	8.0
0	0	0	1	5.8
0	0	1	0	4.2
0	0	1	1	3.0
0	1	0	0	2.0
0	1	0	1	1.4
0	1	1	0	1.0
0	1	1	1	0.76
1	0	0	0	0.49

*1001-1111 are unused states.

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6.2.5. *Output Buffer Control Registers*

The output buffer is designed with three programmable features. The first is the offset reference level control. The MS3110 allows two reference levels for the output signal. They are nominally 0.5V for single-variable mode and 2.25V for differential mode. The truth table for this selection is included below. The block diagram in Section 6.1 shows the trim location in the signal path.

Offset Reference Level Control

SOFF	Output Offset
0	VREF~2.25V
1	~0.5V

In addition, a fine trim for the DC offset is included in the output buffer. This offset trim is in addition to the offset trim available with the CS1 and CS2 trim capacitor array discussed in Section 6.2.3. The offset trim for the output buffer ranges +/- 100mV in 6.25mV steps. An abridged version of the truth table is included below and is applicable for GAINSEL = 0.

Offset Trim Control (~6.25mV/step)

OFF4	OFF3	OFF2	OFF1	OFF0	Offset Trim
0	0	0	0	0	-100mV
1	0	0	0	0	Nominal
1	1	1	1	1	100mV

A fine trim for the signal path gain is included in the output buffer with a nominal gain of 2 V/V or 4V/V. This gain trim is in addition to the gain trim available with the CF trim capacitor array discussed in Section 5.2.3. The gain trim for the output buffer ranges +/- 0.3V/V in 0.0024V/V steps. An abridged version of the truth table is included below.

Gain Control (~0.0024 V/V per step) for GAINSEL = 0

B7	B6	B5	B4	B3	B2	B1	B0	Gain Trim
0	0	0	0	0	0	0	0	-15%
1	0	0	0	0	0	0	0	Nominal
1	1	1	1	1	1	1	1	+15%

Nominal Output Buffer Gain Setting Control

GAINSEL	GAIN V/V
1	4
0	2

7.0 MS3110 UNIVERSAL CAPACITIVE READOUT™ OVERVIEW

7.1. Overview of the MS3110

The MS3110 is a CMOS integrated circuit designed to interface with capacitive-type sensors, such as pressure sensors, accelerometers, gyros, and any other mechanical means which capacitance or change in capacitance needs to be sensed. The MS3110 is designed to operate off a single +5VDC supply.

The MS3110 signal path itself contains three major building blocks. They are the Capacitive Trans-impedance Amplifier (IAMP), the Low-Pass Filter, and the Output Buffer. The IAMP stage is designed to accommodate a large range of sense capacitance (0.2-10pF) by including a range of feedback capacitors as well as balance and trim capacitors. The IAMP is able to operate single-variable or differentially. It features a large range of feedback capacitance trim to accommodate a large span of applications and input offset capacitance trims. The Low-Pass Filter limits the signal and noise bandwidths and is selectable over the range of 500Hz to 8KHz with a two-pole frequency response. Finally, the Output buffer serves to drive the signal into an Analog-To-Digital Converter input stage. The Output buffer has a nominal gain of 2 or 4V/V and also accommodate a gain trim, an offset trim and a reference voltage selection.

Internal to the MS3110 are various supporting cell blocks, including an internal oscillator (trimmable), EEPROM, Digital Cells for timing and logic functions, and reference voltage generators. The V2P25 Voltage Reference Output may be used as an ADC reference voltage for good temperature tracking.

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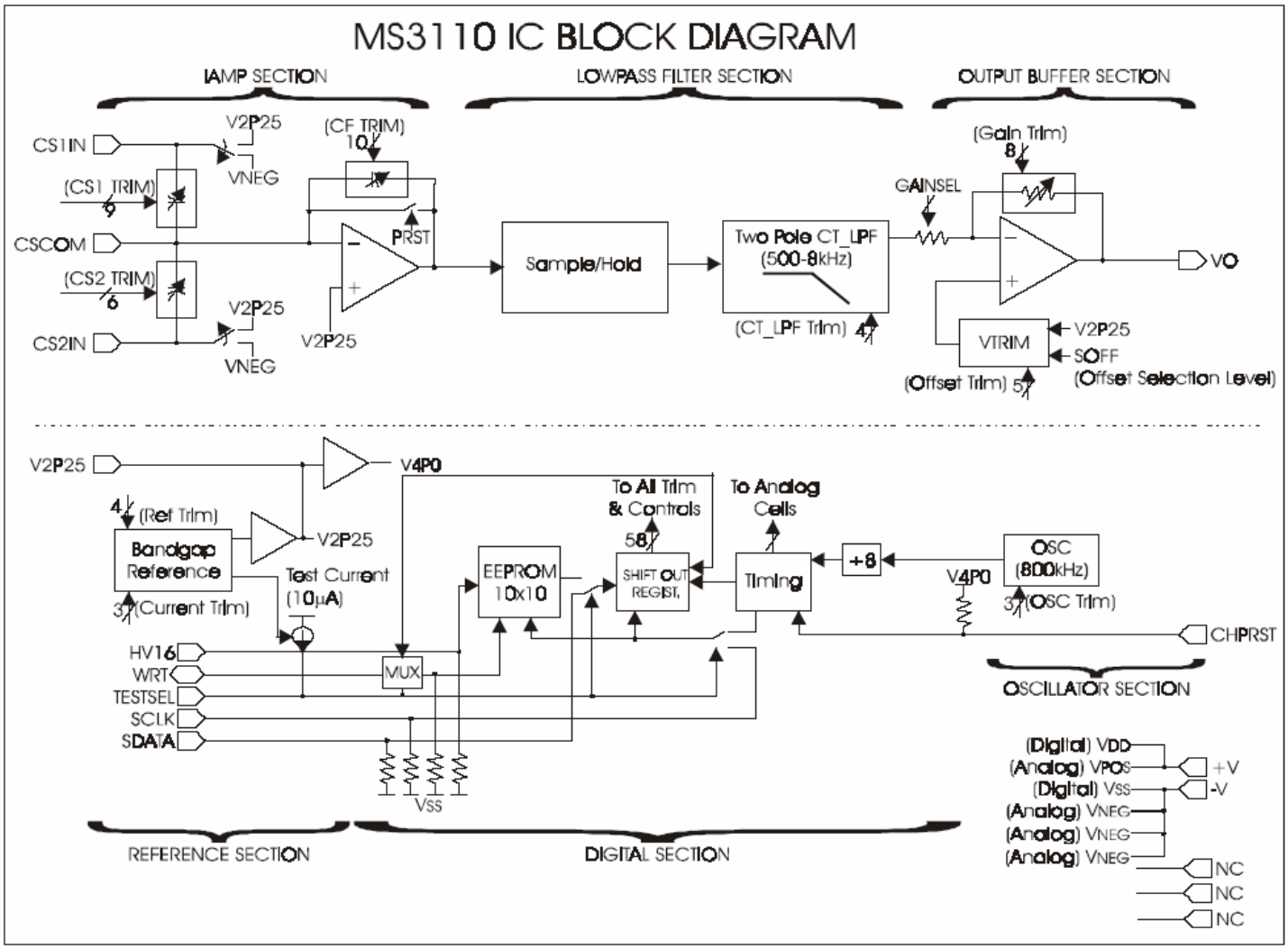


7.2. MS3110 Theory of Operation

The MS3110 senses the difference between two capacitors and outputs a voltage proportional to the difference. A block diagram of the MS3110 is shown above. The capacitors to be sensed are an external balanced pair, CS1 and CS2 on port CS1IN and CS2IN respectively. The output voltage as a function of the sensing capacitance CS1T and CS2T is:

$$VO = Gain * V2P25 * 1.14 * [(CS2-CS1)/CF] + VREF \quad Volts$$

where the Gain is nominally 2 V/V or 4 V/V and is trimmable, V2P25 is the ASIC internal 2.25V DC Reference, and CF is the Capacitor Feedback around the Input Trans-Impedance Amplifier, can be selected to optimize for the range of the input sensing capacitors. VREF can be 2.25V or 0.5V.

Notes:

CS2T = CS2IN + CS2 ;For CF ≥ 1.5pF, and CS2T = CS1T, Then V_0 = VREF
CS1T = CS1IN + CS1

7.3. Pin-out of the MS3110

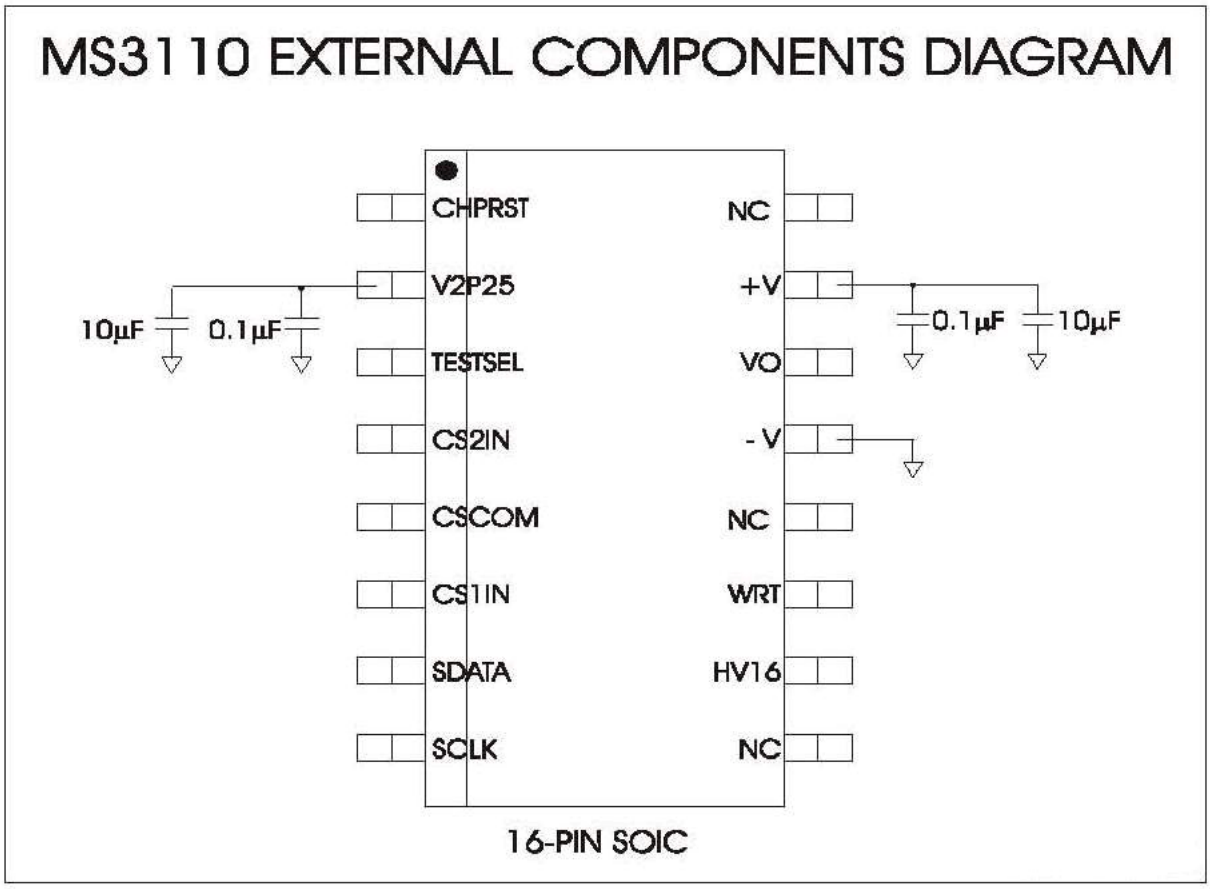
The MS3110 SOIC pin-outs are presented below.

Pin-out/Pad-out

SOIC Pin No.	Name	Description
1	CHPRST	ASIC Reset, internally pulled up. Normally 4.0V
2	V2P25	2.25V DC Reference.
3	TESTSEL	Test Select. Enables the user to bypass the on-chip EEPROM and program the ASIC directly.
4	CS2IN	Capacitor sensor input 2, to be connected with the upper electrode.
5	CSCOM	Capacitor sensor common, to be connected to the common sensor node.
6	CS1IN	Capacitor sensor input 1, to be connected with the upper sensor electrode.
7	SDATA	Serial Data Input, used for the serial data input port for programming the EEPROM or the ASIC registers directly. This node is internally pulled down.
8	SCLK	Serial Clock Input, serves as the strobe which the ASIC latches the serial data. This node is internally pulled down.
9	NC	No Connect.
10	HV16	16V DC input port, tied to 16V when writing to EEPROM and Grounded otherwise.
11	WRT	Write Select. Enables the user to program the on-chip EEPROM.
12	NC	No Connect
13	-V	Negative Voltage Rail, usually 0V.
14	VO	ASIC Signal Path Voltage Output.
15	+V	Positive Voltage Rail, usually +5V.
16	NC	No Connect

7.4 External Component Requirements

The MS3110 requires only a few components for optimum performance. It is recommended that the following ports have a 10µF in parallel with a 0.1µF to a local GND: V2P25, and +V. HV16 decoupling capacitors are optional. See Diagram below.



7.5 MS3110 Orientation in the ZIF socket on the Evaluation Board

The MS3110 is placed in the ZIF socket (J1) with pin 1 located in the lower right corner. This will orient the 16-pin SOIC so the CS2IN, CSCOM, and CS1IN pins are along the right side of the ZIF socket, near the interface pads and jumper point J3.